TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS

TEES

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ELECTRICAL EQUIPMENT GENERAL SPECIFICATIONS

CHAPTER 1-SECTION 1
ELECTRICAL TERMONOLOGY

1.1.1 Glossary of Terms

A	Amperes
AASHTO	American Association of State Highway and Transportation Officials
AC	Alternating Current
AC+	120 Volts AC, 60 hertz ungrounded power source
AC-	120 Volts AC, 60 hertz grounded return to the power source
AGENCY	Purchasing Government Agency
ANSI	American National Standard Institute
API	Application Program Interface
ASCII	American Standard Code for Information Interchange
Assembly	A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules
ASTM	American Society for Testing and Materials
ATC	Advanced Transportation Controller
AWG	American Wire Gage
bps	bits per second
Big Endian	The sequencing of byte order in memory such that the most significant byte is stored at the lowest memory address, with the next byte in significance stored at the next memory location, and so on.
C	Celsius
C Language	The ANSI C Programming Language
Cabinet	An outdoor enclosure generally housing the controller unit and associated equipment
Certificate of Compliance	A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications
Channel	An information path from a discrete input to a discrete output
CIA	CMS Controller Isolation Assembly
CIP	CMS Interface Panel
CMOS	Complementary Metal Oxide Semiconductor
CMS	Changeable Message Sign
CMS SYSTEM	Includes Controller Unit, Model 334C Cabinet, Interconnect Harnesses, CMS and other associated equipment required to operate the system.

Component	Any electrical or electronic device
Contractor	The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the AGENCY, as party(s) of the second part or legal representative
Controller Unit	That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly
CPDA	CMS Pixel Driver Assembly
CPDM	CMS Pixel Driver Module
CPMM	CMS Pixel Matrix Module
CPU	Central Processing Unit
CR	ACIA Control Register
CRC	Cyclic Redundancy Check
CTS	Clear to Send
DAT Program	The AGENCYs Diagnostic and Acceptance Test Program
Daughter Board	(from TechEncyclopedia) A Printed Circuit Board that plugs into another Printed Circuit Board to augment its capabilities
DB	Decibel
DBa	Decibels above reference noise, adjusted
DC	Direct Current
DCE	Data Communications Equipment
DIN	Deutsche Industrie Norm
DMA	Direct Memory Access
DTA	Down Time Accumulator
DTE	Data Terminal Equipment
DPST	Double Pole Single Throw
EG	Equipment Ground
EIA	Electronic Industries Association
EMI	Electro Magnetic Interference
Engineer	The AGENCY director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them
EPROM	Ultraviolet Erasable, Programmable, Read Only Memory Device
EEPROM	Electrically Erasable, Programmable, Read Only Memory Device
Equal	Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device
ETL	Electrical Testing Laboratories, Inc.

FCU	Field I/O Controller Unit.
Firmware	A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM
FLASH	An IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features
FPA	Front Panel Assembly
HDLC	High-Level Data Link Control
HEX	Hexadecimal
Hz	Hertz
IC	Integrated Circuit
I.D.	Identification
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
IPI	Initial Protocol Identifier
ISP	Internet Support Package
ISO	Short for "Isolated" and signifies that two or more power supplies each have different reference grounds.
ISO/IEC	International Standards Organization
ITE	Institute of Transportation Engineers
ITS	Intelligent Transportation Systems
Jumper	A means of connecting/disconnecting two or more conductive points by soldering/desoldering a conductive wire.
KB	Kilobytes
Laboratory	The established laboratory of the AGENCY or other laboratories authorized by the AGENCY to test materials involved in the contract
LED	Light Emitting Diode
LOGIC	Negative Logic Convention (Ground True) State
LSB	Least Significant Byte
Lsb	Least Significant Bit
MB	Megabyte
MSB	Most Significant Byte
Msb	Most Significant Bit
m	Milli
MPU	Microprocessor Unit
MIL	Military Specifications
MODEM	Modulation/Demodulation Unit
Module	A functional unit that plugs into an assembly

Motherboard	A printed circuit connector interface board with no active or passive components
MOS	Metal-Oxide Semiconductor
MOV	Metal-Oxide Varistor
MS	Military Standards
M/170	Program Module/Model 170 Controller Unit Connector
M/170E	Model 170E Auxiliary Board Connector
N.C.	Normally closed contact
N.O.	Normally open contact
NA	Presently Not Assigned. Cannot be used by the manufacturer for other purposes
NEMA	National Electrical Manufacturer's Association
NETA	National Electrical Testing Association, Inc.
n	nano
NLSB	Next Least Significant Byte
Nlsb	Next Least Significant Bit
NMSB	Next Most Significant Byte
Nmsb	Next Most Significant Bit
NTCIP	National Transportation Communication for ITS Protocol
PCB	Printed Circuit Board
PDA	Power Distribution Assembly
PLA/PAL	Programmable Array Logic Device
PMPP	Point-to-Multi-Point Protocol
ppm	Parts per million
PPP	Point-to-Point Protocol
PWM	Pulse Width Modulation
RAM	Random Access Memory
RDR	ACIA Receiver Data Register
RF	Radio Frequency
RMS	Root-Mean-Square
ROM	Read Only Memory Device
RTC	Model 170E Controller Unit Real Time Clock. This circuitry provides a 170E CPU IRQ Interrupt pulse clocked off the local power company's line frequency every 16.67 ms.
RTCA	Real Time Clock Adjuster Circuitry
RTS	Request to Send
RXD	Receive Data
R/W	Model 170E Controller Unit Read/Write Control Line

SCI	Serial Communications Interface
SDLC	Synchronous Data Link Control
S	Logic State
s	second
SS	Second Source. Produced by more than one manufacturer
Shunt	A means of connecting/disconnecting two conductive points on a solderless PCB post heater.
SR	ACIA Status Register
SRAM	Static Random Access Memory Device
SW	Switch
TB	Terminal Block
TDR	ACIA Transmit Data Register
TIA	Telecommunications Industry Association
TOD	Time of Day Clock
Triac	Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit
TTL	Transistor-Transistor Logic
TSD	Thumb Screw Device. A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No. 2 shall be flat black.) TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal. TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal. TSD No.3 - M3 SOUTHCO #47-81-181-10 or equal.
TXC	Transmit Clock
TXCI	Transmit Clock Input
TXCO	Transmit Clock Output
TXD	Transmit Data
µ	Micro
UL	Underwriter's Laboratories, Inc.
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VMA	Valid Memory Address
VME	Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
VMS	Variable Message Sign
X	Number Value
XX	Manufacturer's Option
WDT	Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and react

CHAPTER 1-SECTION 2
GENERAL

1.2.1 Chapter Conflict
In case of Chapter Conflict, the individual Chapter shall govern over Chapter 1.

1.2.2 Furnished Equipment
All furnished Equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

1.2.3 Interchangeability
The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

ASSEMBLIES	ASSOCIATED DEVICES
Output File #1LX & #2LX	Model 200 Switch Pack Model 210 Monitor Unit Model 430 Heavy Duty Relay
Input File	Model 222 & 224 Detectors Model 222i & 224i Detectors Model 242L & 252 Isolators
PDA #2LX	Model 204 Flasher Unit Model 206L/E Power Supply Module
PDA #3LX	Model 200 Switch Pack Model 206L/E Power Supply Module Model 208 Monitor Unit Model 430 Heavy Duty Relay
PDA #4L	Model 206L Power Supply CMS Isolation Module
Model 170E Controller Unit	Cabinet Models 33xLS, 34xLX & ATC (x=2,4,6 for Cabinets) Model 400 MODEM Model 412C Program Module

Model 2070 Controller Unit	Cabinet Models 33xLS, 34xLX & ATC (x=2,4,6 for Cabinets) Model 2070-1 CPU Module Model 2070-2 Field I/O Module Model 2070-3 Front Panel Assembly Model 2070-4 Power Supply Model 2070-5 VME Cage Assembly Model 2070-6 Serial Comm Module Model 2070-7 Serial Comm Module Model 2070-9 Dial-Up Comm Module Model 2070-X… Network Comm Module (X=Alphabetic Character for Network Modules)
ASSEMBLIES	**ASSOCIATED DEVICES**
Model 2070-N1 Controller Unit	Model 2070 Controller Unit Model 2070-8 NEMA Module Model 2070-2 Field I/O Module Model 2070-4N Field I/O Module
Model 2070-N2 Controller Unit	Model 2070 Controller Unit Model 2070-2N Field I/O Module Model 2070-4N Power Supply Module
Pixel Driver Assembly	Pixel Driver Module

1.2.4 Documentation

1.2.4.1 Manual

Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 8.5 in by 11 in paper, with the exception that schematics, layouts, parts lists and plan details may be on 11 in by 17 in sheets, with each sheet neatly folded to 8.5 in by 11 in size. Manual text font shall be ARIAL BOLD, size 12. Text characters shall be no more than 10 characters per 1 in and 7 lines per 1 in, with the exception of schematic text, which shall be no more than 18 characters per 1 in and 11 lines per 1 in.

1.2.4.2 Parts Listed

The State of California title, device name, date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals. The manual shall be separated into two volumes; volume one shall be labeled as Operating Manual and volume two shall be label as Electrical/Mechanical Drawings.

Volume one of the Manual shall include a table of contents and items 2 through 9 and Volume two shall include a table of contents and items 10 through 12 in order as listed:

Item #	Section #	Description
1	**N/A**	Table of Contents

2	**1**	Glossary
3	**2**	General Description
4	**3**	General Characteristics
5	**4**	Installation
6	**5**	Adjustments
7	**6**	Theory of Operation a. Systems Description (include block diagram). b. Detailed Description of Circuit Operation.
8	**7**	Maintenance a. Preventive Maintenance. b. Trouble Analysis. c. Trouble Shooting Sequence Chart. d. Wave Forms. e. Voltage Measurements. f. Alignment Procedures.
9	**8**	Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).
10	**9**	Electrical Interconnection Details & Drawings.
11	**10**	Schematic and Logic Diagram.
12	**11**	Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.

1.2.4.3 Cabinet Manuals

Manuals and Wiring Diagram Sheets for the Cabinet shall be furnished in a weatherproof plastic pouch placed in the cabinet. Cabinet Wiring Diagrams shall be on non-fading, minimum 22-inch x 34-inch sheets.

1.2.4.4 Draft

A preliminary Draft of the Manual shall be submitted to the Engineer for approval prior to final printing.

1.2.5 Packaging

Each item delivered shall be individually packed in its own shipping container. When loose styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the styrofoam.

1.2.6 Delivery

Each item delivered for testing shall be complete, including manuals, and ready for testing.

1.2.7 Metal Edges
All sharp edges and corners shall be rounded and free of any burrs.

1.2.7.1 Aluminum
Aluminum sheets shall be Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

1.2.7.2 Stainless Steel
Stainless Steel Sheets shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

1.2.7.3 Cold Rolled Steel
Cold Rolled Steel Sheets, Rods, Bars and Extruded shall be Type 1018/1020.

1.2.7.3.1 Plating
All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

1.2.8 Mechanical Hardware
All Hardware bolts, nuts, washers, screws, hinges and hinge pins shall be stainless steel unless otherwise specified.

1.2.9 Electrical Isolation
Within the circuit of any device, module, or PCB, Electrical Isolation shall be provided between DC logic ground, equipment ground and the AC- (Neutral) conductor. They shall be electrically isolated from each other by 500 MΩ, minimum, when tested at the input terminals with 100 Volts DC.

1.2.10 Daughter Boards
Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with four spacers / metal screws depending on the area supported. Connectors shall be either Flat Cable or PCB Headers. Components are allowed to be mounted under the daughter board.

CHAPTER 1-SECTION 3
COMPONENTS

1.3.1 General
All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

1.3.1.1 Special Design
When a component is of such Special Design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

1.3.1.2 Electronic Circuit
The Electronic Circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

1.3.2 Electronic Components

1.3.2.1 Socket Mounted
NO device shall be Socket Mounted unless specifically called out or requested and approved at Qualified Product List Submittal.

1.3.2.2 Rated Power
NO component shall be operated above 80% of its maximum Rated Voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

1.3.2.3 Manufactured Date
NO component shall be provided where the Manufactured Date is 3 years older than the contract award date. The design life of all components, operating continuously (24 hours a day, 365 days per year) in their circuit application, shall be 10 years or longer.

1.3.2.4 Encapsulation
Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators, transistor arrays and termination networks. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

1.3.2.5 Contractor
The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

1.3.2.6 Temperature Rating

All components used shall be designed to operate within the full temperature range specified. The component data sheets shall be the only accepted form of validation of the temperature range. Testing and/or screening of commercial grade components is not permitted.

1.3.3 Capacitors

The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150% except for supercaps which shall be 110%. Supercaps are capacitors rated less than 10 working Volts DC with capacitance values greater than or equal to 1.0F. Capacitor encasements shall be resistant to cracking, peeling and discoloration. With the exemption of Surface Mount Capacitors, all capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.

1.3.4 Potentiometers

Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements. Potentiometers with ratings less than 1 Watt shall be used only for trimmer type function. The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

1.3.5 Resistors

Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications MIL-PRF-22684F and Amendment 1. All resistors shall be insulated and shall be marked, except for surface mount, with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -34.6^0F and 165.2^0F.

1.3.5.1 Thermal

Special Ventilation or Heat Sinking shall be provided for all 2-watt or greater resistors. They shall be insulated from the PCB.

1.3.6 Semiconductor-Devices

1.3.6.1 Solid State

All Solid-State devices, except LED's, shall be of the silicon type.

1.3.6.2 Transistors / IC / Diodes

All Transistors, Integrated Circuits, and Diodes shall be a standard type listed by EIA. With exemption of Surface Mount Components, Transistors, Integrated Circuits and Diodes shall be clearly identifiable.

1.3.6.3 Metal Oxide Semi-Conductor
All Metal Oxide Semi-Conductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

1.3.6.4 Device Pin 1
Device Pin "1" locations shall be properly marked on the PCB adjacent to the pin.

1.3.7 Transformers / Inductors
With the exemption of Surface Mount Components, all power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

1.3.8 Triacs
Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.

1.3.9 Circuit Breakers
Circuit Breaker shall be UL 489 approved. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the Amperes rating shall be marked and visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from 0.4 ^{0}F to 122 ^{0}F. The minimum Interrupting Capacity shall be 5,000 Amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 Amperes and above, the minimum interrupting capacity shall be 10,000 Amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carling switch Time Delay Curve #24 or equal).

1.3.10 Fuses
All Fuses shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the chassis, PCB or beside the holder. Fuses shall be easily accessible and removable without use of tools.

1.3.11 Switches

1.3.11.1 Dual-Inline-Package-(DIP)
Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 mA, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 mA, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal). The DIP shall have recessed switches to prevent accidental switching.

1.3.11.2 5 VDC Logic Switch
5 VDC Logic rating shall be 0.4VA @ 20VAC or DC with contact material of gold over nickel plating or copper alloy. The switch shall be rated for a minimum of 40,000 operations.

1.3.11.3 12 -24 VDC Logic/Control Switches
12-24 VDC control switch contacts shall be rated for a minimum of five-Amperes resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.3.11.4 Power Rating
The switch contacts shall be rated for a minimum of 10 Amperes resistive load at 120 VAC or 28 VDC and shall be silver over brass or equal.

1.3.12 Terminal Blocks
The terminal blocks shall be barrier type, rated at 20 Amperes and 600 VAC RMS minimum. The terminal screws shall be 0.313 in minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

1.3.13 Wiring / Cabling / Harnesses

1.3.13.1 Harnesses
Harnesses shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize cross talk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements. Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.

1.3.13.2 AC Wiring
Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

1.3.13.3 Cabling
Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

1.3.13.4 Labeling
All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

1.3.13.5 Conforming
All conductors shall conform to MIL-W-16878G/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

1.3.13.6 Conductor Color

Conductor Color identification shall be as follows:

AC - (Neutral) circuits	White.
Equip. Ground	Solid green or continuous green color with 1 or more yellow stripes.
DC logic ground	Solid white or continuous white with a red stripe.
AC + (Line) circuits	Solid black or continuous black with colored stripe.
DC logic ungrounded or signal	Any color not specified.

1.3.14 Indicators / Displays

All indicators and character displays shall be readily visible at a radius of up to 4 ft within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

1.3.14.1 Indicators

All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and visibly illuminated when on. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15 degrees minimum shall be provided for Models 208, 210, 212, 222, 232, 242 and 252, as well as a clearance of 30 degrees minimum for Models 200, 204 and 206.

1.3.14.2 Character Displays

Liquid Crystal Displays (LCD) shall operate at temperatures of -4 ^{0}F to 158 ^{0}F.

1.3.15 Connectors

1.3.15.1 Keyed

All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

1.3.15.2 Type T

The Type **T** connector shall be a single row, 10 position, feed through terminal block. The terminal block shall be a barrier type with 6-32, 0.25 in or longer, nickel plated brass binder head screws. Each terminal shall be permanently identified as to its function.

1.3.15.3 Plastic Circular / M Type

Plastic Circular and M Type connectors - Pin and socket contacts for connectors shall be beryllium copper construction sub-plated with 0.00005 in nickel and plated with 0.0000299 in gold. Pin diameter shall be 0.061811 in. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

1.3.15.4 Edge / PCB

Card Edge and Two-Piece PCB Connectors

1.3.15.4.1 PCB Edge

PCB Edge connectors shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

Operating Voltage:	600 VAC (RMS)
Current Rating:	5.0 Amperes
Insulation Material:	Diallyl Phthalate or Thermoplastic
Insulation Resistance:	5,000 MΩ
Contact Material:	Copper alloy plated with 0.00005 in of nickel and 0.000015 in of gold
Contact Resistance:	0.006 Ohm maximum

1.3.15.4.2 Two Piece PCB

The Two-Piece PCB connector shall meet or exceed the DIN 41612.

1.3.15.4.3 PCB 22/44

The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 0.156 in contact centers.

1.3.15.4.4 PCB 28/56

The PCB 28/56 Connector shall have 28 independent contacts per side, dual sided with 0.156 in contact centers.

1.3.15.4.5 PCB 36/72

The PCB 36/72 Connector shall have 36 independent contacts per side, dual sided with 0.100 in contact centers.

1.3.15.4.6 PCB 43/86

The PCB 43/86 Connector shall have 43 independent contacts per side, dual sided with 0.100 in contact centers.

1.3.15.5 Wire Terminal Connectors

Each wire terminal shall be solderless with PVC insulation and a heavy-duty short -locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.

1.3.15.6 Flat Cable Connectors

Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 0.000015 of gold over 0.00005 inches of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 mega Ohms minimum.

1.3.15.7 PCB Header Post Connectors

Each PCB header post shall be 0.00155 in^2 by 0.343 in high; shall be mounted on 0.156 in centers; and shall be tempered hard brass plated with 0.000015 in of gold over 0.00005 in of nickel.

1.3.15.8 PCB Header Socket Connectors

Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 0.000010 in of gold over 0.00005 in of nickel.

1.3.16 Surge Protection Device

A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 μs and fall in 20 μs to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes. It shall have the following ratings:

Impulse Breakdown:	Less than 1,000 Volts in less than 0.1 us at 10 KV/us.
Standby Current:	Less than 1 mA.
Striking Voltage:	Greater than 212 Volts.

CHAPTER 1-SECTION 4
MECHANICAL

1.4.1 Assemblies
All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 0.75 in from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.4.2 PCB Design
No components, traces, brackets or obstructions shall be within 0.125 in of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.4.3 Model Numbers
The manufacturer's model and serial number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the State model number shall be displayed on the front panel in bold type, at least 0.25 in high.

1.4.4 PCB Connectors
All PCB Connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

1.4.5 Fasteners
All screw type Fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

1.4.6 Workmanship
Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.

1.4.7 Tolerances
The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	+/- 0.0525 in
PCB	+/- 0.010 in
Edge Guides	+/- 0.015 in

1.4.8 Thumb Screw Devices
Thumb Screw Devices (TSDs) shall be of the following type: retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No. 2 shall be flat black.)

TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal.
TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal.
TSD No.3 - M3 SOUTHCO #47-81-181-10 or equal.

1.4.9 PCB Modules

All PCB Modules shall be mounted vertically in their corresponding host assembly.

CHAPTER 1-SECTION 5
ENGINEERING

1.5.1 Human Engineering

1.5.1.1 Equipment
The Equipment shall be engineered for simplicity, ease of operation and maintenance.

1.5.1.2 Knobs
Knobs shall be a minimum of 0.5 in diameter and a minimum separation of 0.5 in edge to edge.

1.5.1.3 PCB
PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 4.5 lbs or greater than 50 lbs for insertion or removal.

1.5.2 Design Engineering
The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. The design shall take into consideration the protection of personnel from all dangerous voltages.

1.5.3 Generated Noise
No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits

CHAPTER 1-SECTION 6
PRINTED CIRCUIT BOARDS

1.6.1 Design, Fabrication and Mounting

The Design, Fabrication and Mounting of components and assemblies shall comply with the Association Connecting Electronics Industries Standards (IPC) as specifically listed in this specification. In the event of any conflict between the requirements of this specification and IPC standards, the IPC Standards shall govern.

1.6.1.1 Contacts on PCBs

All contacts on PCBs shall be plated with a minimum thickness of 0.00003 in gold over a minimum thickness of 0.000075 in nickel.

1.6.1.2 PCB Design

PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

1.6.1.3 Fabrication

Fabrication of PCBs shall be in compliance with IPC-4101B and Amendment 2, except as follows:

1.6.1.3.1 Copper Tracks

NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 in minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 1.0 ounces per square foot with adequate cross section for current to be carried. All copper tracks shall be plated or covered by solder mask to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

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1.6.1.3.2 Pits, Dents, Bows and Twists

Grade of Pits and Dents shall be of Grade B or better. The permissible bow or twist shall be Class C or better.

1.6.1.4 Mounting

The mounting of parts and assemblies on the PCB shall conform to IPC-2221A, Class 3, except as follows:

1.6.1.4.1 Semiconductor Devices

Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 50 ^{o}F or more shall be mounted with spacers, transipads or heat sinks where applicable to prevent contact with the PCB.

1.6.1.4.2 Residual Flux

When completed, all residual flux shall be removed from the PCB.

1.6.1.4.3 Resistance
Except where Surface Mount Components are used, the resistance between any 2 isolated, independent conductor paths shall be at least 100 MΩ when a 500 VDC potential is applied.

1.6.1.4.4 Coated
All PCBs shall be conformal coated with a UV Tracer. This coating shall to conform to the configuration of the object coated, applied on the completed board assembly. The coating shall be resistant to the effect of moisture and solvents.

1.6.1.4.5 Lateral Separation
Where less than 0.125 in lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.03125 in ± 0.0156 in thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

1.6.1.5 Connector Edges
Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 0.045 in ± 0.005 in for 0.1 in spacing and 0.055 in ± 0.005 in for 0.156 in spacing.

1.6.2 Soldering

1.6.2.1 Hand Soldering
Hand soldering shall comply with IPC-J-STD-00D and Amendments.

1.6.2.2 Automatic Flow Soldering
Automatic flow soldering shall be a constant speed, conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within ± 46.4 ^{o}F of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

1.6.2.3 Time-Temperature
If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

1.6.3 Definitions
Definitions for the purpose of this section on PCBs shall be taken from IPC-613 and Amendment 1.

CHAPTER 1-SECTION 7
QUALITY CONTROL

1.7.1 Components
All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

1.7.2 Subassembly, Unit or Module
Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

1.7.3 Predelivery Repair

1.7.3.1 Defects / Deficiencies
Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

1.7.3.2 PCB Flow Soldering
PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

1.7.3.3 Hand Soldering
Hand soldering is allowed for printed circuit repair.

CHAPTER 1-SECTION 8
ELECTRICAL, ENVIRONMENTAL AND TESTING REQUIREMENTS

1.8.1 General
The requirements called out in these specifications dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to ensure compliance.

1.8.2 Certification
These test procedures shall be followed by the Contractor who shall certify that they have conducted inspection and testing in accordance with these specifications.

1.8.3 Inspection
A visual and physical inspection shall include mechanical, dimensional and assembly conformance of all parts of these specifications.

1.8.4 Environmental and Electrical
All components shall properly operate within the following limits unless otherwise noted:

Applied Line Voltage: 90 to 135 VAC, note "Power Failure / Restoration" limits
Frequency: 60 (+/-3.0) Hertz
Humidity: 5% to 95%
Ambient Temperature: -34.6 ^{0}F to +165.2 ^{0}F
Shock - Test per Specification MIL-STD-810G Method 516.6.
Vibration - per Specification MIL-STD-810G Method 514.6.

1.8.4.1 Commencement Operation
All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

1.8.4.2 Equipment Compliance
All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in a State accepted cabinet connected to the commercial power lines.

1.8.4.3 Power Line Surge Protection
The power line surge protection shall enable the equipment being tested to withstand (non-destructive) and operate normally following the discharge of a 25 μF capacitor charged to ± 2,000 volts, applied directly across the incoming AC line at a rate of once every 10 seconds for a maximum of 50 occurrences per test. The unit under test will be operated at 68 ^{0}F ± 41 ^{0}F and at 120 (±12) VAC.

1.8.4.4 Operating
The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every

second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 68 ^{0}F ±41 ^{0}F and at 120 (+/-12) VAC.

1.8.4.5 Modules
The controller unit communications modules shall be tested resident in a State-accepted controller unit which in turn is housed in the cabinet.

1.8.4.6 CMS System Equipment
CMS system equipment will be tested for compliance as a complete system with power from commercial power lines applied at the CMS CIP Panel.

1.8.4.7 UL Requirements
Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

1.8.4.8 Normal Operation
All equipment shall continue normal operation when subjected to the following:

1.8.4.8.1 Low Temperature Test
With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be lowered from 68 ^{0}F to -34.6 ^{0}F at a rate of not more than 64.4 ^{0}F per hour. The item shall be cycled at -34.6 ^{0}F for a minimum of 5 hours and then returned to 68 ^{0}F at the same rate.

1.8.4.8.2 High Temperature Test
With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be raised from 68 ^{0}F to 165.2 ^{0}F at a rate of not more than 64.4 ^{0}F per hour. The item shall be cycled at 165.2 ^{0}F for 5 hours and then returned to 68 ^{0}F at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.3 Normal Operation
All equipment shall resume normal operation following a period of at least 5 hours at -34.6 ^{0}F and less than 10 percent humidity and at least 5 hours at 165.2 ^{0}F and 22% humidity, when 90 VAC is applied to the incoming AC.

1.8.4.9 Humidity and Ambient Temperature

The relative humidity and ambient temperature values in the following table shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY AT BAROMETRIC PRESSURES (29.92 In. Hg.)

Ambient Temperature/ Dry Bulb (in ^{0}F)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in ^{0}F)
-34.6 to 33.98	10	1.04 to 108.86
33.98 to 114.8	95	108.86
119.84	70	108.86
129.92	50	108.86
140.0	38	108.86
149.72	28	108.86
160.16	21	108.86
165.2	18	108.86

1.8.4.10 Opening and Closing of Contacts

All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

1.8.5 Contractor's Testing Certification

1.8.5.1 QC / Final Test

A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

1.8.5.2 Quality Control Procedure & Test Report

The quality control procedure and test report format shall be supplied to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

Acceptance testing of all supplied components.
Physical and functional testing of all modules and items.
A minimum 100-hour burn-in of all equipment.
Physical and functional testing of all items.

CHAPTER 1-SECTION 9
CONNECTOR DETAILS

Section Notes:

M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 Mega Ohms. The contacts shall be secured in the blocks with stainless steel springs.

M Type connector corner guides shall be stainless steel. The guide pins shall be 1.097 inches in length and the guide sockets shall be 0.625 inches in length.

Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated heat stabilized and fire resistant.

CHAPTER 2
MODEL 170E ENHANCED CONTROLLER & ASSOCIATED MODULES SPECIFICATIONS

2.1.1 System READ Access Time

With Model 412C Module Resident in the Controller Unit, valid data shall be present at the MPU at least 100 ns prior to the end of the machine cycle.

2.1.2 Diagnostic and Acceptance Test (DAT) Program

The DAT-170E Program shall be provided resident on the Model 412C Program Module U1 memory device and on the CPU U6 memory device. A copy of the DAT Programs will be available to the contractor at no charge.

2.1.3 PAL, EPROM, or ROM Devices

If a PAL, EPROM, or ROM device is used in address decoding and timing algorithms, the device code listing together with data sheet(s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the Contractor uses to directly reproduce the device.

2.1.4 System Address Organization

The system address organization of the Model 170E shall consist of two addressing configurations. The Decoder Input shall be furnished jumpered in address configuration 1. The internal module address organization shall be as specified in the appropriate module section.

2.1.4.1 Configurations

The two addressing configurations shall be selectable by use of one post jumper. The jumper shall control the Logic State of one Decoder Circuit Input. The logic line shall be a three-post type with the two logic levels on the outer posts. The following input line state conditions shall cause the Decoder circuit to provide the associated address configurations:

CONFIGURATION	LINE	FUNCTION
1.	+5 VDC	170E / 412C
2.	DC GND	170E INTERNAL / 170

2.1.4.2 Configuration 1-Address Organization

FUNCTION	ADDRESS RANGE	COMMENTS
CPU SRAM	0000-0FFF	
U4 Memory	1000-3FFF	412C
Reserved	4000-4FFF	
DTA Minutes	5000	READ
DTA Reset	5000	WRITE
INPUT / OUTPUT	5001-5008	
	5009-500A	WRITE
RESTART State	5004	BIT 1 READ
DTA Seconds	500F	READ
Reserve	5009-500E	READ
	500B-500F	WRITE
	5010-5FFE	
CPU STATUS	5FFF	READ Bit 1 – ACIA #1 IRQ Bit 2 – ACIA #2 IRQ Bit 3 – ACIA #3 IRQ Bit 4 – ACIA #4 IRQ Bit 5 – Reserved Bit 6 – Address Configuration Bit 7 – DTA Timeout Bit 8 – RTC IRQ
RTC Reset	5FFF	WRITE
ACIA #1	6000	WRITE CR, READ SR
ACIA #1	6001	WRITE TDR, READ RDR
ACIA #2	6002	WRITE CR, READ SR
ACIA #2	6003	WRITE TDR, READ RDR
ACIA #3	6004	WRITE CR, READ SR
ACIA #3	6005	WRITE TDR, READ RDR
ACIA #4	6006	WRITE CR, READ SR
ACIA #4	6007	WRITE TDR, READ RDR
Reserve	6008-600F	
CPU SRAM	6010-6FFF	

Program Module

Memory Write Protect	7000	WRITE
I.D. Feature	7000	READ
I.D. Location	7001	READ
	7001	WRITE Reserve
Reserve	7002-7009	
	700B-700E	WRITE
	700F	READ
RTCA Valid/Reset	700A	
RTCA Counters 1 to 4	700B-700E	READ
U3 Memory	7010-7FFF	
U1 & U2 Memory	8000- FFFF	

Note -- Address locations noted as "Reserve" are assignable by the Agency only and shall not be used. CPU STATUS Bit 6: "0" equals Address Configuration 1 and "1" equals Address Configuration 2.

2.1.4.3 Configurations 2-Address Organization

Configuration 2 Address Organization - This configuration provides all Model 412C Program Module features internal to the controller unit. The address organization is the same as CONFIGURATION 1 with the following exceptions:

CPU SRAM	0000-3FFF	U3 & U4 Memory internal
	6010-6FFF	
	7010-7FFF	
U6 EPROM	8000-FFFF	U1 & U2 Memory internal

2.1.5 Memory Devices

Each memory device shall stabilize to normal operation within 10 ms following Power Restoration and shall be in Standby until addressed. Each device shall have the following maximum power drain at +5 VDC in its various states:

MEMORY	ACTIVE	STANDBY	POWERDOWN
EPROM	100 mA	40 mA	-
SRAM	85 mA	20 mA	100 μA (non-internal power)

2.1.6 Prom Memory Sockets

PROM Memory Sockets shall be a 28 Pin AMP Diplomate LF #641894-2, or equal. The MPU, ACIA and other memory sockets shall be an AUGAT #500/800 series AG10DPC or equal. Each socket number shall be permanently marked on the PCB adjacent to its Pin 1. Should the "... or equal MPU" Pin / Package be other than the 40 pin package, the MPU socket used shall match the above specified socket features.

CHAPTER 2-SECTION 2
MODEL 170E CONTROLLER UNIT

2.2.1 Unit Composition

2.2.1.1 170E Controller Consisting
The Model 170E Controller Unit shall consist of the following:

Central Processing Unit (CPU)
Input / Output Interface
Unit Chassis
M170E Auxiliary Board
Model 412C Program Module
Unit Power Supply with external power connection
Unit Standby Power
Front Panel Assembly
Internal System Interface
Connectors C1S, C2S, C20S, C30S, C40S, and T-1
Communications System Interface

2.2.1.2 Configuration
The 170E shall be delivered pinned for Configuration 1 Addressing.

2.2.1.3 Composition Weight
The composition weight shall not exceed 25 lbs.

2.2.2 Central Processing Unit (CPU)

2.2.2.1 Micro Processing Unit (MPU)
The CPU shall be provided with an MPU and shall properly execute object programs developed to operate on the MPU. The MPU interrupt requirements shall be as follows:

2.2.2.1.1 Non-Maskable Interrupt (NMI)
The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the MPU NMI line to immediately go LOW. The line shall be held LOW until the RES goes LOW to prevent multiple NMI issuance.

2.2.2.1.2 Reset Interrupt (RES)
The RES is exclusively assigned to Power Restoration and MPU Startup. The RES line shall go LOW 3 (±1) ms following the NMI going LOW. The line shall remain LOW until 150 (±75) ms after Power Restoration.

2.2.2.1.3 Interrupt Request (IRQ)
The IRQ Line shall be jointly used by the RTC and Four ACIAs to initiate IRQ to the MPU.

2.2.2.1.3.1 Real Time Clock (RTC)

Real Time Clock circuitry shall be provided to trigger an interrupt to the MPU on the IRQ line once every 1/60 of a second during the 270 degree to 330 degree portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency. The RTC shall be READ at Bit 8, Address 5FFF (STATUS) and reset by a WRITE to Address 5FFF.

2.2.2.1.3.2 ACIA

Four ACIAs shall be provided, each capable of receiving and transmitting up to eight-bits of parallel data from the MPU for serial data communications. The ACIA shall have 4 registers which are addressable by the MPU. The MPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR) and writing in the Transmit Data Register (TDR) and in the Control Register (CR).

2.2.2.1.3.3 Jumpers

Each ACIA shall be provided with a 2-post type jumper between its IRQ output and the MPU IRQ input. The 170E shall be delivered with these jumpers installed.

2.2.2.2 CPU Clock Timing

The CPU clock circuitry shall be provided to generate the MPU clock timing. The clock circuitry and the MPU shall provide two selectable MPU machine cycle times of 0.651 and 1.302 (±0.0015) μs. The machine cycle time selection shall be by Post Jumper (Three Post Type) with jumper in for 1.302 μs. The CPU clock circuitry shall be located no further than 2 in from the MPU clock pin inputs.

2.2.2.3 SRAM Memory

SRAM Memory, DALLAS 1235Y or equal, shall be provided.

2.2.2.4 AN EPROM Memory

AN EPROM Memory, ST Microelectronics M27C256B or equal, shall be provided in socket U6.

2.2.2.5 Restart Timer

A Restart Timer Circuitry shall be provided to react to the duration of power outage. The Restart Timer output is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (±0.25) seconds, its output state shall go to LOW and remain in that state for 50 (±24) ms after the RES line goes HIGH. If power is restored prior to the timer timing out, the output shall remain HIGH and the timer shall be reset to “0”.

2.2.3 Downtime Accumulator (DTA)

2.2.3.1 Power Failure and Restoration

A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon NMI line going LOW and continue counting until the RES line goes HIGH following Power Restoration.

2.2.3.2 Binary Registers

The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ±1 second over the 255-minute range. The DTA shall stop counting when the Minutes register equals 255 decimal. Both DTA registers shall reset to 0 by a WRITE to Address 5000. The DTA shall READ Minutes at Address 5000 and Seconds at Address 500F. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and reset the other register to "0".

2.2.4 Current Drain

Total Current Drain for DTA AND Restart Timer Circuitry (power down mode) shall not exceed 400 μA at 5 VDC, 95^0F while timing and 100 μa at 5 VDC when timeout is latched.

2.2.5 Input / Output Interface

2.2.5.1 Ground True Logic

Input / Output Interface shall utilize a ground true logic. The transfer of data between interface and working registers within the MPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of the MPU read / write command at the time the given address is valid.

2.2.5.2 Output Interface

The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

2.2.5.3 Input Interface

The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC, shall be turned OFF (false) when the input current is less than 100 μa or the input voltage exceeds 8.5 VDC, shall pull up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

2.2.6 Unit Chassis

The controller unit shall be housed in a compact, portable metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 19-inch rack. The enclosure shall be designed for convenient removal of PCBs without the use of tools.

2.2.7 Unit Power Supply

2.2.7.1 Power Supply
A power supply shall be provided to produce all DC power necessary to operate the controller unit. In addition, the supply shall provide the following voltages and current:

1. 1000 mA at +12 VDC
2. 300 mA at -12 VDC
3. 500 mA at + 5 VDC
4. 400 mA at- 5 VDC

2.2.7.2 DC Ground
The DC ground shall not be connected to equipment ground.

2.2.7.3 Controller Unit power
Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ±17 ms beyond the NMI line going LOW.

2.2.7.4 Maximum DC Voltage
The maximum DC voltage generated shall not exceed 45 volts.

2.2.7.5 Power Supply
The Power Supply shall be so designed that no further filtering regulation is needed for the required DC voltages.

2.2.7.6 Radio Frequency Suppressors
Radio frequency suppressors shall be provided on the AC+ and AC- power lines. The part shall be COR COM 3VS1 or equal.

2.2.8 Unit Standby Power

2.2.8.1 Standby Power Supply
A standby power supply shall be provided to retain power (minimum of 72 hrs) to the CPU Restart Timer, DTA and Internal RTCA during power failure in the controller unit. The supply shall consist of holdup Capacitors, capacitor charging circuitry and power sense / transfer circuitry.

2.2.8.2 Power Sense / Transfer Circuitry
The power sense / transfer circuitry shall sense power loss and transfer battery power immediately to the required circuits. The transfer circuitry shall isolate the capacitors by transistor or relay until power loss transfer. The circuitry shall sense power restoration and transfer back to the normal isolation mode.

2.2.8.3 Charging Circuit
A charging circuit which shall, under normal operating conditions, fully charge and float the standby capacitors consistent with manufacturer's recommendations.

2.2.9 Front Panel Assembly

2.2.9.1 Fastening / Removing
The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

2.2.9.2 Connection
The front panel shall be electrically connected by means of Connector C3. The front panel shall be connected to equipment ground through Connector C3.

2.2.9.3 Character Displays
The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 0.4 in high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the MPU through the output interface to the display shall result in the display of each character in its non-inverted state.

2.2.9.4 Indicators
The front panel shall be provided with 10 LED CALL / ACTIVE indicators.

2.2.9.5 Keyboard
A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MPU shall result in each character being received in its non-inverted state. The character shall consist of 4 bits of binary data, while the character control shall consist of 1 bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 0.075 in^2 and shall be mounted on a minimum of 0.5 in centers; shall have an actuation force between 0.0001102 lbs and 0.0002205 lbs and shall provide a positive tactical indication of contact. Key contacts shall have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact opening.

2.2.9.6 Toggle LOGIC Switch
The front panel shall be provided with a toggle LOGIC switch to enable the stop timing function and shall be labeled "STOP TIMING".

2.2.9.7 Toggle CONTROL Switch and Fuse
An ON-OFF toggle CONTROL switch and fuse shall be provided for AC power. The switch and fuse shall protrude through the front panel, but shall remain with the controller unit chassis when the front panel is removed. The fuse shall be a 3AG Slow Blow type, rated at either 1 or 2 Amperes, dependent upon the controller unit power requirements.

2.2.9.8 Framework
The front panel, under the legend "OPERATING INSTRUCTIONS", shall include a framework to retain a card, 4 in wide by 6 in high by 0.063 in thick.

2.2.10 Internal System Interface

2.2.10.1 Connector Spacing
PCB to PCB Connector spacing shall be a minimum of 1 in. Continuous nylon card guides (permanent locking type) shall be provided for the modules and all internal PCBs.

2.2.10.2 22/44S & 36/72S PCB Connectors
Two PCB 22/44S Connectors shall be provided for the MODEM Modules MC1 and MC2, and two PCB 36/72S Connectors shall be provided for the M170 Connector / Program Module and the M170 Connector / M170E Auxiliary Board.

2.2.10.3 Depth Placement
The depth placement of the vertical M/170 Connector shall be such that the Program Module Front Panel shall be flush with the Model 170E Controller Unit Front Panel when the module is connected.

2.2.11 Data and Address Bus Requirements

2.2.11.1 Data Bus Buffers and Drivers
All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 ns.

2.2.11.2 Address Bus Inputs
All Address Bus Inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 picofarads.

2.2.12 Connector Requirements

2.2.12.1 Connector C1S
Connector C1S shall be mounted on the controller unit providing 44 inputs and 56 outputs of control interface to and from external devices or files.

2.2.12.2 400 MODEM and CPU ACIA Connections
The Model 400 MODEM and CPU ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (TYPE T Connector). The control and data transmission lines for ACIA 1 shall be paralleled through C2S and T-1 connectors. ACIA 2 lines shall be routed to C20S Connector, ACIA 3 to C30S, and ACIA 4 to C40S.

2.2.12.3 Signal Lines and Buffer
ACIA 4 RS 232 Signal Lines and Buffered mirrored signals NMI, RES and ROT Shall be internally route to M170 and M170E as noted in Pin Assignments under Section 5 Details.

2.2.13 Communication System Interface

2.2.13.1 Communication Consisting

The communication system shall consist of the CPU, ACIAs, motherboard connectors and lines, MODEM Module Connectors MC1 & MC2 and interfaces between ACIA & MODEM and both MODEM and ACIA to C2S, C20S, C30S, C40S and Connector / T-1 Terminal. The interface between the ACIA and MODEM shall comply with EIA RS-232-C Standards and all functions under T-1, C2, C20S, C30S, and C40S Connectors are referenced to the ACIA. AUDIO IN and AUDIO OUT are referenced to the MODEM. The RTS and TX Data lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12 VDC respectively.

2.2.13.2 Connectors

C20S, C30S, and C40S Connectors shall meet the requirements for the C2S Connector.

2.2.13.3 Frequencies

A minimum of four baud rate generator frequencies, 19.2 kHz, 38.4 kHz, 76.8 kHz and 153.6 kHz shall be provided at the ACIA Rx / Tx Clock Inputs (pins 3 & 4). The frequency selection shall be by post type jumpers. Each ACIA shall have independent baud rate selection with jumpers delivered pinned for 19.2 kHz.

2.2.14 Electrical Requirements

2.2.14.1 Connection

The front panel and chassis shall be connected to equipment ground.

2.2.14.2 Surge Arrestor

A surge arrestor shall be provided between the AC+ and AC- for protection against powerline noise transients. The surge arrestor shall meet the following requirements:

1. Recurrent peak voltage: 212 Volts
2. Energy rating maximum: 20 Joules
3. Power dissipation, average: 0.85 Watt
4. Peak current for pulses less than 6 us: 2000 Amperes
5. Standby current: less than 1 mA

2.2.14.3 Power Resistors / Inductance

Two 0.5 Ohm, 10-Watt wire-wound power resistors with a 0.2µH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three surge arrestors rated for 20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68µF capacitor shall be added between AC+ and AC- coming off the 0.5 Ohm resistor going to the surge arrestors.

2.2.14.4 AC Power

The AC power to the controller unit shall be supplied by a 3-conductor cable at least 3 feet in length. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

2.2.14.5 Test Points

Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such

that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 0.063 in diameter and 0.19 in high, minimum. The clearance between test points and other components shall be 0.25 in, minimum.

2.2.15 M170E Auxiliary Board

2.2.15.1 M170E Auxiliary Board

The M170E Auxiliary Board shall contain the RTCA Circuitry and the Identification Switches. (See Section 3 for the RTCA circuitry and the Identification Switch requirements.) The RTCA circuitry and the Identification Switches on the M170E Auxiliary Board shall be disabled when a Model 412C is installed. The M170 connector pins 71 and / or 72 shall provide a DC Ground path via the Model 412C Module (pins 69 & 70) to M170E connector (pins 71 & 72). A ground true present shall cause board feature disablement.

2.2.15.2 PCB Dimensions

The M170E Auxiliary Board's PCB dimensions shall meet the Model 400 Modem except for the PCB edge connector dimensions.

2.2.15.3 PCB Connector

The M170E Auxiliary Board's PCB connector shall be a PCB 36 / 72 and shall mate with the M170E connector.

CHAPTER 2-SECTION 3
MODEL 400, 400B AND 400BE MODEM MODULE

2.3.1 Modems
The Modems shall provide two-wire half-duplex and four-wire full-duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN / OUT.

2.3.2 Compliance
The Modems shall be compatible with Bell Standard 202S and comply with the following requirements:

Model	Mark Hz	Space Hz	Soft Carrier Hz	Data Rate bps
400	1200	2200	900	300 - 1200
400B	11200	17600	7800	300 - 9600
400BE	19200	38400	13800	300 - 19200

2.3.2.1 Modulation
Modulation: Phase coherent frequency shift keying (FSK).

2.3.2.2 Data Format
Data Format: Asynchronous, serial by bit.

2.3.2.3 Line and Signal Requirements
Line and Signal Requirements: Type 3002 voice-grade, unconditioned.

2.3.2.4 Interface
ACIA and Modem Interface: EIA - 232 Standards.

2.3.2.5 Tone Carrier Frequencies
Tone Carrier Frequencies (Transmit & Receive): MARK and SPACE with ±1% tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

2.3.2.6 Transmitting Output Signal Level
Transmitting Output Signal Level: 0, -2, -4, -6 and –8 dB (at 1700 Hz) continuous or switch selectable.

2.3.2.7 Receiver Input Sensitivity
Receiver Input Sensitivity: 0 to –40 dB.

2.3.2.8 Receiver Bandpass Filter
Receiver Bandpass Filter: Shall meet the error rate requirement and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

2.3.2.9 Clear-to-Send (CTS)
Clear-to-Send (CTS) Delay: 12 (±2) ms.

2.3.2.10 Receive Line Signal Detect Time
Receive Line Signal Detect Time: 8 (±2) ms mark frequency.

2.3.2.11 Receive Line Squelch
Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

2.3.2.12 Turn Off Time
Soft Carrier Turn Off Time: 10 (±2) ms.

2.3.2.13 Modem Recovery Timer
Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

2.3.2.14 Error Rate
Error Rate: Shall not exceed 1 bit in 100,000 bits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

2.3.2.15 Transmit Noise
Transmit Noise: Less than –50 dB across 600 Ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

2.3.3 Modem Power Requirements
The Modem power requirements are as follows:

Input Voltage	Maximum Current Consumption
+12 VDC	75 Milliamperes
-12 VDC	75 Milliamperes

2.3.4 Indicators
Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data.

CHAPTER 2-SECTION 4
MODEL 412C PROGRAM MODULE

2.4.1 General Requirements

2.4.1.1 Prevention
A device shall be provided to prevent the module, when inserted upside down, from making contact with the modules' mating connector within the controller unit.

2.4.1.2 Module PCB Connector
The module PCB Connector shall be provided with electrostatic discharge protection to prevent CMOS device damage.

2.4.1.3 VMA / Phase 2 (E) Clock Signal
The VMA / Phase 2 (E) Clock Signal (M/170 Pin 25) shall not be used in a memory device READ operation.

2.4.1.4 Current Requirements
The total module current requirements shall not exceed 450 mA at +12 VDC and 100 mA at +5 VDC.

2.4.1.5 Program Model 412 Identifier
Address 700E, Bit 8 shall permanently Read as "1". This bit state is used to differentiate between past delivered Model 412/64 modules (Bit 8 decoded "0") and the Model 412C module.

2.4.1.6 Module PCB Connector
The module PCB connector shall be a PCB 36/72P.

2.4.1.7 Module Front Panel
The module front panel shall be connected to Equipment Ground at M170 Pin 34.

2.4.1.8 Addressable Devices
All addressable devices shall be fully decoded.

2.4.1.9 Memory Sockets
All memory sockets shall be a 28 pin AUGAT #528/828 Series AG10DPC or equal.

2.4.2 Feature Requirements

2.4.2.1 Bus Inputs and Outputs

2.4.2.1.1 Data Lines
All data lines shall be tri-state buffered on the module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed, the data output lines shall be disabled into a high impedance state and the data lines shall not source or sink more than 100 μA.

2.4.2.1.2 Addressed Input Lines

All addressed input lines shall load the bus by 1 TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 ns.

2.4.2.2 Memory

2.4.2.2.1 Memory Sockets

Four numbered memory sockets shall be provided and fully decoded using the following method. The module shall be delivered with MEMORY SELECT #3 Configuration designated memory devices (OR EQUAL), address decode and jumpers.

2.4.2.2.2 Device Manufacturer

Device manufacturer is designated as INT-Intel, D-Dallas and HD-Hitachi. The sockets shall be decoded by block jumper selection as follows:

	MEMORY SELECT	SOCKET ADDRESS RANGE AND DEVICE			JUMPER PATTERN		
	U1	U2	U3	U4	1	2	3
1.	E000-FFFF INT2764A	C000-DFFF INT2764A	7010-7FFF DAL1225	1000-4FFF HD6264 OR HD62256	IN	IN	OUT
2.	C000-FFFF INT128A	8000-BFFF NT128A	SAME	SAME	OUT	IN	IN
3.	8000-FFFF	NOT ADRS	SAME	SAME	OUT	OUT	IN
4.	8000-FFFF INT27256A	3000-4FFF DAL1225	SAME	1000-2FFF SAME *	OUT	OUT	OUT

* The pin #26 jumper pattern shall provide either address line 13 for the HD62256 device or tied HIGH for CS2 function in HD6264. Pin 27 shall be assigned to WE function.

2.4.2.2.3 Jumper Positions

Jumper positions for Sockets U2 and U4 shall be provided to convert the sockets from an EPROM socket to a SRAM socket or vice versa. Jumper positions for Sockets U2, U3 and U4 shall be provided to convert the socket from a non-standby power socket to a standby power socket or vice versa. Sockets U2 and U3 shall be jumpered for non-standby power. Socket U4 shall be jumpered for standby power.

2.4.2.2.4 Write Protect Circuit (WPC)

A Write Protect Circuit (WPC) shall be provided to prevent writing to SRAM memory during the Controller Unit MPU RESET Interrupt Line in a LOW State. A WRITE to ADDRESS 7000 shall be decoded and shall activate the WPC to place the R/W in a READ ONLY State. A subsequent WRITE to ADDRESS 7000 shall be decoded and shall deactivate the WPC allowing R/W

function. The WPC state shall be brought out to address 700E, Bit 7 ("1" State means "active"). The WPC power drain shall not exceed 40 μA at +5 VDC.

2.4.2.3 Module Power Supply

2.4.2.3.1 Power Supply
A power supply shall be provided onboard the module consisting of a DC Regulation Circuit, Standby Power and all necessary support circuitry.

2.4.2.3.2 DC Regulator Device
A DC Regulator device with its circuitry shall be provided to reduce the +12 VDC to +5 VDC for module use. The Regulator shall have a minimum efficiency of 75% and provide +5±0.25 VDC from no load to full load with a maximum of 2% ripple.

2.4.2.3.3 Standby Power
Standby power shall be provided to holdup WPC, SRAM and RTCA circuits during a Model 170 Controller Unit Power Failure. A circuit shall be provided to sense the +12 VDC M/170 power line and switch to standby power when the line falls below +9 VDC. The standby power circuit shall switch off when the power line is greater than +11 VDC. The standby power shall be a standard "AA" cap terminal cell battery rated at a minimum of 1.6 Ampere-hours at 3.7 ±0.2 VDC. All module circuitry and devices shall not exceed a maximum power drain of 2 mA at 3.7 VDC on the Standby Battery.

2.4.2.3.4 Battery
The battery shall be delivered separate from the module. It shall not be used except for test loading check by the Contractor.

2.4.2.3.5 Battery Holder
A battery holder for a “AA” battery shall be provided securely mounted to the back of the front panel. The holder shall have a TAB header type connector attached to the battery's plus cathode mounting terminal.

2.4.2.4 Identification Switch Circuitry

2.4.2.4.1 Switch Packages and Associated Circuitry
Two identification packages 8-position SPST DIP switches and associated circuitry shall be provided. The switch packages shall be decoded at Address 7000 (features) and 7001 (locations). Each package shall have 8 SPST switch positions with each switch associated to a DATA Bit (Switch 1 to Bit 1 and so on). Switch ON shall denote a bit state and shall be read logic "1" by the 170 CPU MPU and Switch OFF shall denote bit state and shall be read logic "0" by the 170 CPU MPU.

2.4.2.4.2 Switch Package
The Switch Package shall be a DIP slide type.

2.4.2.5 Real Time Clock Adjuster (RTCA)

2.4.2.5.1 RTCA Adjusting
A RTCA shall be provided to adjust for missing RTC timing interrupts.

2.4.2.5.2 RTCA Accuracy
The RTCA shall be continuously powered and not affected by a controller unit power failure. RTCA accuracy shall be ±10 ppm at 77 ^{0}F. Integral devices incorporating RTCA features and functions may be used in lieu of individual components. The RTCA current drain shall not exceed 1.5 mA at +3.7 VDC.

2.4.2.5.3 Pulse Generator (PG)
The RTCA shall include a free running 60 Hz Pulse Generator (PG), a 24-bit binary counter counting 60 Hz pulses, 4 eight-bit buffer ports and port decode / PG interrupt logic. The PG shall trigger binary counter to increment on every input pulse, counting continuously until reset to 0 by its Reset Line. Bits 21, 22, 23 and 24 in an all "1"'s state shall cause that PG to be disabled (Binary Counter Bit 1 is the least significant bit).

2.4.2.5.4 Counter Bits
The counter bits shall be continuously read out to 4 eight-bit buffer ports. The ports shall be addressed and bits assigned as follows:

CPU ADDRESS	PORT BITS	COUNTER BITS	COMMENTS
700A	This address shall normally READ (decode) "55 HEX". If the standby power supply fails or is removed, it shall decode "54 HEX". A WRITE to this address will RESET the RTCA Binary Counter.		
700B	1-6	1-6	READ Only
700C	1-6	7-12	READ Only
700D	1-6	13-18	READ Only
700E	1-6	19-24	READ Only

2.4.2.5.5 LOGIC Switch
A SPST finger throw LOGIC switch shall be provided on the board to activate/deactivate standby power to the RTCA Circuitry. With the switch in the deactivated state the RTCA Circuitry shall present NO power drain to the standby power supply.

CHAPTER 2-SECTION 5
MODEL 400N ETHERNET MODULE

2.5.1 Model 400N Ethernet Module

The Model 400N Ethernet Module shall provide an EIA-232 Asynchronous communications channel. The Model 400N Ethernet Module shall be dimensionally and electrically designed to fit in a single slot of a standard 170 controller. The Model 400N Ethernet Module shall be a 170 plug-in module with EIA-232 activity LEDs on the front edge. The Network Model 400N Ethernet Module shall communicate over standard IEEE 802.3 networks using both TCP (point-to-point) and UDP (point-to-multipoint) protocols.

2.5.2 Mechanical/Electrical Requirements

The Model 400N Ethernet Module shall be dimensionally and electrically designed to fit in a single slot of a standard 170 controller. All components shall be protected from physical damage by a metal cover.

All EIA-232 LED Indicators shall be on the Front Panel.

The Model 400N Ethernet Module shall be provided with LED indicators for 10/100 and Half/Full Duplex Network Communications.

The Main Data Port shall be a 170 male 44 pin edge connector (PCB 22/44) located at the rear. The User Serial port shall be a DB9 Female connector accessible from the front. The Network port shall be a RJ45 modular jack connector accessible from the front. DIP switches shall be externally accessible. The Model 400N Ethernet Module shall be powered directly from the Model 170 Controller's Edge Connector (PCB 22/44).

2.5.3 Functional Requirements

The Model 400N Ethernet Module shall interface to the 170 controller using controller's Main Port EIA-232.

The Main and User Serial Ports shall operate EIA-232 Asynchronous communications and shall support data rates of 1.2, 2.4, 9.6, 19.2, 38.4, 57.5 and 115.2Kbps.

The Model 400N Ethernet Module Network Interface shall meet IEEE 802.3 and ANSI 8802-3 Standards and support 10/100 Mbps.

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The Auxiliary Port shall be configurable to operate as a DCE or DTE.

The Model 400N shall have an option to enable or disable Dynamic DCD.

2.5.4 Network Configuration

The Model 400N Ethernet Module shall support the following features:

TCP and UDP over IP protocols.

Subnet masks for Class A, B, and C networks (see table below):

NETWORK CLASS	HOST BITS	Subnet Mask	Example IP Address
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100
C	8	255.255.255.0	192.168.0.100

Manual or Automatic TCP/IP socket connections configuration.

Telnet access for both configuration and communications.

Dumb Terminal access using a User Serial port for configuring network parameters.

The Ability to adjust packet size and packing algorithm.

The Model 400N Ethernet Module shall be provided with a Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and Serial Settings using a Web Browser.

2.5.5 Data Interfaces

Main Data Port	Model 170 male 44 pin Edge Connector
User Serial Port	EIA-232 (DB9 Female)
Ethernet Data Port	RJ45 EIA 568B Pin Out

2.5.6 Switch Selections for half duplex and full duplex

User Serial Port Directionality	DTE/DCE
Main Port Operation	Enabled / Disabled
DCD	Constant / Switched
RXD Data Flow Control	Constant / Switched

2.5.7 LED Indicators

RTS Green or Red: DTE Request to Send

CTS Green or Red: Network Clear to Send

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

CD Green or Red: Network Data

2.5.8 Power Requirements

170 Module +12 VDC, 3 Watts

2.5.9 Environmental

The Model 400N shall operate within the specification listed in Chapter 1 Section 1.8.4.

CHAPTER 2-SECTION 6
MODEL 400F FIBER OPTICS MODULE

2.6.1 Model 400F Fiber Optics Module
The Model 400F Fiber Optics Module shall provide an RS232 Asynchronous communications channel. The Model 400F Fiber Optics Module (Model 400F) shall be a Plug-in Card style version for the 170 Controller. The Fiber Optic Model 400F shall operate over Single Mode Fiber.

2.6.2 Mechanical/Electrical Requirements
The Plug-in Card Model 400F shall have a protective cover or enclosure.

The Model 400Fs card edge connector shall be fully compatible with the 170 Controller's Modem card slot.

The Auxiliary Data port shall be a RJ45 connector.

All DIP Switches shall be accessed externally without disassembly of the Model 400F.

The Model 400F will be powered direct from the 170 Controller's edge connector.

2.6.3 Fiber Optics Module Requirements
The Model 400F shall meet the Fiber Optics Requirements of the Model 2070-6D Module as specified elsewhere in these specifications.

2.6.4 Electro Optical Requirements
The Model 400F shall meet the Electro Optical Requirements of the Model 2070-6D Module as specified elsewhere in these specifications.

2.6.5 Form Factor
See A2-8 for details

2.6.6 Power Requirements
The Model 400F shall draw less than 500mA on Model 170 ± 12VDC Power Supply.

2.6.7 Environmental
The Model 400F shall operate within the specifications listed in Chapter 1 Section 1.8.4

CHAPTER 2-SECTION 7
MODEL 170E DETAILS

NOTES:

1. Program module' height and width dimensions are maximum.
2. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.
3. All function under connector C2 & the terminal block T-1 are in reference to the MODEM
4. Detail Definitions:

BL = BLANKING
CC = CHARACTER CONTROL OR STROBE
CD = CARRIER DETECT
CH = CHARACTER
CTS = CLEAR TO SEND
DP = DECIMAL POINT
LS = LEAST SIGNIFICANT
MS = MOST SIGNIFICANT
NA = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
NLS = NEXT LEAST SIGNIFICANT
NMS = NEST MOST SIGNIFICANT
P&I = PHASE AND INTERVAL
RTS = REQUEST TO SEND

CHAPTER 3-SECTION 1
GENERAL REQUIREMENTS

3.1.1 Models 200 and 204 General

3.1.1.1 Unit Chassis
The unit chassis shall be made of metal suitable to meet rigid support and environmental requirements. Where electrical isolation is the only requirement, plastic insulation material can be used in lieu of metal.

3.1.1.2 Unit Control Circuitry and Switches
The unit control circuitry and switches shall be readily accessible by the use of a screwdriver or wrench. Only one type of screw head end (Slotted or Phillips) shall be used.

3.1.1.3 Unit Handle
The unit shall be so constructed that no live voltage is exposed. A handle shall be attached to the front panel for insertion or removal from the unit mating connector.

3.1.1.4 Unit Lower Surface
The unit shall be so constructed that its lower surface shall be no more than 2.06 in below the centerline of the connector and no part shall extend more than 0.9 in to the left or 1.1 in to the right of the connector centerline.

3.1.1.5 Edge Guides
Continuous edge guides shall be provided on the unit.

3.1.1.6 Switching
Each switch shall be capable of switching any Current from 0.050 to 10.0 Amperes (AC) load with power factor of 0.85 or higher.

3.1.1.7 Operations
Each switch shall be designed for a minimum of 300 Million operations while switching a tungsten load of 1000 Watts at 158 ^{0}F. Switch isolation between DC input and AC output circuit shall be at least 10,000 Mega Ohms at 2000 VDC.

3.1.1.8 Positions
Each switch shall turn ON within ± 5 degrees of the zero-voltage point of the AC sinusoidal line, and shall turn OFF within ± 5 degrees of the zero-current point of the alternating current sinusoidal line. After power restoration, the zero voltage turn ON may be within ± 10 degrees of the zero voltage point only during the first half cycle of line voltage during which an input signal is applied. Turn ON and OFF shall be within 8.33 ms following application or removal of the logic signal, respectively.

CHAPTER 3-SECTION 2
MODEL 200 SWITCH PACK UNIT

3.2.1 Switches
The Model 200 Switch Pack Unit shall be a modular plug-in device containing three solid-state switches. Each switch shall open or close a connection between applied power and external load.

3.2.2 Grounds
A Ground True Controller Unit Input (0 to 6 VDC) shall cause the switch to energize and a Ground False (16 VDC or more) shall cause it to de-energize, State transition shall occur between 6 and 16 VDC. The input shall not sink more than 20 ma or be subjected to more than 30 VDC. The input shall have reverse polarity protection.

3.2.3 Maximum Currents
With all switches on, the unit shall not draw more than 60 mA at +16 VDC or more from the +24 VDC cabinet supply.

3.2.4 Rating
Each switch shall have an OFF state dv/dt rating of 100 V/μs or better. Each switch shall be isolated so that line transients or switch failure shall not alter the controller unit.

3.2.5 Unit Front Panel
The unit front panel shall have an indicator on the input to each switch. The indicator shall be labeled or color-coded “Red”-top switch, “Yellow”-middle switch, and “Green”-bottom switch. The middle switch indicator shall be vertically centered on the unit front panel with the other indicators positioned 1 inch above and below.

3.2.6 Resistance
The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15K Ohms when the switch is in open state. When the switch is in off state the output current through the load shall not exceed 10 mA peak.

CHAPTER 3-SECTION 3
MODELS 204 - FLASHER UNIT AND 205 – TRANSFER RELAY UNIT

3.3.1 Model 204 Flasher Unit

3.3.1.1 Flasher Unit
The Flasher Unit shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. The unit's function is to alternatively open and close connections between applied power and external load.

3.3.1.2 Internal DC Power
The unit shall generate its own internal DC power from the AC Line.

3.3.1.3 Flashing
The unit shall commence flashing operation when AC power is applied providing 50 to 60 flashes per minute per switch with a 50 % duty cycle.

3.3.1.4 Rating
Each switch shall have an OFF state dv /dt rating of 200 V/μs or better.

3.3.1.5 Indicator
An indicator showing the switch's output state shall be provided. The two indicators shall be centered with 1 in minimum spacing.

3.3.1.6 Operation
Each circuit shall be designed to operate in an open-circuit condition without load for 10 years minimum.

3.3.1.7 Arrestor
A surge arrestor shall be provided between AC (pin 11) and Flasher Output (pins 7 & 8). The arrestor shall meet the following requirements:

Minimum Varistor Voltage	212 Volts
Average Power Dissipation	0.85 Watts
Peak I for pulses less than 6 us	3kA
Standby I	less than 1 mA

3.3.2 Model 205 Transfer Relay Unit

3.3.2.1 Type
The Transfer Relay Unit shall be of electromechanical type, designed for continuous duty:

3.3.2.2 Cover

Each unit shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating, and part number shall be placed on the cover. They shall be durable, permanent and readily visible.

3.3.2.3 Contacts

Each unit shall be provided with DPDT contacts. The contact points shall be of fine silver, silver alloy or a superior alternate material. Contact points and arms shall be capable of switching 20 Amperes or 1 Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitation. The points and arms shall be able to withstand 0.1 DA or 10 Gs, 10 –55 Hz without contact chatter.

3.3.2.4 Relay Coil

The relay coil shall have a power consumption of 2.0 Volt - Ampere maximum.

3.3.2.5 Relay Potential and Rating

Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a one cycle surge rating of 175 Amperes RMS and pickup and drop out within 20 ms.

CHAPTER 3-SECTION 4
MODEL 206L POWER SUPPLY UNIT

3.4.1 Unit Chassis
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.4.2 Unit Design
The unit shall provide +24 VDC to the cabinet files. The unit shall be a Switch-Mode design. It shall conform to the following requirements:

3.4.2.1 Input Protection
Two 0.5 Ohm, 10-watt wire-wound power resistors with a 0.2 µh inductance shall be provided (one on the AC+ Line & on the AC- Line). Three UL 1449 Varistors (MOVs), with a Nominal Discharge Current Rating (In) of 3kA shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 µf. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.4.2.2 Output Protection
The output shall be fused for over-current protection. The output shall also be protected against voltage transients by a suppressor with minimum rating of 1400 Watts.

3.4.2.3 Input and Output Fuses
Input/output fuse protection shall comply with IEC-60127.

3.4.2.4 Line and Load Regulation
Line and Load Regulation- shall not exceed +23 to + 25 VDC (4.2%) with a design voltage of +24 VDC at full load.

This includes ripple noise; from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 86 ^{0}F above ambient.

3.4.2.5 Design Voltage
Design Voltage +24 ± 0.5 VDC at full load, 86 ^{0}F, 115 VAC incoming voltage.

3.4.2.6 Full Load Current
Full Load Current 5 Amperes each for +24 VDC, minimum.

3.4.2.7 Ripple Noise
Ripple Noise - 2 volts peak-to-peak and 500 mV RMS at full load.

3.4.2.8 Efficiency
Efficiency (at full load) - 80% minimum.

3.4.2.9 Power Factor Correction

The Model 206L Power Supply shall include power factor correction circuitry resulting in a minimum full load power factor of 0.96.

3.4.2.10 Circuit Capacitors

Circuit capacitors shall be rated for 40 volts minimum.

3.4.2.11 Output Turn-on Delay

The Model 206L shall have an Output Turn-On Delay of less than 200ms from AC turn-on.

3.4.3 Front Panel and Terminals

The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

3.4.3.1 LED Indicators

LED indicators shall be provided on the Front Panel indicating AC Line input status and fuse integrity. The indicators shall also display output status and fuse integrity of the 24VDC output.

CHAPTER 3-SECTION 5
MODEL 208 MONITOR UNIT

3.5.1 Monitoring

The Model 208 Monitor Unit shall reliably sense and cause a relay output contact (Failed State) when monitoring the following:

A Watchdog Timer (WDT) Timeout Condition

Cabinet +24 VDC Power Supply below specified threshold

3.5.2 WDT Monitor Requirements

3.5.2.1 WDT Circuitry

WDT Circuitry shall be provided to monitor a controller unit output line state routed to the monitor unit at its assigned pin. The WDT Circuitry shall sense any line state change and the time between the last change. No state change for 1.5 ± 0.1 seconds shall cause a Failed State. The timer shall reset at each state change in a Non Failed state.

3.5.2.2 Unit Reset / WDT

Only the Unit Reset or a WDT inactive due to the voltage sense shall reset the WDT from a failed state.

3.5.2.3 Failed State

A Failed state caused by the WDT shall illuminate a front panel indicator light labeled “WDT ERROR”. The indicator shall remain ON until Unit Reset Issuance.

3.5.2.4 WDT Circuitry

The WDT Circuitry shall sense the incoming VAC Line and when the voltage falls below 98 ± 2 VAC for 50 ± 17 ms shall inhibit the WDT Function. When the WDT Circuitry senses the incoming VAC Line rise above 103 ± 2 VAC for 50 ± 2 ms the WDT shall become active. A hysteresis between the Voltage Inhibit and the Voltage Active Settings shall be a minimum of 3 Volts.

3.5.3 Power Supply Monitor Requirements

3.5.3.1 Monitor Unit

The monitor unit shall sense the Cabinet +24 VDC Power Supply Output Voltage. Voltages sensed at +18 VDC or below for a duration of 500 ms or longer shall cause a Failed state. Voltages sensed at +22 VDC or above shall NOT cause a failed state. Voltages sensed below +22 VDC for a duration of 200 ms or less shall NOT cause a Failed state. All timing and voltages conditions other than those specified above may or may not cause a failed state.

3.5.3.2 Indicator
A Failed state caused by sensing the power supply shall illuminate a front panel indicator light labeled “VDC FAILED”. The indicator shall remain ON until Unit Reset.

3.5.3.3 Unit Reset
Only Unit Reset shall reset the power supply sense circuitry from a Failed State.

3.5.4 Failed State Output Circuits
An electro-mechanical relay shall be provided to switch an output circuit during a Failed State. The relay coil shall be energized in a Non- Failed State. The relay contacts shall be rated for a minimum of 3 Amperes at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 ms or less.

3.5.5 Monitor Unit Reset
A momentary SPST Control switch labeled “RESET” shall be provided on the unit front panel to reset the monitor unit circuitry to a Non- Failed state. The switch shall be so positioned on the front panel that the switch can be operated while gripping the front panel handle.

3.5.6 Provision
The unit shall be provided with provision to drive an external NE2H light through a 56 K Ohm, 1/2-Watt series resistor (resident on unit).

3.5.7 PDA #3 WDT Reset Input
The PDA #3 WDT Reset Input shall not be sensed by the unit.

3.5.8 Output Relay
The output relay Contact for Failed State shall be Open.

CHAPTER 3-SECTION 6
MODEL 210 MONITOR UNIT

3.6.1 Monitor Unit Conditions

The Monitor Unit shall sense the following conditions and cause a FAILED STATE should any of the conditions exist:

1. The cabinet +24 VDC power supply below the voltage threshold.
2. The WDT Timeout Condition.
3. Conflicting field Output Circuit ON Condition.

3.6.2 Requirements

See Chapter 3, Section 5 Model 208 Monitor Unit for requirements on Power Supply Monitoring, Watchdog Timer, Failed State Output Circuits and Monitor Unit Reset.

3.6.3 Conflict Monitoring

The monitor shall sense up to 16 Channels for conflict (32 field outputs of Green and Yellow). The Green and Yellow are Logically OR'd together. The associated cabinet output file assignment or operator selected output switches shall determine channel assignment.

3.6.3.1 Monitored Field Output Voltages

All monitored field output voltages shall be measured as true RMS responsive (up to 3 KHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of 2 cycles. If digital means are used in calculating RMS, a minimum of 2 samples shall be taken per alternation.

3.6.3.2 Sensed Conflicting Field Output Voltages

Sensed conflicting field output voltages 25 VAC or greater for a duration of 500 ms or longer shall cause a Failed state. Sensed conflicting field output voltages between 15 VAC or less OR any voltage having a duration of 200 ms or less shall NOT cause a Failed state(s).

3.6.3.3 Conflict Monitoring Circuitry

The Conflict Monitoring Circuitry shall be capable of detecting both a positive and negative half-wave failure under the foregoing conditions.

3.6.3.4 Failed State

A Failed state caused by sensing voltage conflicts shall be reset only by the Unit Reset.

3.6.3.5 Indicators

Sixteen indicators shall be provided on the unit front panel to indicate if the channel output is sensed ON. The indicators shall remain ON in a latched state during a Failed state unless unlatched by Unit Reset or a unit loss of power during said Failed state.

3.6.4 Conflict Programming Card

3.6.4.1 PCB Programming Card

A plug-in PCB Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically labeled and laid out for easy identification of the diodes by channel. With diodes in place all output channels being monitored shall be in conflict. When the diode (anode to numerical pins and cathode to alphabetical pins) has been removed the channels shall be defined as non-conflict.

3.6.4.2 Pad / Placement

A pad for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin the yellow inhibit common shall disable sensing the said channel yellow.

3.6.4.3 Connection

The programming card shall intermate with a PCB 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provide a mechanically sound card and connector support including continuous card guides. When the programming card is resident in the unit, the card's front end shall be flushed with the unit's front panel.

3.6.4.4 Pins 16 and T

Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.

3.6.5 Conflicting

A front panel indicator labeled "CONFLICT" shall be provided. The indicator shall illuminate when there is a FAILED state caused by conflicting channels and go off only by Unit Reset Issuance.

3.6.6 Output Relay Contact

The output relay contact for FAILED State shall be "CLOSED".

3.6.7 Second Output Circuit

A second output circuit (STOPTIME controller input) shall be provided to sink an NPN Open Collector Transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50 mA at up to 30 VDC. A blocking diode shall be provided on the transistor output to prevent it from souring power into the controller unit.

3.6.8 LOGIC Toggle Switch

An internal SPST LOGIC toggle switch shall be provided on the Model 210 Monitor Unit to activate the WDT function. When the switch is ON the WDT Circuitry shall be active. The switch shall be mounted on the module PCB in a readily accessible location.

3.6.9 RESET Switch

The Front Panel RESET Switch shall be tied to the External Test Reset Input Line (Pin Z). The External Line shall be optically isolated from internal circuitry

CHAPTER 3-SECTION 7
COMMUNICATIONS AND CABINET HARNESS

3.7.1 C1 Harness

The C1 Harness shall be a minimum of 4 ft. in length. The harness wire bundle shall be provided with external protection and routed on the Input Panel Side of the cabinet. Adequate length shall be provided to allow the C1P Connector to properly connect any State Approved Model 170 Controller Unit mounted in the cabinet.

3.7.2 C1 Ends

One end of the C1 Harness shall be the C1P Connector with pin contacts wired per the detail assignment. The other ends of the harnesses shall terminate as follows:

Harness #1 - C4S Connector (connected to C4P on Output File #1)
C5S Connector (connected to C5P on either the Input Panel or Output File #2)
Assigned Input Files I & J Positions and Logic Ground Bus

Harness #2 - C5S Connector (same as Harness #1)
C6S Connector (connected to C6P on Output/PDA Assembly)
Assigned Input File I Positions and Logic Ground Bus

Harness #3 - C4S Connector (same as Harness #1)
Assigned Input File I Positions
Input Panel Terminal Block and Logic Ground Bus

3.7.3 C1 Harness #3/Output File #2 Adaptor

C1 Harness #3/Output File #2 Adaptor shall be comprised of a C4P Connector on one end and a C5S on the other. The adaptor shall interface the first 24 pins of C4 Connector to the 24 pins of C5.

3.7.4 C1 Conductors

Conductors between the C1 Connector and the Input File(s) shall be of adequate length to allow any conductor to be connected to any detector output terminal (Positions S, F, or W).

CHAPTER 3-SECTION 8
MODEL 280 INPUT FILE ETHERNET SWITCH UNIT

3.8.1 Model 280 Network Switch Unit
The Model 280 Unit shall provide 8 Ethernet Network Communications ports and two fiber optics communication ports. The Fiber Optics Communications shall meet the requirements of Chapter 10 Section 4 for the Model 2070-FX Network Communications Module.

3.8.2 Mechanical/Electrical Requirements.
The Model 280 Unit card edge connector shall be fully compatible with the Caltrans Cabinet Input File.

The Model 280 Unit shall be powered direct from the 206L, 206LS or 206E Power Supply.

3.8.3 Network Standards
The Model 280 Unit shall meet the IEEE802.3 10Base-T, IEEE 802.3u, and IEEE 802.3x.

3.8.4 Modes of Operation
The Model 280 Unit shall have auto-negotiation for 10/100 Mbps Connection speed and Half/Full-Duplex modes on all RJ-45 ports.

The Model 280 Unit shall be provided with Auto-MDIX for all RJ-45 ports.

3.8.5 Network Media Support
The Model 280 Unit shall be configured as a Multiple Channel Media Converter, three RJ-45 Front Panel Connectors.

The Model 280 Unit shall support the following Media:

100Baset-TX: Cat. 5, EIA/TIA-568B, 100-Ohm UTP cables.

3.8.6 LED Indicators
The Model 280 Unit shall be provided with RJ-45 Connectors containing Link/Activity and 10/100 Speed LED indicators.

3.8.7 Form Factor
See A3-11 for Details.

3.8.8 Power Requirements
The power requirements of the 280 Unit shall be within the power limitations of the Model 206 Power Supply as describe in Section 3.4 of these specifications.

3.8.9 Environmental
The Model 208 Unit shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 3-SECTION 9
MODEL 206E POWER SUPPLY UNIT

3.9.1 Unit Chassis
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.9.2 Unit Design
The unit shall provide +24 VDC to the cabinet files. The unit shall be a Switch-Mode design. It shall conform to the following requirements:

3.9.3 Input Protection
Two 0.5 Ohm, 10-watt wire-wound power resistors with a 0.2 µh inductance shall be provided (one on the AC+ Line & on the AC- Line). Three UL 1449 Varistors (MOVs), with a Nominal Discharge Current Rating (In) of 3kA shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 µf. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.9.4 Output Protection
The output shall be fused for over-current protection. The output shall also be protected against voltage transients by a suppressor with minimum rating of 1400 Watts.

3.9.5 Input and Output fuses
Input/output fuse protection shall comply with IEC-60127.

3.9.6 Line and Load Regulation
Line and Load Regulation- shall not exceed +23 to + 25 VDC (4.2%) with a design voltage of +24 VDC at full load.

This includes ripple noise; from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 86 ^{0}F above ambient.

3.9.7 Design Voltage
Design Voltage +24 ± 0.5 VDC at full load, 86 ^{0}F, 115 VAC incoming voltage.

3.9.8 Full Load Current
Full Load Current 10 Amperes each for +24 VDC, minimum.

3.9.9 Ripple Noise
Ripple Noise - 2 volts peak-to-peak and 500 mV RMS at full load.

3.9.10 Efficiency
Efficiency (at full load) - 80% minimum.

3.9.11 Power Factor Correction
The Model 206E Power Supply shall include power factor correction circuitry resulting in a minimum full load power factor of 0.96.

3.9.12 Circuit Capacitors
Circuit capacitors shall be rated for 40 volts minimum.

3.9.13 Front Panel and Terminals
The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

3.9.14 LED Indicators
LED indicators shall be provided on the Front Panel indicating AC Line input status and fuse integrity. The indicators shall also display output status and fuse integrity of the 24VDC output.

CHAPTER 3-SECTION 10
MODEL 700 POWER SUPPLY UNIT

3.10.1 Unit Chassis
The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. The Model 700 Power Supply shall be provided with mounting brackets so that it can be securely mounted as shown in A1-27.

3.10.2 Unit Design
The unit shall provide +24 VDC to power the PMMs. The unit shall be a Switch-Mode design. It shall conform to the following requirements:

3.10.3 Input Protection
Cold Start Inrush Current shall be less than 25Apk at 115VAC. Three UL 1449 Varistors (MOVs), with a Nominal Discharge Current Rating (In) of 3kA shall be provided between AC+ to AC, AC+ to EG, and AC- to EG.

3.10.4 Output Protection
The output shall be over-current and short-circuit protected. Output could drop out of regulation (<95%) when output current is 105% to 130% of full load. The output shall also be protected against voltage transients by a suppressor with minimum rating of 1500 Watts.

3.10.5 Input fuses
Input fuse protection shall comply with IEC-60127.

3.10.6 Line and Load Regulation
Line and Load Regulation- shall not exceed +23 to + 25 VDC (4.2%) with a design voltage of +24 VDC at 50% load.

This includes ripple noise; from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 86 ^{0}F above ambient.

3.10.7 Design Voltage
The power supply shall include an ORing Diode/FET and current sharing functionality. Design output +24.5 ± 0.1 VDC at 0.2A load and linearly drops to 23.5 ± 0.1 VDC at full load, 86 ^{0}F, 115 VAC incoming voltage.

3.10.8 Full Load Current
Full Load Current 31 Amperes each for +24 VDC, minimum.

3.10.9 Ripple Noise
Ripple Noise - 2 volts peak-to-peak and 500 mV RMS at full load.

3.10.10 Efficiency
Efficiency (at full load) - 80% minimum.

3.10.11 Power Factor Correction
The Model 700 Power Supply shall include power factor correction circuitry resulting in a minimum full load power factor of 0.98.

3.10.12 Circuit Capacitors
Circuit capacitors shall be rated for 35 volts minimum.

3.10.13 Front Panel and Terminals
The front panel shall include AC fuses, power ON light and test points for monitoring the output voltages at the upstream of the ORing Diode/FET. The unit including terminals shall be protected to prevent accidental contact with energized parts.

3.10.14 LED Indicators
LED indicators shall be provided on the Front Panel indicating AC Line input status and fuse integrity. The indicators shall also display output status of the 24VDC output.

CHAPTER 3-SECTION 11
AUXILIARY EQUIPMENT & HARNESS DETAILS

CHAPTER 4
REFER TO BATTERY BACKUP SYSTEM SPECIFICATIONS

CHAPTER 5
SPECIFICATIONS DETECTOR SENSOR UNITS, ELEMENTS AND ISOLATORS

CHAPTER 5-SECTION 1
GENERAL REQUIREMENTS

5.1.1 Sensor and Isolator Channels

The sensor and isolator channels shall be operationally independent from each other. Each sensor or isolator channel shall draw no more than 50 mA from the +24 VDC cabinet power supply and shall be insensitive to 700 mVolts RMS ripple on the incoming +24 VDC line.

5.1.2 Front Panel

The sensor unit or isolator front panel shall be provided with the following:

Hand pull to facilitate insertion and removal from the input file.
Control switches and Channel Indicators.
Channel visual indication of detection or incoming signal.

5.1.3 Output

Each sensor or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs. The output shall have a minimum impedance of 2 Mega Ohms when no vehicle is detected.

5.1.4 Valid Channel Input

A valid channel input shall cause a channel Ground True Output to the controller unit of a minimum 100 ms in duration. An onboard two-post shunt jumper shall be provided to disallow this requirement when the jumper is in an OPEN position.

5.1.5 Sensor Unit

The sensor unit or sensing element shall operate and interface successfully with an associate CALTRANS Standard Sensing Unit or Element.

5.1.6 Output Transistor

The output transistor shall switch from OFF to ON state or ON to OFF state in 20 μs or less.

5.1.7 Onboard Protection

Onboard protection shall be provided to enable the sensor unit or isolator to withstand the discharge of a 10 μF capacitor charged to +/- 1000 Volts directly across the input pins with no load present. With a dummy load of 5 Ohms, protection shall enable the sensor unit or isolator to withstand the discharge of a 10 μF capacitor charged to +/- 2000 Volts directly across either the input pins or from either side to equipment ground.

CHAPTER 5-SECTION 2
MODEL 222 & 224 LOOP DETECTOR SENSOR UNIT REQUIREMENTS

5.2.1 Sensor Unit Channel
The sensor unit channel shall produce an output signal when a vehicle passes over or remains over wire loops embedded in the roadway. The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease in inductance of the circuit measured at the input terminals of the sensor unit. The detector zone shall include all configurations listed in paragraph **5.2.9.1**.

The loops connected to each unit channel shall be scanned alternatively to minimized crosstalk.

5.2.2 Open Loop
An open loop shall cause the sensor unit channel to output a signal.

5.2.3 Detection
Each sensor unit channel shall be capable of detecting all types of California licensed motor vehicles when connected to the loop configuration/lead-in requirements of 5.2.9.1

5.2.4 Sensor Unit Compliance
The sensor unit shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 50 to 700 μH with a Q-parameter as low as 5 at the sensor unit operating frequency.

5.2.5 Loop Inputs
Loop inputs to each channel shall be transformer isolated.

5.2.6 Switches
Each individual channel shall have a minimum of 4 switch selectable operating frequencies.

5.2.7 Tuning Circuits
The sensor unit channel tuning circuits shall be automatic and shall be so designed that drift caused by environmental changes, or changes in applied power shall not cause an actuation.

5.2.8 Modes Selection Requirements
Each sensor unit channel shall have Pulse and Presence selectable modes.

5.2.8.1 Pulse Mode

5.2.8.1.1 Vehicle Presence
In the Pulse Mode, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 (± 25) ms in duration.

5.2.8.1.2 Detection Zone

Should a vehicle remain in a portion of the detection zone for a period in excess of 2 seconds, the sensor unit channel shall automatically "tune out" the presence of said vehicle. The sensor unit channel shall then be capable of detecting another vehicle entering the same detection zone. The recovery time to full sensitivity between the first vehicle pulse and channel capability to detect another vehicle shall be 3 seconds maximum.

5.2.8.2 Presence Mode

5.2.8.2.1 Duration

In the Presence Mode, the sensor unit channel shall recover to normal sensitivity within 1 second after termination of vehicle presence in the detection zone regardless of the duration of the presence.

5.2.8.2.2 Presence Sensitivity Settings

The channel sensitivity settings shall be provided that detect the presence of a vehicle in the detection zone for a specified time period and inductance change(s). The conditions are as follows:

	Minimum Time Duration	Detector Input Inductance Change
Setting 6	3 Minutes 10 Minutes	0.02% or more 0.06% or more
Setting 2	4 Minutes	1.00% or more

5.2.9 Sensitivity

5.2.9.1 Standard Plans Loop Configurations

California Standard Plan ES-5A & B Loop Configurations. (California Department of Transportation Standard Plans.)

5.2.9.1.1 Single Type-250

Single Type A, B, Q or Round Loop with a 250 ft lead-in cable.

5.2.9.1.2 Single Type-1000

Single Type A, B, Q or Round Loop with a 1000 ft lead-in cable.

5.2.9.1.3 4 Type-Series/Parallel-250

4 Type A, B, or Q Loops connected in series/parallel with a 250 ft lead-in cable.

5.2.9.1.4 4 Type-Series-1000

4 Type A, B, Q or Round Loops connected in series with a 1000 ft lead-in cable.

5.2.9.1.5 Type C-250

One 50-foot Type C Loop with a 250 ft lead-in cable.

5.2.9.2 Sensitivity Settings

Each sensor unit channel shall be equipped with a front panel selectable sensitivity setting(s) in presence and pulse modes to accomplish the following under operational and environmental requirements of this specification.

5.2.9.2.1 Setting 2

Each sensor unit channel shall respond while in setting 2 to a nominal change in inductance between 0.15% to 0.4% (median sensitivity of 0.32%) while connected to the above **5.2.9.1** loop configuration. This setting shall not respond to an inductance change of less than 0.1%

5.2.9.2.2 Setting 6

Each sensor unit channel shall respond while in the setting 6 to an induction of 0.02% while connected to the above **5.2.9.1** loop configuration.

5.2.9.3 Vehicle Detection

The sensor unit channel shall not detect vehicles, moving or stopped, at distances of 3 ft or more from any loop perimeter, in all configurations listed in paragraph **5.2.9.1**

5.2.9.4 Differ

All sensitivity settings shall not differ +/- 40% from the nominal value chosen.

5.2.9.5 Selectable Sensitivity Setting(s)

There shall be a minimum of 7 selectable sensitivity settings including specified sensitivity settings.

SETTING	SENSITIVITY	SETTING	SENSITIVITY
1	0.64%	5	0.04%
2	0.32%	6	0.02%
3	0.16%	7	0.01%
4	0.08%	8	Channel OFF

5.2.10 Response Time

Response time of the sensor unit channel for Sensitivity Setting, 2 shall be less than 5 ± 1 ms. That is, for any decreased inductive change which exceeds its sensitivity threshold, the channel shall output a ground true logic level within 5 ± 1ms. When such change is removed, the output shall become an open circuit within 5 ± 1ms.

5.2.11 Normal Operation

The sensor unit channels shall begin normal operation within 2 seconds after the application of power or after a reset signal of 30 μs.

5.2.12 Lightning Protection

Lightning Protection shall be installed within the sensor unit as defined in the Section 5.1.7 of these specifications.

5.2.13 Tracking Rate
The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.

5.2.14 Tracking Range

5.2.14.1 Inductance
The sensor unit shall be capable of normal operation as the input inductance is changed ± 5.0% from the quiescent tuning point regardless of internal circuit drift.

5.2.14.2 Resistance
The sensor unit shall be capable of normal operation as the input resistance is changed ± 0.5% from the quiescent tuning point regardless of internal circuit drift.

5.2.15 Temperature Change
The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes with the rate of temperature change not exceeding 1°C per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18°C between the inside and outside air shall not affect the proper operation of the sensor unit.

5.2.16 Switch
A switch or switch position shall be provided on the front panel to disable each channel output.

CHAPTER 5-SECTION 3
MAGNETIC DETECTOR REQUIREMENTS

5.3.1 Model 231 Magnetic Detector Sensing Element

5.3.1.1 Sensing Element

Each sensing element shall be designed for ease of installation, repositioning, and removal. The sensing element shall be 2.24 in maximum in diameter, have no sharp edges, and its length not to exceed 18 in. The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a 100 ft lead-in cable. Leakage resistance shall be a minimum of 10 MegaOhms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a saltwater bath after the device has been entirely immersed in the bath for a period of 24 hours at 68 ^{0}F +/- 37.4 ^{0}F. The saltwater bath concentrate shall be one fourth ounce of salt per gallon of water.

5.3.1.2 Lead-In

Each sensing element including lead-in shall have a DC resistance of less than 3500 Ohms and an inductance of 20 Henrys +/- 15 %.

5.3.2 Model 232 Two Channel Magnetic Detector Sensing Unit

5.3.2.1 Sensing Channel

When resident in an active cabinet input assembly and attached to one or more Model 231 Sensing Elements resident in conduit under the travel way, the sensing channel shall output a Ground True Output to the Controller Unit when sensing an induced voltage caused by a California Licensed Vehicle passing within 6 ft from an element with a 1000 ft of lead-in cable at all speeds between 3.11 and 80.78 mile per hour. The sensing channel output shall be continuous as long as the vehicle is detected. A rotary sensitivity adjusting knob for Gain (0 to Full) and a momentary test switch providing a voltage test input shall be furnished for each channel on the front panel.

CHAPTER 5-SECTION 4
MODEL 242L TWO-CHANNEL DC ISOLATOR REQUIREMENTS

5.4.1 Model 242 DC Isolator Channel
The Model 242 DC Isolator Channel shall provide isolation between a VDC input circuit (external electrical switch closure) and the controller unit input. The minimum isolation shall be 1000 mega Ohms and 2,500 VDC measured between the input and the output of the same channel.

5.4.2 Test Switch
Each isolation channel shall have a front panel mounted test switch to simulate valid input. The test switch shall be a single-pole double-throw, three position CONTROL test switches: The position assignment shall be UP – constant ON; MIDDLE – OFF; and DOWN – momentary ON.

5.4.3 Power Source
The DC Isolator operating voltage shall be obtained from the cabinet's 24 VDC power supply. The isolator shall have an internal isolated dc-dc power supply supplying 20 +/- 4 VDC to the field input side of the isolation channels. This internal isolated power supply shall provide at least 1500 Vrms of isolation from the cabinet 24 VDC power supply. The isolator shall not draw more than 2.0 watts of DC power. PCB should be two-layer design minimum, using plated-thru vias, and Gold-Plated Fingers on Both Sides of PCB.

5.4.4 Onboard Jumper
An onboard two-post shunt jumper shall be provided to allow for minimized output durations of less than 100 ms when the jumper is in the OPEN position.

5.4.5 Channel Contact Closure Input
A valid channel input shall cause a channel Ground True Output to the controller unit of a minimum 100 ms in duration. A channel contact closure input of 5 ms or less shall not cause an output (ground true) to the controller. A contact closure between 5 and 10 ms may or may not cause an output to the controller. A contact closure input of 10 ms or greater shall cause an output to the controller. The output pulse width shall be a minimum of 100ms upon a valid input, unless onboard jumper is in the OPEN position, in which case the output pulse width shall be minimized and return to a false state immediately following completion of valid input.

5.4.6 Field Input
Each isolation channel field input shall be turned on (true) when a contact closure causes an input voltage of less than 8 VDC and shall be turned off (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA nor more than 40 mA to an electrical contact closure or short from the power supply. Each input shall be provided with electrical transient protection.

5.4.7 Outputs
Each isolation channel output shall be an opt-isolated NPN open collector capable of sinking 50 mA at 30 Volts. The outputs shall be compatible with Model 2070 controller.

CHAPTER 5-SECTION 5
MODEL 252 TWO-CHANNEL AC ISOLATOR

5.5.1 Model 252 Two-Channel AC Isolator
The Model 252 Two-Channel AC Isolator shall contain 2 isolation channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits.

5.5.2 Channel Input Voltage "Von"
A channel input voltage "Von" of 80 +/- 5 VAC applied for a minimum duration of 110 ms ± 10 ms shall cause an output (Ground True) to the controller unit.

5.5.3 Channel Input Voltage "Voff"
A channel input voltage "Voff" (Von minus 10 VAC) applied for a minimum duration of 110 ms ± 10ms shall cause an output (Ground False) to the controller unit.

5.5.4 Post Jumper
A two-post jumper shall be provided to select inverted output states for Von and Voff. When in CLOSED position (Grounded) Von shall cause a Ground False output. An indicator shall be provided on the front panel labeled 'RR" which shall indicate a Voff input, Ground True output.

5.5.5 Input Impedance
The input impedance of each channel shall be between 6,000 - 15,000 Ohms at 60 Hz.

5.5.6 Minimum Isolation
The minimum isolation shall be 1000 mega Ohms between the input and output terminals at 500 AC applied voltage.

5.5.7 Power Source
The AC Isolator operating voltage shall be obtained from the cabinet's 24Vdc power supply. The isolator shall not draw more than 2.0 watts of DC power. PCB should be two-layer design minimum, using plated-thru vias, and Gold-Plated Fingers on Both Sides of PCB.

5.5.8 Outputs
Each isolation channel output shall be an opt-isolated NPN open collector capable of sinking 50 mA at 30 Volts. The outputs shall be compatible with Model 2070 controller.

5.5.9 Input Transient Protection
Each isolation channel output shall be provided with electrical transient protection.

CHAPTER 5-SECTION 6
MODEL 222I & 224I INTELLIGENT LOOP DETECTOR SENSOR UNIT REQUIREMENTS

5.6.1 General
The sensor unit must comply with section 5.2 requirements for Model 222 and 224 detectors and the enhancements described in this specification. The unit must be a scanning detector with 2 or 4 channels. Each unit must have the capability to detect any type of vehicle reliably, including bicycles.

5.6.2 Temperature Compensation
Temperature changes as described in 5.2.15 must be compensated for by the unit circuitry rather than by creating a housing for the circuit. Unit must also include LCD heater.

5.6.3 Network
Each unit must have an RJ45 Ethernet port compliant with EIA 568B standard for communication.

The unit must be provided with a Web-Based-Interface (WBI) allowing the user to observe data output and configure any channel through a Web browser.

The unit shall have a default IP address of 192.168.222.51 and subnet mask 255.255.255.0.

5.6.4 Display
As a minimum, the WBI shall display:

1. Settings for each channel as described in "Configuration and Output": operating mode, sensitivity level, frequency, network parameters, firmware version
2. Real-time traffic data: inductance change or percent inductance change, vehicle count, speed, and occupancy of vehicles traveling over the loop (single or dual loops)

5.6.5 Configuration and Output
As a minimum, the user must be able to use the Web browser for the following:

1. Change operating modes (presence or pulse)
2. Change sensitivity level
3. Configure network parameters
4. Program new images to device
5. Upgrade firmware
6. Reset the device
7. Output session data to .txt file

5.6.6 Lead-in Cable
The unit shall be able to detect vehicles with a 2500-foot lead-in cable.

5.6.7 Selectable Sensitivity Settings

There shall be a minimum of 15 selectable sensitivity settings including specified sensitivity settings.

SETTING	SENSITIVITY	SETTING	SENSITIVITY
1	0.64%	9	0.08%
2	0.56%	10	0.06%
3	0.48%	11	0.04%
4	0.40%	12	0.02%
5	0.32%	13	0.01%
6	0.24%	14	0.005%
7	0.16%	15	0.0025%
8	0.12%	Off	Channel Off

5.6.8 Bicycle Detection

Each unit must be able to detect bicycles reliably using the standard Type D loops. The reference bicycle defined by the California MUTCD has a minimum 16-inch wheel size with aluminum rims and stainless-steel spokes. The frame, fork, and cranks are non-ferromagnetic.

5.6.9 Vehicle Classification

The sensor unit shall have vehicle classification capability as described by the Federal Highway Administration (FHWA) Traffic Monitoring Guide (TMG). The vehicle classification data must include the following information: location ID, direction of travel code, lane of travel/channel, date (month, day, year), time, total internal volume/occupancy, restrictions, and vehicle class.

The traditional classified by the FHWA are described in Appendix C of the TMG; the classes are:

Class 1: Motorcycles
Class 2: Passenger Cars
Class 3: Two-Axle, Four-Tire Single Unit
Class 4: Buses
Class 5: Two-Axle, Six-Tire Single Unit
Class 6: Three-Axle, Single Unit
Class 7: Four or More Axle, Single Unit
Class 8: Four or Less Axle, Single Trailer
Class 9: Five-Axle Tractor Semitrailer
Class 10: Six or More Axle, Single Trailer
Class 11: Five or Less Axle, Multi Trailer
Class 12: Six-Axle, Multi Trailer
Class 13: Seven or More Axle, Multi Trailer

In addition to FHWA's axle-based classifications the Model 222i shall include the following length-based classifications:

Length-based Vehicles	Length (ft)
Motorcycles	< 7
Small	7 - 22

Medium	22 - 49
Large	49 - 85
Very Large	85 +

The unit must be able to classify a minimum of 5 length-based vehicle types, plus bicycles.

5.6.10 Warranty

Each unit shall have a manufacturer's warranty of at least 4 years covering defects and impairment of operation discovered during normal, expected use of the device. Under the warranty, the manufacturer shall repair or replace the unit within 60 days of receiving the unit.

CHAPTER 5 SECTION 7
SENSOR & ISOLATOR DETAILS

CHAPTER 6
CABINET SPECIFICATIONS MODELS 332LS, 334LS, 336LS, 342LX, 344LS & 346LX

CHAPTER 6-SECTION 1
GENERAL REQUIREMENTS AND CABINET MODEL COMPOSITION

6.1.1 Composition

Unless otherwise specified the model shall be furnished, ready for operation with the following composition.

Cabinet Model	PDA	6.2.2.3 Output Files		Power Supply
332LS	2LX	1LX	2LX (Model 520)	206L
334LS	3LX			206L
336LS	2LS	1LX		206LS
342LX	2LX	1LX	2LX (Model 520)	206E
344LX	3LX			206E
346LX	2LS	1LX		206LS

6.1.1.1 Model 332LS Cabinet

Model 332LS Cabinet shall consist of:

Housing 1 B
Mounting Cage 1
PDA #2LX
Input Files I & J
C11 Harness
Output File #2LX (Model 520)
Output File #1LX
C1 Harness #1
Service Panel #1
Input Panel #1
C16 Harness

6.1.1.2 Model 334LS Cabinet

Model 334LS Cabinet shall consist of:

Housing 1 B
Mounting Cage 1
Input File I
Input Panel #3
PDA #3LX
C1 Harness #2
Service Panel #1

6.1.1.3 Model 336LS Cabinet

MODEL 336LS CABINET shall consist of:

Housing 2
Mounting Cage 2
PDA #2LS
Input File I
Output File #1LX
C1 Harness #3
Service Panel #2
Input Panel #4

6.1.1.4 Model 342LX Cabinet

Model 342LX Cabinet shall consist of Housing 3 and two ITS Mounting Cages.

First Mounting Cage shall consist of:

PDA #2LX
Input Files I & J
Output File #1LX
C1 Harness #1
Service Panel #1
Input Panel #1

C11 Harness
Output File #2LX (Model 520)
C16 Harness

Second Mounting Cage shall consist of:
(2) Blank Side Panels
Service / PDA Assembly
(2) Shelves

6.1.1.5 Model 344LS Cabinet

Model 344LS Cabinet shall consist of Housing 3 and two ITS Mounting Cages.

First Mounting Cage shall consist of:
Input File I
Input Panel #3
PDA Assembly #3LX
C1 Harness #2
Service Panel #1

Second Mounting Cage shall consist of:
(2) Blank Side Panels
Service / PDA Assembly
(2) Shelves

6.1.1.6 Model 346LX Cabinet

Model 346LX Cabinet shall consist of Housing 4 and two ITS Mounting Cages.

First Mounting Cage shall consist of:

PDA #2LS
Input Files I
Output File #1LX
C1 Harness #3
Service Panel #2
Input Panel #4

Second Mounting Cage shall consist of:
(2) Blank Side Panels
Service / PDA Assembly
(2) Shelves

6.1.1.7 Assemblies and Files

All assemblies and files shall be mounted on the cage mounting rails per cabinet model detail. Cabinet model interface wiring shall be per specified C1 Harness, detailed wiring lists and required One Line Wiring.

6.1.2 Cabinet Shipping Requirements

The cabinet shall be delivered mounted on a plyboard shipping pallet. The pallet shall be bolted to the cabinet base. The cabinet shall be enclosed in a slipcover cardboard packing shell. The housing doors shall be blocked to prevent movement during transportation.

6.1.3 Cabinet Adaptors
When specified, adaptors shall be provided. The adaptor shall be fabricated of the same material and finish as the cabinet housing.

6.1.4 Stainless Steel
All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

6.1.5 Cage Mounting
A cage mounting clear area for the controller unit shall be provided. The area shall extend 1.5 inches in front of and 16 inches behind the front EIA mounting angles.

6.1.6 Protection
All conductors, terminals and parts which could be hazardous to maintenance personnel shall be protected with suitable insulating material.

CHAPTER 6-SECTION 2
HOUSING REQUIREMENTS

6.2.1 Housing

The housing shall include, but not be limited to, the following:

Enclosure	Police Panel
Doors	Ventilation
Latches/Locks	Gasketing
Hinges and Door Catches	Cage Supports and Mounting

6.2.2 Housing Construction

6.2.2.1 Waterproof

The housing shall be rainproof with the top of the enclosure crowned to prevent standing water. It shall have single front and rear doors, each equipped with a lock.

6.2.2.2 Fabricating

The enclosure, doors, lifting eyes, gasket channels, police panel, and all supports welded to the enclosure and doors shall be fabricated of 0.125 in minimum thickness aluminum sheet. Bolted on supports shall be either the same material and thickness as the enclosure or 0.105 in minimum steel. The side panels and filter shell shall be fabricated of 0.125 in minimum thickness aluminum sheet.

6.2.2.3 Exterior

All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filed to a radius of 0.03125 in minimum. Exterior cabinet welds shall be done by gas Tungsten arc TIG process only. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum. Internal cabinet welds shall be done by either gas metal arc MIG or gas Tungsten arc TIG Process.

6.2.2.4 Aluminum surfaces

Aluminum surfaces shall conform to the following:

6.2.2.5 Powder Coating

The cabinets shall be Powder Coated with a coating that is at least 2 mils thick. The color shall be an Aluminum finish, Federal Standard 595C, # 17178.

6.2.2.6 Enclosure Doorframes

The enclosure doorframes shall be double flanged out on all 4 sides and shall have strikers to hold tension on and form a firm seal between the door gasketing and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 0.156 (+/- 0.08) in.

6.2.2.7 Gasketing

Gasketing shall be provided on all door openings and shall be dust tight. Gaskets shall be 0.25-inch minimum thickness closed cell neoprene or silicone (BOYD R-10480 or equal) and shall be permanently bonded to the metal. If neoprene is used the mating surface of the gasketing shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A Gasket Top Channel shall be provided to support the top gasket on the door (prevent gasket gravitational fatigue).

6.2.2.8 Cage Bottom Support Mounting Angles

The Model 332LS, 334LS & 336LS

Cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment; side cage supports shall be provided for the bracket cage supports; and bracket cage support attachments.

Model 342LX, 344LX and 346LX

Cage bottom supports shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness of either 0.188 in aluminum or 0.105 in steel.

6.2.2.9 Lifting Eyes

The housing shall be provided with 2 lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 0.75 in. Each eye shall be able to support a weight load of 1000 pounds.

6.2.2.10 Exterior Bolt Heads

All exterior bolt heads shall be tamperproof type.

6.2.3 Door Latches & Locks

6.2.3.1 Latching Handles

The latching handles shall have provision for padlocking in the closed position. Each handle shall be 0.75 in minimum diameter stainless steel with a minimum 0.5 in shank. The padlocking attachment shall be placed at 4.0 in from the handle shank center to clear the lock and key. An additional 4.0 in minimum gripping length shall be provided.

6.2.3.2 Latching Mechanism

The latching mechanism shall be a three-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 0.25 in thick by 0.75 in wide, minimum.

6.2.3.3 Locks and Handles for Model 332LS, 334LS and 336LS

When the door is closed and latched, the door shall be locked. The locks and handles shall be on the right side of the front door and left side of the rear door. The lock and lock support shall be rigidly mounted on the door. In the locked position, the bolt throw shall extend a minimum of

0.25 ± 0.03125 in into the latch Cam area. A seal shall be provided to prevent dust or water entry through the lock opening.

6.2.3.4 Locks
The locks shall be Corbin 2 type, or equal. Two keys shall be supplied with each cabinet. The keys shall be removable in the locked position only.

6.2.3.5 Bolts
The locks shall have rectangular, spring-loaded bolts. The bolts shall have a 0.281 in throw and shall be 0.75 in wide by 0.75 in thick (tolerance is ±0.035 in).

6.2.3.6 Center Latch Cam
The center latch cam shall be fabricated of a minimum thickness 0.1875 in steel or aluminum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.

6.2.3.7 Rollers
Rollers shall have a minimum diameter of 0.875 in with nylon wheels and steel ball bearings.

6.2.4 Ventilation
The housing ventilation including intake, exhaust, filtration, fan assembly and environmental control are as follows:

6.2.4.1 Front Door
The Model 332LS, 334LS and 336LS front door shall be provided with louvered vents. The louvered vent depth shall be a maximum of 0.25 in. A removable and reusable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 0.25 in to house the filter. The filter resident in its shell shall be held firmly in place with a bottom bracket and a spring-loaded upper clamp. No incoming air shall bypass the filter. The bottom filter bracket shall be formed into a waterproof sump with drain holes to the outside housing. The Model 342LX, 344LX and 346LX left front door and right rear door shall be provided with louver vents.

6.2.4.2 Intake and Exhaust Areas
The intake (including filter with shell) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for housing #1, 26 cubic feet of air per minute for housing #2 and 120 cubic feet of air per minute for housing #3.

6.2.4.3 Electric Fan
The Model 332LS, 334LS and 336LS housing shall be equipped with an AC powered electric fan with ball or roller bearings and a capacity of at least 100 cubic feet of free air delivery per minute. The fan shall be mounted within the housing and vented. The Model 342LX, 344LX and 346LX housing shall be equipped with four AC powered electric fans.

6.2.4.4 Temperature Controlling

Each fan shall be thermostatically controlled and shall be manually adjustable to turn on between 32 ^{0}F and 140 ^{0}F with a differential of not more than 20 ^{0}F between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor ampacity. The manual adjustment shall be graded in 20 ^{0}F increment scale. The Thermostat shall be an Omega KT01101141900 or equal.

6.2.4.5 Filter

The filter shall be 16 in wide by 12 in high by 0.875 in thick. The filter shall be an ECO-AIR Products E35S or equal.

6.2.5 Hinges & Door Catches

6.2.5.1 Leave Hinges

Two-bolt per leave hinges shall be provided to bolt the enclosure to the door. Housing 1B and 3 shall have 4 hinges and Housing 2 three hinges. Each hinge shall be 3.5 in minimum length and have a fixed pin. The pin ends shall be welded to the hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

6.2.5.2 Front and Rear Doors

Front and rear doors shall be provided with catches to hold the door open at both 90 and 180 ±10 degrees. The catch minimum diameter shall be either 0.375 in for plated steel or aluminum rods or 0.25 in for Stainless steel. The catches shall be capable of holding the door open at 90 degrees in a 60-mph wind acting at an angle perpendicular to the plane of the door.

6.2.6 Police Panel

6.2.6.1 Police Panel Assembly

A police panel assembly shall be provided to allow the police officers limited access to intersection control. The police panel assembly including switches shall not extend into the cabinet more than 2.5 in.

6.2.6.2 Police Panel Door

The police panel door shall be equipped with a lock. The lock shall be keyed for a master police key. One key shall be furnished with each police lock. Each police key shall have a shaft at least 1.75 inches in length.

6.2.6.3 Toggle Power Switches

The police panel shall contain 2 DPST Toggle Power Switches.

6.2.6.3.1 Model 334LS and 344LX

One switch shall be labeled "ON-OFF LIGHTS" and the other "POLICE CONTROL ON-OFF".

6.2.6.3.2 Models 332LS, 336LS, 342LX and 346LX

One switch shall be labeled “ON-OFF" and the other "FLASH/AUTOMATIC".

6.2.6.3.3 Front and Back of the Panel

The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

6.2.6.3.4 Panel Assembly

The panel assembly shall have a drain to prevent water collecting within the assembly. The drain shall be channeled to the outside.

CHAPTER 6-SECTION 3
CABINET CAGE REQUIREMENTS

6.3.1 EIA 19-inch Rack Cage
A standard EIA 19-in rack cage shall be installed inside the Model 332LS, 334LS, and 336LS housing for mounting of the controller unit and cabinet assemblies**.** Two standard EIA 19-in rack cages shall be installed inside the Model 342LX, 344LX and 346LX housing for mounting of the controller unit and cabinet assemblies**.**

6.3.2 EIA Cage Rack Portion
The EIA rack portion of the cage shall consist of 2 pairs of continuous, adjustable equipment mounting angles. The angles nominal thickness shall be either 0.1345 in plated steel or 0.105 Stainless Steel. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angles shall comply with Standard EIA RS-310-D and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.

6.3.3 Clearance
Clearance between rails for mounting assemblies shall be 17.75 in.

6.3.4 Angles
Two steel supporting angles extending from the front to the back rails shall be supplied to support the controller unit. The angles shall be designed to support a minimum of 50 pounds each. The horizontal side of each angle shall be a minimum of 3 in. The angles shall be vertically adjustable.

6.3.5 Cage
The cage shall be bolted to the cabinet at 4 points, via the housing cage supports and associated spacer brackets, 2 at the top and 2 at the bottom of the rails.

6.3.6 Cage Position
The cage(s) shall be centered within the cabinet(s).

CHAPTER 6-SECTION 4
CABINET ASSEMBLIES

6.4.1 General

6.4.1.1 Equipment
The following equipment shall be completely removable from the cabinet without removing any other equipment and using only a slotted or Phillips screwdriver:

Power Supply Assembly
Power Distribution Assembly
Input File
Output File
Monitor Unit Assembly

6.4.1.2 Fuses, Circuit Breakers, Switches and Indicators
All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

6.4.1.3 Equipment in the Cabinet
All equipment in the cabinet, when required shall be clearly and permanently labeled. The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed.

6.4.1.4 Resistor-Capacitor Transient Suppression
Resistor-capacitor transient suppression shall be provided at all AC relay sockets (across relay coil) except for the Flash Transfer Relays (FTR) in the output files where one suppression device may be common for all.

6.4.1.5 Leakage Resistor
A leakage resistor, which permits a small amount of current to pass through the heavy-duty relay coil, shall be installed across the terminals of a relay socket to overcome the residual magnetism.

6.4.1.6 Assembly
Assembly or file depth dimension shall include terminal blocks.

6.4.1.7 Air Circulation
All assemblies and files shall allow air circulation through its top and bottom unless specifically called out otherwise.

6.4.1.8 Socket Types
Socket types for the following equipment shall be

Switch Pack	BEAU S-5412-XX (or equal)
Heavy Duty Relay	BEAU S-5408-XX (or equal)
Flasher Unit & Power Sup Mod	BEAU S-5406-XX (or equal)
208 Monitor Unit	PCB 22/44S

6.4.1.9 Mounting

Connector sockets for Flasher Unit, Power Supply, and Switch Pack modules shall be mounted with their front face 7.5 in deep from assembly or file front panel (Note: Output File Exception).

6.4.1.10 Guides

Guides (Top and Bottom) shall be provided for Switch Pack Modules, Flasher Units, Monitor Unit, Watchdog Timer Module, Detector & Isolator Modules, and Power Supply Module (Bottom only). The guides shall begin 1.0±0.5 inches in from the front panel surface and extend to within 0.5 inches from the connector socket face.

6.4.1.11 Fabricating

Assemblies and Files shall be fabricated of 0.060 in minimum thickness aluminum or stainless-steel sheet. The metal surface shall be treated with clear chromate.

6.4.2 Power Supply Assembly

6.4.2.1 Power Supply

A power supply shall be provided to supply +24 VDC to the Input and Output Files for use by their associated devices. The power supply shall be compliant with Chapter 3, Section 4 under Model 206L Power Supply Unit of these specifications.

6.4.3 Power Distribution Assembly (PDA)

6.4.3.1 Equipment

The following equipment shall be provided with the power distribution assemblies:

6.4.3.1.1 PDA #2LX

1	-- Duplex NEMA 5-15R Controller Receptacle
2	-- Duplex NEMA 5-15R Equipment Receptacle (one with GFCI)
1	-- 1 Pole 15 Amperes minimum, 120 VAC Signal Bus Circuit Breaker
1	-- 1 Pole 15 Amperes minimum, 120 VAC Clean Power Circuit Breaker
6	-- 1 Pole Ganged, 10 Amperes, 120 VAC Signal Bus Circuit Breaker with Auxiliary Switch
1	-- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
1	-- 2 Pole Ganged, 10 Amperes, 120 VAC Flash Bus Circuit Breaker
1	-- Solid State Relay (Normally Closed) - rated minimum 50 Amperes, 120 VAC, Crydom A2450-B or equal.
2	-- Model 204 Flasher Unit and Socket
1	-- Model 206L/E Power Supply Module and Socket
1	-- AUTO/FLASH Control Switch
1	-- Flash On Indicator Light
3	-- 10 Position TBK T1, T2 & T4
1	-- 4 Position TBK T3

1 -- SSR Fault Indicator Light
1 --HI Health Indicator Relay
1 --K24 VDC Controlled Relay

6.4.3.1.2 PDA #2LS

1 -- Duplex NEMA 5-15R Controller Receptacle
2 -- Duplex NEMA 5-15R Equipment Receptacle (one with GFCI)
1 -- 1 Pole 15 Amperes minimum, 120 VAC Signal Bus Circuit Breaker
1 -- 1 Pole 15 Amperes minimum, 120 VAC Clean Power Circuit Breaker
6 -- 1 Pole Ganged, 10 Amperes, 120 VAC Signal Bus Circuit Breaker with Auxiliary Switch
1 -- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
1 -- 2 Pole Ganged, 10 Amperes, 120 VAC Flash Bus Circuit Breaker
1 -- Solid State Relay (Normally Closed) - rated minimum 50 Amperes, 120 VAC, Crydom A2450-B or equal.
2 -- Model 204 Flasher Unit and Socket
1 -- Model 206LS Power Supply Module and Socket
1 -- AUTO/FLASH Control Switch
1 -- Flash On Indicator Light
3 -- 10 Position TBK T1, T2 & T4
1 -- 4 Position TBK T3
1 -- SSR Fault Indicator Light
1 --HI Health Indicator Relay
1 --K24 VDC Controlled Relay

6.4.3.1.3 PDA #3LX

1 -- Duplex NEMA 5-15R Controller Receptacle
2 -- Duplex NEMA 5-15R Equipment Receptacle
1 -- 1 Pole 15 Amperes, 120 VAC Equip. Circuit Breaker
2 -- 1 Pole 10 Amperes, 120 VAC Field Circuit Breakers
1 -- 1 Pole 15 Amperes, 120 VAC Clean Power CB
1 -- Model 206L/E Power Supply Module and Socket
1 -- Model 208 Monitor Unit and Socket
1 -- Model 430 Heavy Duty Relay and Socket (Transfer Relay)
1 -- Watchdog Timer ON/OFF-RESET Control Switch
3 -- Model 200 Switch Pack Sockets
3 -- 10 Position TBK T1, T2 & T4
1 -- 4 Position TBK T3

6.4.3.2 Rating of Breakers

Rating of breakers shall be shown on face of breaker or handle. Breaker function shall be labeled below breakers on front panel.

6.4.3.3 Equipment Receptacle

The first equipment receptacle in the circuit shall have ground-fault circuit interruption as defined in the National Electrical Code. Circuit interruption shall occur on 6 mA of ground-fault current and shall not occur on less than 4 mA of ground-fault current.

6.4.3.4 AUTO/FLASH Switch

The AUTO/FLASH Switch when placed in FLASH position (down) shall energize the Solid-State Relay (SSR). When the switch is placed in the AUTO Position (up) the switch packs shall control the signal indications. The switch shall be a SPST Toggle Control Switch.

6.4.3.5 FLASH Indicator Light

The FLASH Indicator Light labeled "Flash On" shall be mounted on the PDA Front Panel. The lamp shall be driven by Flasher Unit/Output through Flash Relay Circuit No. 1 or per Circuit Breaker.

6.4.3.6 SSR Fault Indicator Light

The SSR Fault Indicator Light labeled “SSR Fault” shall be mounted on the PDA Front Panel. The lamp shall be driven by the SSR output when the Health Indicator Relay is energized.

6.4.3.7 Conductors

All conductors from the power distribution assembly routed to the cabinet wiring shall be connected to the terminal block on the common side, except for the AC power conductor between the service terminal block and main circuit breaker. All internal conductors terminating at the blocks shall be connected to the other side of the blocks.

6.4.3.8 Ganged Circuit Breakers

Ganged Circuit Breakers shall be certified by the circuit breaker manufacturer that their circuit breakers shall gang trip.

6.4.3.9 Monitor Unit

The Monitor Unit ON/OFF-RESET Switch shall be a DPST Toggle Control mounted on the PDA #3L's front panel. When placed in DOWN Position (OFF-RESET) a grounded input shall be presented at the Monitor Unit Pin 22 (resetting the WDT Circuitry) and the other side switch circuit closes by passing the Monitor Unit.

6.4.3.10 Circuit Breaker with Auxiliary Switch

6.4.3.10.1 Single Pole

Six Single Pole 10 Ampere Circuit Breakers with Auxiliary Switch Feature and Medium Trip Delay Characteristic shall be provided.

6.4.3.10.2 Breakers

The six breakers shall be wired and routed per the Option One Line Diagram. The breaker auxiliary switch circuit shall be open when the breaker is in ON Position. The auxiliary circuits shall be wired in parallel so that any tripped breaker shall energize the Solid-State Relay input,

Flash Transfer Relay Coils and the "FLASH ON" Indicator. The Auxiliary Contacts shall be rated at 5 Amperes, 120 VAC Minimum (fast on type connection).

6.4.3.10.3 Terminals
Breaker switches shall be bussed using straight solid non-insulated bus wire which is soldered directly to the “fast-on” terminals.

6.4.3.11 Model 206L/E/LS Power Supply Module

6.4.3.11.1 Requirements
The module shall meet the requirements specified in 6.4.2.1.

6.4.3.11.2 Module Chassis
The module chassis shall be vented. Its top and sides shall be open except for unit supports

6.4.3.11.3 PDA Assembly
When resident in the PDA assembly, the module shall be held firmly in place by its stud screw, assembly connector support panel and a wing nut.

6.4.3.11.4 Wire-Wound Power Resistors
Two 0.5 Ohm, 10-watt minimum wire-wound power resistors with a 0.2uH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three UL 1449 Varistors (MOVs), with a Nominal Discharge Current Rating (In) of 3kA shall be supplied between AC+ and EG, AC- and EG, and between AC+ and AC-. A 0.68uF capacitor shall be placed across AC+ and AC- between the two power resistors and the MOV's.

6.4.3.12 Terminal Screw Sizes
Terminal screw size shall be 10-32 for TBK T1, T2 & T4 and 6-32 for TBK T3.

6.4.4 Input File

6.4.4.1 Depth
The file shall have a maximum depth of 8.5 in and shall intermit with and support 14 two-channel detector sensor or isolator units.

6.4.4.2 Connectors
The file shall provide a PCB 22/44S connector centered vertically for each two-channel detector. The associated number and letter side connectors shall be shorted internally. Pins D, E, F, J, K, L and W shall be brought out to an 8-position terminal block on the back of the file. The output emitters shall be common grounded with the ground terminating at TB 15, Position 4. Position 8 of the terminal block is assigned to Equipment Ground and is used to terminate lead in shields.

6.4.4.3 Marker Strips
The input file shall be provided with marker strips to identify isolators and detectors in the file.

6.4.4.4 Screw Size
Terminal Block (TB) terminal screw size shall be 8-32.

6.4.5 Output File

6.4.5.1 General Requirements

6.4.5.1.1 Marker Strips
The Output File shall be provided with marker strips to identify switch packs when mounted in the file.

6.4.5.1.2 Connectors
Switch pack connectors, monitor unit connectors, flash transfer relay sockets and flash programming connectors shall be accessible from the back of the Output File without the use of tools or removal of any other equipment.

6.4.5.1.3 Terminal Positions
TBK O1 and O3 terminal positions shall be labeled functionally. A permanent label reading "Channels 9 & 10 Separated" placed on the right Output File mounting flange.

6.4.5.1.4 Field Wire
Field wire terminal blocks shall be mounted vertically on the back of the assembly. Output File #1 shall have 3 terminal blocks with 12 positions and Output File #2 shall have 3 terminal blocks with 6 positions. Terminal position screw size shall be 10-32.

6.4.5.1.5 Flash Transfer Relays
The Flash Transfer Relays shall be Heavy Duty Relay, Model 430. The coil of the relay shall be energized only when the signals are in flashing operation and the police panel ON/OFF switch is ON. The relay shall transfer the field outputs from switch pack output to flash control. The transfer shall not interrupt the controller unit operation.

6.4.5.1.6 Depth
The depth of the file shall not exceed 14.5 in.

6.4.5.1.7 Flash Programming Connectors
The flash programming connectors shall be Molex Type 1375 or equal. The receptacle shall be mounted on the file with a programmable plug connected. The plug connector, with programming jumpers, shall be furnished for each circuit to allow red or yellow flash programming. Plug pins shall be crimped and soldered.

6.4.5.1.8 TB O1, O2, O3 & O4 Terminal Screw Sizes
Terminal Block (TB) O1 and O3 terminal screw size shall be 8-32 and TBK O2 & O4 shall be 6-32.

6.4.5.2 Output File #1LX

6.4.5.2.1 Containing
The output file shall be capable of containing 12 Model 200 Switch Packs, 4 Flash Transfer Relays, and the Model 210 Monitor Unit. Four Flash Transfer Relays and 1 Model 210 Monitor Unit shall be furnished with each output file.

6.4.5.2.2 Output Circuits
The red and yellow output circuits of switch packs 1, 2, 3, 4, 5, 6, 7 and 8 shall be made available at individual pack Molex receptacle /plug connection for flash select-ability. Eight red & 4 yellow Molex Plugs shall be provided.

6.4.5.2.3 Model 210 Monitor Unit
It shall be possible to remove the Model 210 Monitor Unit without causing the intersection to go into flashing operation. The cabinet shall be wired so that with the front cabinet door closed and with the monitor unit removed, the intersection shall go into flashing operation (See One Line Diagram). The cabinet shall contain a conspicuous warning against operation with the Model 210 Monitor Unit removed.

6.4.5.2.4 Monitor Unit Compartment
The monitor unit compartment including the housed Model 210 Monitor Unit exclusive of handle shall extend no farther than 1.25 in front of the 19-in rack front surface. The switch pack socket connector front surface shall be no more than 8.5 inches in depth from the front surface of the output file.

6.4.5.3 Output File #2LX (Model 420)

6.4.5.3.1 Switch Packs and Flash Transfer Relays
The Output File #2LX shall be capable of containing 6 Model 200 Switch Packs and 2 Flash Transfer Relays. Two Flash Transfer Relays shall be provided with the file.

6.4.5.3.2 Output Circuits
The red and yellow output circuits of Switch Packs No. 1, 2, 4 and 5 shall be made available at a Molex receptacle/plug connection for flash select ability.

6.4.5.4 Output File #2LX (Model 520)

6.4.5.4.1 Switch Packs and Flash Transfer Relays
The Output File #2LX (Model 520) shall be capable of containing 5 Model 200 Switch Packs and 4 Transfer Relays. Four Flash Transfer Relays shall be provided with the file.

6.4.5.4.2 Output Circuits
Shall meet Section 6.4.5.3.2

6.4.6 Heavy Duty Relay (Model 430)

6.4.6.1 Electromechanical Type
Heavy duty relays shall be the electromechanical type designed for continuous duty.

6.4.6.2 Enclosing
Each relay shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating and part number shall be placed on the cover. They shall be permanent, durable and readily visible.

6.4.6.3 DPDT Contacts
Each relay shall be provided with DPDT contacts. Contact points shall be of fine silver, silver alloy or superior alternative material. Contact points and arms shall switch a 20 Amperes at 120 VAC tungsten load per contact once every 2 seconds with a 50% duty cycle for at least 250,000 operations without contact welding or excessive burning, pitting or cavitation.

6.4.6.4 Relay Coil
The relay coil shall have a power consumption of 10 Volt-Amperes maximum.

6.4.6.5 Potential & Surge Rating
Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a 1 cycle surge rating of 175 Amperes RMS.

6.4.7 Side Panels

6.4.7.1 Viewing
Two panels shall be provided and mounted on the cage parallel to the cabinet sides. In viewing from the back door, the left side panel shall be designated as the "Input Panel" and the right-side panel shall be designated as the "Service Panel".

6.4.8 Cabinet Harnesses
Harnesses shall meet the specifications as listed in Chapter 3 Section 7.

CHAPTER 6-SECTION 5
CABINET WIRING

6.5.1 Cabinet Wiring Diagram

6.5.1.1 Diagrams/Drawings Supply
Four sets of nonfading (comparable to Xerox 2080) cabinet wiring diagram and drawing sheets shall be supplied with each cabinet. The diagrams shall be nonproprietary. They shall identify all circuits in such a manner as to be readily interpreted. The cabinet drawing sheets shall show the equipment layout in an elevation view as viewed from the rear of the cabinet with the left and right cabinet walls shown in their relative positions.

The diagram and drawing sheets shall be placed in a heavy-duty side opening clear plastic pouch and attached to the front cabinet door.

6.5.1.2 Pouch
A pouch that would hold the Cabinet Manuals, Cabinet Wiring and Drawing Sheets, and Cabinet Keys shall be provided as part of the Cabinet.

The pouch shall be of such design and material that it provides adequate storage and access to the wiring diagram sheets and cabinet manuals. The pouch shall be of size and strength to easily hold the documents and keys without tearing.

6.5.1.3 Manuals
Two cabinet manuals shall be provided in the pouch together with the wiring diagram and drawing sheets.

6.5.2 Conductors

6.5.2.1 General
All conductors used in cabinet wiring shall terminate with properly sized non-insulated (if used, for DC Logic Only) or clear insulated spring-spade type terminals except when soldered to a through-panel solder lug on the rear side of the terminal block or as specified otherwise. All crimp-style connectors shall be applied with a power tool which prevents opening of the handles until the crimp is completed.

6.5.2.2 Sizes
Conductors between the service terminal AC- and Equipment Ground and their associated bus, the equipment ground bus conductor to Power Distribution Assembly and cage rail, AC- Bus to Power Distribution Assembly shall be No. 8 or larger.

6.5.2.3 Types
All conductors unless otherwise specified shall be No. 22, or larger, with a minimum of 19 copper strands. Conductors shall conform to Military Specification: MIL-W-16878D, Type B, or better. The insulation shall have a minimum thickness of 10 mils and shall be nylon jacketed polyvinyl

chloride except that Conductors No. 14 and larger may have Type THHN insulation (without Nylon Jacket), and shall be stranded with a minimum of 7 copper strands.

6.5.2.4 Labels

All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

6.5.2.5 Color-Code Requirements

All conductors shall conform to the following color-code requirements:

6.5.2.5.1 Grounded Conductors

The grounded conductors of AC circuits shall be identified by a solid white or solid gray color.

6.5.2.5.2 Equipment Grounding

The equipment grounding conductors shall be identified by a solid green color or by a continuous green color with 1 or more yellow stripes.

6.5.2.5.3 DC Logic Ground

The DC logic ground conductors shall be identified by a continuous white color with a red stripe.

6.5.2.5.4 Ungrounded AC+ Conductors

The ungrounded AC+ conductors shall be identified by a solid black or continuous black with colored stripe.

6.5.2.5.5 Logic Ungrounded Conductors

The logic ungrounded conductors shall be identified by any color not specified above.

6.5.2.6 DC Logic Ground and Equipment Ground

Within the cabinet, the DC logic ground and equipment ground shall be electrically isolated from the AC grounded conductor and each other by 500 Mega Ohms when tested at 250 VDC.

6.5.2.7 AC- Copper Terminal Bus

The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 0.25 in shall be used for securing the bus to the service panel.

6.5.2.8 Power Supply DC Ground

The cabinet power supply DC Ground shall be connected to the DC logic ground bus using a No. 14, or larger, stranded copper wire.

6.5.2.9 Input Terminal

Each detector lead-in pair, from the field terminals in the cabinet to the sensor unit rack connector, shall be a cable of UL Type 2092 or better. The stranded tinned copper drain wire shall be connected to a terminal on the input file terminal block. This input terminal shall be connected to the equipment grounding bus through a single conductor.

6.5.3 Terminal Blocks

6.5.3.1 Terminal Screws

The terminal blocks shall be barrier type rated at 20 Amperes, 600 volts RMS minimum. The terminal screws shall be 0.3125 in minimum length nickel plated brass binder head type with screw inserts of same material. Screw size is called out under associated cabinet assembly, file or side panel.

CHAPTER 6-SECTION 6
SERVICE PANEL ASSEMBLY

6.6.1 General Requirements
A Service Panel Assembly shall be provided. The assembly shall function as the entry point for AC Power to the cabinet including main and secondary circuit breakers, cabinet transient and voltage surge protection, clean power filtering, and Raw and Clean AC Power Sources.

6.6.2 Location
The assembly shall be located on the lower right Cage when viewed from the back door.

6.6.3 Service Terminal Block
The terminals of the Block shall be labeled AC+, AC-, AC+ In, AC+ Out and EQ GND and shall be covered with a clear insulating material to prevent inadvertent contact. The Terminating Lugs shall be large enough to accommodate # 2 conductors. An AWG #8 Jumper Conductor shall be provided between AC+ In and AC+ Out.

6.6.4 Surge Protector
The surge protector shall be the EDCO Model SHA-1250 ITS or equal.

6.6.4.1 Impulse Breakdown
Less than 1,000 volts in less than 0.1 us at 10 kilovolts/us.

6.6.4.2 Standby Current
Less than 1 mA AC.

6.6.4.3 Minimum Varistor Voltage
Greater than 212 VDC.

6.6.4.4 Ranges
Capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes

CHAPTER 6-SECTION 7
SERVICE POWER DISTRIBUTON ASSEMBLY

6.7.1 General Requirements
A Service Power Distribution Assembly (Service PDA) shall be provided. The assembly shall function as the entry point for AC Power to the LX cabinets including main and secondary circuit breakers, cabinet transient and voltage surge protection, clean power filtering, and Raw and Clean AC Power Sources.

6.7.2 Location
The Service PDA shall be located on the lower left rack when viewed from the back door.

6.7.3 Service Terminal Block
The terminals of the Block shall be labeled AC+, AC-, EQ GND, AC+, AC- and EQ GND and shall be covered with a clear insulating material to prevent inadvertent contact. The Terminating Lugs shall be large enough to accommodate # 2 conductors.

6.7.4 Surge Protector
The surge protector shall be the EDCO Model SHA-1250 ITS or equal.

6.7.4.1 Impulse Breakdown
Less than 1,000 volts in less than 0.1 us at 10 kilovolts/us.

6.7.4.2 Standby Current
Less than 1 mA.

6.7.4.3 Striking Voltage
Greater than 212 VDC.

6.7.4.4 Ranges
Capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes.

CHAPTER 6-SECTION 8
332LS, 334LS, 336LS, 342LX, 344LX & 346LX CABINET DETAILS

CHAPTER 7
REFER TO ATC CABINET STANDARD

CHAPTER 8
REFER TO MODEL 500 CHANGEABLE MESSAGE SIGN SPECIFICATIONS

CHAPTER 9
MODEL 2070 CONTROLLER SPECIFICATIONS

CHAPTER 9-SECTION 1
GENERAL

9.1.1 Controller Unit

The Controller Unit shall be composed of the Unit Chassis, modules and assemblies per their version. The following is a list of 2070 Versions, their interface rolls and composition:

UNIT VERSION	DESCRIPTION
2070LX+ UNIT	LX+ Unit mates to 170 & ATC cabinets. It consists of: 2070LX + UNIT CHASSIS, 2070-1C CPU, 2070-2E+ (2C+ if ATC Cabinet) FIO, 2070-3B+ FRONT PANEL, 2070-4 POWER SUPPLY, and Model 2070-LAN Module.
2070E UNIT	LITE Unit mates to the 170 & ATC cabinets. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2E+ (2C+ if ATC CABINET) FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY.
2070M UNIT	OS-9 Based IC Unit mates to 170 & ATC cabinets. It consists of: UNIT CHASSIS, 2070-1M CPU, 2070-2E+ (2C+ if ATC CABINET) FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY.
2070LX UNIT	LX Unit mates to the 170 & ATC cabinets. It consists of: UNIT CHASSIS, 2070-1C CPU, 2070-2E+ (2C+ if ATC CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY

Note: See Chapter 11 for 2070 NEMA Versions.

9.1.2 Communications and Option Modules

The communications and option modules shall be called out separately from the unit version. The composition weight shall not exceed 25 lbs.

9.1.3 Chassis

The Chassis top and Bottom Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel shall be made of minimum aluminum sheet. The Chassis Side panels shall be 0.090 inches minimum sheet.

9.1.4 Power Failure Power Restoration Operations

It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules shall comply to said operations.

9.1.5 2070 Unit Module

2070 UNIT module / assembly power limitations shall be as follows:

Models	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
2070-1E CPU	1.0 A	250 mA		
2070-1C or M CPU, Host Board	2A	250mA		
2070-2E+ FI/O	250 mA	750 mA	-----	-----
2070-2C+ FI/O	250 mA	500 mA	-----	-----
2070-3A, B&D FPA	500 mA	-----	50 mA	50 mA
2070-3A+, B+&D+ FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	500 mA	-----	50 mA	50 mA
2070-LX+ Unit Chassis/A6	2.0 A	250 mA	300 mA	
2070-LX+ Unit Chassis/A7	2.0 A	250 mA	300 mA	
2070-6A & Others	900mA	-----	300 mA	300 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA
2070-LAN	1A	-----	-----	-----

9.1.6 EIA-485 Communications Links

All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 Mbps. Isolation circuitry shall be by optical/digital isolator technologies.

9.1.7 EIA-485 Line Drivers/Receivers

The EIA-485 Line Drivers/Receivers shall be socket mounted or Surface mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

9.1.8 Sockets

Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9.1.9 Frame Address

SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

	SP 5	SP3
CPU 2070-1	“19"	“19”
FI/O 2070-2E+	"20"	“NA”
Manufacturer Use	128 -254	128-254

CPU Broadcast to all	"255"	“255”

All other addresses are reserved or assigned by the Agency with the exception of NEMA TS2 Type 1 Requirements (See Chapter 11). The SDLC response shall contain the frame address of the Command sender.

CHAPTER 9-SECTION 2
MODEL 2070-1 CPU MODULE

9.2.1 Model 2070-1M CPU Module
The Model 2070-1M CPU Module shall meet the specifications of a Model 2070-1C with exception that it shall host the OS-9 Operating System for Power PC.

9.2.2 Model 2070-1E CPU Module
The Model 2070-1E CPU Module shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the Motherboard Slot A5. The module shall meet all the requirements listed under this section and Chapter Details Section 7. The Model 2070-1E Module shall have a Motorola MC68EN360 CPU or equal, clocked at 24.576 MHz minimum.

9.2.2.1 Dual SCC Device
A Dual SCC Device (asynch/synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1 except where noted. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68EN360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements except where noted, including EIA 485 drivers / receivers and synchronous data rate of 153.3 Kbps.

9.2.2.2 68EN360 SCC1
The 68EN360 SCC1 shall be reassigned to Ethernet (ENET) Network meeting Ethernet 10 Mbps IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software. The CPU network lines shall be connected to a port on the Network Switch. Four LEDs labeled "10/100 and Link/Act" shall be mounted on the front panel signifying Ethernet operational conditions between the CPU and the Network Switch.

9.2.2.3 Module 2070 -1E Power Requirements.
The 2070-1E CPU Module shall not draw more than 1.00 A of +5VDC & 250 mA of ISO+12 VDC.

9.2.2.4 The C13S Connector
The C13S Connector shall be a DB25S connector and shall be located on the Module 2070 -1X CPU front panel and shall contain signals for SP8, LINESYNC, NRESET, POWERDOWN, and an isolated BIAS +5VDC as specified in the following subsections and as listed in A9-7. TX and RX LEDs shall be provided as show in A9-7.

9.2.2.4.1 Serial Port SP8
System Serial Port 8 (SP8) shall be isolated, converted to EIA-485, and then routed to Connector C13S. SP8 shall meet all SP2 Port requirements except where noted.

9.2.2.4.2 LINESYNC and POWERDOWN

LINESYNC and POWERDOWN lines shall each be isolated, converted to EIA-485, and then routed to connector C13S for external module use.

9.2.2.4.3 NRESET

CPU Reset and POWER UP lines shall be isolated, then OR'd to form NRESET. NRESET shall then be converted to EIA-485 and routed to connector C13S for external module use.

9.2.3 Model 2070-1C CPU Module

The TYPE 2070-1C CPU Module shall be a single board module meeting the 2X WIDE board requirements. The module shall be furnished normally resident in MOTHERBOARD Slot A5. The module shall meet the requirements as listed in Section 9.2.2.4 of these specifications.

9.2.3.1 Engine Board

The TYPE 2070-1C CPU shall use an Engine Board compliant to the AASHTO/ITE/NEMA Next Generation ATC Standard with the exceptions as defined in Sections 9.2.5 and 9.2.8. The Engine Board shall be used for execution of the application software. No other microprocessor or memory of the 2070-1C CPU shall be used for execution of the application software.

9.2.3.2 Ethernet Ports

The ETHERNET ports of the Engine Board shall be brought out on RJ 45 Connectors mounted on the 2070-1C front panel. The front panel LED indicators for the two CPU Ethernet ports shall be provided as indicated in drawing A9-15.

9.2.3.3 Network Switches, Module 2070-1C

The Model 2070-1C CPU Module shall be provided with two integrated Store-and-Forward Network Switches per the IEEE 802.3, 802.3u and 802.3 x specifications. One switch shall be configured with port 1 and 2 connected to the front panel RJ-45 connectors and port 3 shall be connected to the CPU ENET 1 port. The second switch shall be configured with port 1 connected to the front panel RJ-45, port 2 shall be connected to the CPU ENET 2 port. Port 3 shall be used to route Ethernet across the Motherboard to the "A" Connectors. DC Grounding plane around the network connectors and lines shall be provided. Port 3 Network Lines shall be assigned to: NetP5 TX+, TX-, RX+ and RX- respectively.

9.2.3.4 Universal Serial Bus (USB)

The TYPE 2070-1C CPU Module shall include a USB port compliant to the AASHTO/ITE Next Generation ATC Standard with the exceptions that USB shall conform to the appropriate sections of the USB v2.0 specification for both hardware and software operations. USB shall be brought out from the Engine Board to a USB Connector mounted on the 2070-1C front panel.

9.2.3.5 Host Module

The 2070-1C CPU Module shall use a Host Module that provides the mechanical and electrical interfaces to the Engine Board and Motherboard.

The TYPE 2070-1C CPU Module shall implement the host module identification using the Engine Board SPI serial port, compliant to the AASHTO/ITE Next Generation ATC Standard.

9.2.3.6 Firmware Updates

Circuitry shall be included in the 2070 Unit that provides a bi-directional, asynchronous serial communications path from the CPU Module to microcontroller(s) in the Field I/O, Front Panel. Firmware shall be included on the main processor of the CPU Module, and all microcontrollers, that facilitates in-field firmware updates. As a minimum, the Field I/O processor and Front Panel processor shall be upgradeable via communications from the CPU Module.

The Field I/O processor shall use SP5 for the firmware upgrade path.

The Front Panel processor shall use SP6 for the firmware upgrade path.

9.2.4 Model 2070-1E CPU Module

9.2.4.1 Contiguous Addresses

16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's Supplied File Manager.

9.2.4.2 Incoming +5 VDC

When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. An on-board circuit shall sense the +5 VDC Standby Power and shift to an On-board CPU Power Source. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

9.2.4.3 Ram Memory

A minimum of 32 MB of DRAM/pseudo SRAM memory, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM will be available for agency use, organized in 16 or 32-bit words shall be provided. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

9.2.4.4 Flash Memory

A minimum of 8 MB of FLASH memory, organized in 16- or 32- bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 2 MB of FLASH Memory shall be used for the Boot Image and a minimum of 6 MB shall be available for Agency use. A maximum of 2 MB of Flash Memory shall be reserved the Boot Image only. Flash memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better."

9.2.4.5 Time-of-day Clock

A software settable hardware Time-of-Day (TOD) clock shall be provided. It shall, under on-board standby power maintain an accuracy of ±1 minute per 30 days at 25°C. The clock shall provide a minimum fractional second resolution of 10 ms and shall track seconds, minutes, and hours, day of month, month, and year.

9.2.4.6 CPU_Reset

A software-driven CPU_Reset signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be a driver capable of sinking 30 mA at 30 VDC. Execution of the program module "cpureset" in the boot image shall assert the CPU_Reset signal once. CPU_Reset shall be executed when the controller starts up or is rebooted using the OS-9 break command. The assertion of the CPU_Reset signal shall cause the FCU firmware to reset. The FCU shall become operational and respond to the Modules Status Request with the P bit set, within 33ms after a firmware reset. The cpureset shall be executed when the controller starts up or is rebooted using the OS-9 break command.

9.2.4.7 CPU_ACTIVE LED Indicator

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED Indicator. The LED shall default to ON when the controller starts up.

9.2.4.8 Tick Timer

The OS-9 Operating System Tick Timer interrupt shall be derived from each transition of LINESYNC signal, with a tick rate of 120 ticks per second.

9.2.4.9 SRAM and TOD Clock

The SRAM and TOD Clock Circuitry under Standby mode shall draw no more than 8uA at 2.5 VDC and 35 degrees C. An On Board Capacitor supply shall hold up SRAM and TOD for a minimum of 7 days.

9.2.4.10 Network Switch, Model 2070 -1E

The Model 2070-1E CPU Module shall be provided with an integrated Store-and-Forward Network Switch per the IEEE 802.3, 802.3u and 802.3 x specifications.

The switch shall be configured with two ports connected to the front panel RJ-45 connectors (C14S) and a third port shall be connected to the CPU. A fourth Port on the Network Switch shall be used to route, via magnetics, Ethernet across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively.

9.2.5 Model 2070-1C CPU Engine Board

9.2.5.1 Model 2070-1C CPU Module Processor

The Model 2070-1C CPU Module Processor shall utilize an NXP series MPC 82xx / 83xx /85xx or QorIQ with a minimum MIPS of 400 calculated using the Dhrystone v2.1 benchmark at 25°C. The CPU shall provide support for all single or double-precision floating-point operations.

9.2.5.2 Ram Memory (DRAM)
The Model 2070-1C CPU Module shall contain a minimum of 64Mbytes of DRAM or equivalent volatile memory for application and OS program execution.

9.2.5.3 Flash Memory
The Model 2070-1C CPU Module shall contain a minimum of 32Mbytes of FLASH for storage of OS Software and user application.

9.2.5.4 Static Memory (SRAM)
The Model 2070-1C CPU Module shall contain a minimum of 1MB minimum of SRAM memory for non-volatile parameter storage.

9.2.5.5 Standby Power
The Model 2070-1C CPU Module Engine Board shall provide the Standby Power required for supporting the SRAM and RTC.

9.2.5.6 Real-Time Clock (RTC)
The Model 2070 -1C Module shall be provided with a software settable, hardware RTC that meets the requirements of the ASHTO/ITE/NEMA ATC Standard except that in the absence of VPRIMARY, the RTC shall operate from VSTANDBY as listed in A9-16 of these specifications. Also Operating System Time shall be maintained by utilizing the RTC and LINESYNC as defined in Section 9.5.5.3.

9.2.5.7 CPU_Reset
A software-driven CPU_Reset Signal (Active Low) shall be provided to reset other system devices and shall be accessible by application programs as well as by the command line as “cpureset”. CPU_Reset shall be executed when the Controller starts up or is rebooted using the reboot command.

9.2.5.8 CPU_ACTIVE
An Active Low signal shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED indicator. This signal shall cause to the LED to default to ON when the controller starts up.

9.2.5.9 Application Program Interface (API)
An optional installed copy of the Application Program Interface (API) compliant to the latest ASHTO/ITE ATC API Standard shall be provided upon request.

9.2.5.10 Integrated Security
The Model 2070-1C Module shall be implemented with integrated security support for the AES encryption algorithm as well as a public key accelerator and an on-chip random number generator.

9.2.5.11 SD Card Support
The Model 2070-1C
Module shall support SD Card Memory and shall be provided with an industry standard SD Card socket.

9.2.6 Data Key

A Datakey Keyceptacle™ (KC4210, KC4210PCB or equal) shall be mounted on the CPU module front panel (or the Transition Board of MODEL 1A). Power shall not be applied to the receptacle if the key is not present.

The contractor shall supply an 8Mb Memory Size Datakey (SFK8Mb or equal) with each MODEL 1A TB (Transition Board) or 1E and 1C CPU module unless specified otherwise. The Datakey shall be temperature rated for –40 °C to +85 °C (–40°F to 185 °F) operation, shall be blue in color, and shall be initialized to the format and default values defined below. External capability to program the CPU Datakey shall be provided by the contractor.

When programmed, the memory on the key of header shall be organized as follows:

Bytes	Description	Default Values
1-2	16-bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64	
3	Key Type	See table below
4	Header Version	2
5-8	Latitude	0.0
9-12	Longitude	0.0
13-14	Controller ID	0xFFFF
15-16	Communication drop number	0xFFFF
17-20	IP Address	10.20.70.51
21-24	Subnet Mask	255.255.255.0
25-28	Default Gateway	10.20.70.254
29	Startup Override	0xFF
30-64	Reserved for Agency use	All bytes set to 0xFF
65 to End	User Data	All bytes set to 0xFF

When programmed, Byte 3 of the header shall contain the Key Type value as defined in the following table:

Key Type	Model No.	Memory Size	Sector Size	Part Number
1.	DK1000	1Kb	2 Byte	611-0006-002A
2.	LCK16000	16Kb	2 Byte	611-0070-008A
3.	SFK2Mb	2Mb	64KBytes	611-0089-004A
4.	SFK4Mb	4Mb	64KBytes	611-0104-002A
5.	SFK8Mb	8Mb	64KBytes	611-0132-006A
6.	SFK32Mb	32Mb	64KBytes	611-0164-005A

The data format in the CPU Datakey header for the Latitude and Longitude fields shall comply with IEEE/ANSI 754-1985 STD. All the other fields shall follow a Big-Endian Format as implemented by Motorola CPUs.

The Startup Override byte, not the Key Type, may be used to override the default controller startup procedure, as described in section 9.2.7.3.3.

9.2.7 Model 2070-1E CPU Module Software

The following shall be supplied:

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Deliverables
5. Error Handler

9.2.7.1 Operating System

The CPU Module shall be supplied with Microware Embedded OS-9 Release 4.02 or later with kernel edition #384 or later and CSL edition 29 or later. The following modules shall be included:

1 Embedded OS-9 Real Time Kernel
2 Sequential Character File Manager (SCF)
3 Stacked Protocol File Manager (SPF)
4 Pipe File Manager (PIPEMAN)
5 Random Block File Manager (RBF)
6 C Shared Library (CSL)

Boot Image shall include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Format	Dcheck	Login	Link	Kermit
Tsmon	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime	Merge	Grep	Mat
Tee	Printenv	Chown	Cudo	Mkdatmod	

The Boot Image with the above utilities and including the network driver and descriptor shall be loaded into RAM as part of OS-9 initialization as defined in Section 9.2.7.3.2.

9.2.7.2 Drivers and Descriptors

9.2.7.2.1 Supplied Modules

Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

Device drivers which require extensions to the standard Microware libraries shall use the _os_getstat() and _os_setstat() functions.

A custom setstat code and parameter structure are defined as follows:

```
#define SS_2070      0x2070

error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);

error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);
```

```
typedef struct
{
    u_int32 code;
    u_int32 param1;

    union
    {
       u_int32 param;
       void  *pointer;

    } param2;
} PB2070, *pb;
```

The following subcodes for use with PB2070.code are also defined:

```
#define GS2070_Status          0x1C
#define SS2070_SSig            0x1A
#define SS2070_IFC             0x22
#define SS2070_OFC             0x23
#define SS2070_Timer_Null      0x0000    (Default State)
#define SS2070_Timer_Sig       0x1000
#define SS2070_Timer_Cyc       0x1001
#define SS2070_Timer_Start     0x1002
#define SS2070_Timer_Stop      0x1003
#define SS2070_Timer_Reset     0x1004
```

Note: When PB2070.param2.pointer is used, PB2070.param1 should be loaded with the size of what PB2070.param2.pointer is referencing. When calling _os_getstat() or _os_setstat(), all reserved or unused parameters and fields in PB2070 should be loaded with 0 (zero).

9.2.7.2.2 Memory Drivers

Drivers shall be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors shall apply:

/f0	FLASH drive	non-volatile, writeable
/dd	FLASH drive	OS-9 default device for /f0
/f0wp	FLASH Drive	as /f0 except write protected
/f0fmt	FLASH Drive	as /f0 except format enabled
/r0	SRAM Drive	non-volatile ramdisk
/r0fmt	SRAM Drive	as /r0 except format enabled
/r2	DRAM Drive	volatile 2 MB ramdisk, not automatically initialized
/r4	DRAM Drive	volatile 4 MB ramdisk, not automatically initialized
/r8	DRAM Drive	volatile 8 MB ramdisk, not automatically initialized

9.2.7.2.3 MC68360 Internal Timers

A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Timer resolution shall be one count equals 100 μS and all timer periods shall be specified in units of hundreds of microseconds (μS).

A signal of "0" shall be an invalid signal and the driver shall return an E$PARAM error if received.

Access to the MC68360 internal timers shall be through the descriptors as listed under Descriptors.

The timers should be set to SS2070_Timer_Null Mode upon initialization.

9.2.7.2.3.1 Descriptor

Descriptor names for each timer:

timer1	= access to MC68360's internal timer #1
timer2	= access to MC68360's internal timer #2
timer3	= access to MC68360's internal timer #3
timer4	= access to MC68360's internal timer #4
timer12	= access to MC68360's internal timer #1 & #2 [cascaded]
timer34	= access to MC68360's internal timer #3 & #4 [cascaded]

9.2.7.2.3.2 Timer Standard

Timer Standard OS-9 Function Calls:

```
error_code _os_open (char *timer_desc_name, path_id *path);
error_code _os_read (path_id path, void *timer_value, u_int32 *size);
```

Note: Prior to calling _os_read(), size must be loaded with the value 4 and timer value must be pointed to a u_int32. _os_read() shall read the current timer value and load it into timer_value as μS x 100.

```
error_code _os_close (path_id path);
```

9.2.7.2.3.3 Time Extension

Timer Extension to Standard OS-9 Function Calls:

The timer drivers shall support the following modes using the following function with the SS_2070 option code and a custom parameter block structure:

```
error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);
```

a. Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal. After one-shot signal is sent, timer shall stop (SS2070_Timer_Stop).

```
pb→   code = SS2070_Timer_Sig;          /* request for one-shot signal */
pb→   param1= signal;
pb→   param2.param = period;
```

b. Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal.

```
pb→   code = SS2070_Timer_Cyc (0x1001);   /* request for periodic signal */
pb→   param1 = signal;
pb→   param2.param = period;
```

c. Start timer. Starts the timer if stopped or null. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period. Timer will not send a signal and any pending signals will be cancelled.

```
pb→     code = SS2070_Timer_Start;              /* start timer if stopped */
```

d. Stop timer. Leaves current value in timer. Cancels any pending signals.

```
pb→     code = SS2070_Timer_Stop;               /* stop timer if running */
```

e. Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals.

```
pb→     code = SS2070_Timer_Reset;              /* reset timer (stop and zero) */
```

9.2.7.2.3.4 Timer Extension

Timer Extension to Standard OS-9 Function Calls:
The timer driver shall support the following function with the SS_2070 option code and custom parameter block structure:

```
error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);
```

Retrieve current timer configuration.

```
typedef struct
{
        u_int32 value;
        u_int32 mode;
        u_int32 signal;
        u_int32 period;
} Timer_status;
pb→     code = GS2070_Status (0x1C)     /* Request timer status data */
pb→     param1 = sizeof(Timer_status)
pb→     param2.pointer = &Timer_status *
```

Status data shall be returned in the structure pointed to by pb→param2.pointer as follows:

```
pb→   param2.pointer→value    /* current timer value in µS x 100 */
pb→   param2.pointer→mode     /* SS2070_Timer_Sig if one-shot signal pending,
                                 SS2070_Timer_Cyc if periodic signal pending,
                                 SS2070_Timer_Start if free running,
                                 SS2070_Timer_Stop if not active
                                 SS2070_Timer_Reset if timer is reset
                                 SS2070_Timer_Null when timer is first
                                 initialized */

pb→   param2.pointer→signal   /* signal code pending if
                                 SS2070_Timer_Sig or
                                 SS2070_Timer_Cyc, 0 otherwise */
pb→   param2.pointer→period   /* timer period in µS x 100 if
                                 SS2070_Timer_Sig or
```

SS2070_Timer_Cyc and
Maximum Timer Period if
SS2070_Timer_Start
, 0 otherwise */

The following values shall be returned when the timer is in the SS2070_Timer_Null (Timer initialized) Mode:

Timer Mode = SS2070_Timer_Null
Timer Value = 0
Timer Period = 0
Timer Signal = 0

The following values shall be returned when the timer is in the SS2070_Timer_Start Mode:

Timer Mode = SS2070_Timer_Start
Timer Value = Running Timer Value
Timer Period = Maximum Timer Period
Timer Signal = 0

The following values shall be returned when the timer is in the SS2070_Timer_Stop Mode:

Timer Mode = SS2070_Timer_Stop
Timer Value = Current Timer Value
Timer Period = 0
Timer Signal = 0

The following values shall be returned when the timer is in the SS2070_Timer_Reset Mode:

Timer Mode = SS2070_Timer_Reset
Timer Value = 0
Timer Period = 0
Timer Signal = 0

9.2.7.2.3.5 Timer Period

All timer periods are specified in units of hundreds of microseconds (μS), i.e. a timer period of 7 = 700μS. The minimum allowed timer period shall be 500μS. The maximum timer period for timers 1-4 shall be 6.5535 seconds (0xFFFF). The maximum timer period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF). The driver shall return error E$Param from _os_setstat() if the requested timer period is outside the allowable range.

9.2.7.2.4 CPU Datakey

Access and control to the CPU Datakey shall be provided through the following descriptor name and OS-9 functions:

Descriptor name:
datakey = access to the CPU Datakey

Function Calls:

error_code = _os_open (char *datakey_desc_name, path_id *path);

error_code = _os_close (path_id path);

error_code = _os_read (path_id path, void *data_buffer, u_int32 *data_size);

error_code = _os_write (path_id path, void *control, u_int32 *data_size);

error_code = _os_seek(path_id path, u_int32 *position); sets read / write offset

error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); erases sector(s) if pointer is on a block boundary, returns E$PARAM error if not on a boundary */

error_code = _os_gs_pos(path_id path, u_int32 *position); /* gets current file pointer position */

error_code = _os_gs_size(path_id path, u_int32 *size); /* gets current datakey size */

Error codes returned by Function calls:

E$NotRdy if datakey is not inserted
E$Seek if Offset plus *data_size is beyond end of CPU Datakey.
E$EOF if upon read or write, the last byte of CPU Datakey has previously been processed.
Note: Use of SCF to implement the datakey driver is not allowed.

9.2.7.2.5 Flow Control Modes

The asynchronous serial communications device drivers shall support the six flow control modes (FCM#) described below:

FCM#	Description

1. No Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed. This is the default mode. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode (FCM# 1).
2. Manual Flow Control Mode: The driver transmits data regardless of the state of CTS. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
3. Auto-CTS Flow Control Mode: The driver transmits data only when CTS is externally asserted. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
4. Auto-RTS Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If the user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
5. Fully Automatic Flow Control Mode: The driver transmits data only when CTS is externally asserted. Upon a write command, the driver asserts RTS and waits for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
6. Dynamic Flow Control Mode: The driver transmits data only when CTS is externally asserted. The driver controls RTS based on the status of its receiving buffer. The driver asserts RTS continuously as long as its receiving buffer has sufficient capacity to store incoming data. If the receiving buffer approaches full, the driver de-asserts RTS until enough data has been read from the buffer to create sufficient receive capacity.

9.2.7.2.5.1 Serial Device Driver

The serial device driver shall be able to set user options via _os_setstat() and return status via _os_getstat(). To support legacy application programs, the device driver shall also be able to set user options via _os_ss_size() and to return status via _os_gs_size():

```
error_code_os_setstat(path_id path, SS_2070, void *pb);
error_code_os_getstat(path_id path, SS_2070, void *pb);
error_code_os_ss_size(path_id path, u_int32 size);
error_code_os_gs_size(path_id path, u_int32 *size);
```

Note: The preferred method of accessing serial device drivers is through _os_setstat() and _os_getstat(). The _os_ss_size() and _os_gs_size() interface may not be required by future versions of this specification and is therefore not recommended for new development.

The option subcodes to be passed in pb→code and the data to be contained in pb→param1 are defined as follows. pb→param2 is unused here and should be set to 0 (zero). For _os_ss_size() and _os_gs_size(), the size argument is the same format as pb→param1.

9.2.7.2.5.2 Supported Setstat

The supported _os_setstat() / _os_ss_size() options shall be as follows.

a. **Subcode passed in pb→code is SS2070_OFC (0x23).**

Data passed in pb→param1 is defined as follows:

Bits	Description
31-24	Auto RTS turn-off extension in number of characters (range:0-255, 0=default).
23-14	Reserved for future use.
13	Inhibit return of error E$Write from _os_write() when transmit buffer full in FCM# 2, 4, 5 (default=0, 0=error, 1=block)
12	Inhibit variable SCC MRBLR (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range:0-5).
7-0	Subcode SS2070_OFC (0x23).

Variable MRBLR (68360 SCC)

To reduce the IRQ handler overhead, the 68360 SCC driver shall use variable MRBLR as follows. If SS2070_OFC bit 12 is set to 1, the MRBLR shall be fixed at 16 for all baud rates. Variable MRBLR is not required for SP1 or SP8 on the 2070-1B CPU Module.

Baud Rate	MRBLR Setting
1200	1
2400	2
4800	4
9600	8
19200 & Higher	16

TODR (68360 SCC)

TODR requests processing a new TX buffer immediately. To reduce impact on other serial channel operations, SS2070_OFC bit 11 may be set to 1 to prevent assertion of TODR. TODR is not required for SP1 or SP8 on the 2070-1B CPU Module.

b. Subcode passed in pb→code is SS2070_IFC (0x22).
Data passed in pb→param1 is defined as follows:

Bits	Description
31-11	Reserved for Future Use.
10	DCD must be asserted to receive data (default=0; 0=NO; 1=YES).
9-8	Reserved for Future Use.
7-0	Subcode = SS2070_IFC (0x22).

c. **Subcode passed in pb→code is SS2070_SSig (0x1A).**

1. If CTS is currently negated and bits 16-31 are not all 0:
   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.
   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.
2. If CTS is currently asserted and bits 16-31 are not all 0:
   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal immediately.
   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot as soon as CTS is negated.
3. If both bits 11 and 12 of the SS2070_SSig parameter block are set, and bits 16-31 are not all 0:
   The controller will send a one-shot signal upon the next change of CTS state

Data passed in pb→param1 is defined as follows:

Bits	Description
31-16	A signal number to be sent to calling process when the state of an input changes.
15-13	Reserved for Future Use.
12	Send signal when CTS is de-asserted.
11	Send signal when CTS is asserted.
10-8	Reserved for Future Use.
7-0	Subcode = SS2070_SSig (0x1A).

9.2.7.2.5.3 Supported Getstat

The supported _os_getstat()_ / _os_gs_size() options shall be as follows.

a. **Subcode passed in pb→code is GS2070_Status (0x1C).**
   Data returned in pb→param1 is defined as follows:

Bits	Description
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use.

10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Use.
6	Overrun error –0=no error; 1=error has occur since last GS2070_Status call.
5	Frame error –0=no error; 1=error has occurred since last GS2070_Status call.
4	Parity error –0=no error; 1=error has occurred since last GS2070_Status call.
3-2	Reserved for Future Use.
1	DCD state –0=de-asserted; 1=asserted.
0	CTS state –0=de-asserted; 1=asserted.

9.2.7.2.6 Device Drivers Compliant

Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator

dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

error_code _os_open (char *desc_name, path_id //open descriptor for command *path);

error_code _os_close (path_id path); //close descriptor

error_code _os_write (path_id path, void *value, u_int32 //set value of function *data_size);

*value = 1, turn on LED or enable DST correction (default)

*value = 0, turn off LED or disable DST correction set u_int32*data_size to 1

error_code _os_read (path_id path, void *value, u_int32 //get current state set *data_size); u_int32*data_size to 1

9.2.7.2.7 Manufacturer Support

The manufacturer shall provide the following features to support the TOD operation and synchronization.

9.2.7.2.7.1 Leap Year and Daylight Savings Time

Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years.

9.2.7.2.7.2 Setting Hardware Clock

Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

9.2.7.2.7.3 Setting OS-9 System Clock

Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall be synchronized to a minimum of 10 ms resolution.

9.2.7.2.8 Flash Ram Drive

The FLASH drive shall be protected from corruption. It shall be protected using the Write Protect (WP) bit of the Base Register. When writing to the FLASH drive the current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy.

A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds.

9.2.7.3 OS-9 Application Kernel

9.2.7.3.1 Boot Sysreset

The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the default parameters as listed in A9-16.

9.2.7.3.2 Hardware Initialization

Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test) and forking OPEXEC shall be completed in less than 4 seconds. This startup time shall be measured from the release of SYSRESET to the turn on of the CPU_ACTIVE LED using a user level program named ONLED. The ONLED program shall be the last module loaded into RAM and executed using opexec or a startup file.

9.2.7.3.3 Startup Procedure

The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo shall operate as follows:

1. Sysgo shall set the execution directory to /f0wp/CMDS
2. Sysgo shall check if the backspace key (0x08) is being received on /sp4 (c50j). If received, Sysgo shall:
    a. Fork a shell with no arguments on /sp4 using the current directory.
    b. Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo shall fork another shell with no arguments on /sp4. Unless Sysgo dies, a shell shall always be provided on /sp4.

3. If the backspace key was not received, Sysgo shall check for the presence of a Datakey. If present and valid (Datakey Header Version 2 or greater), Sysgo shall check the Startup Override Byte in the Datakey header.

   If Startup Override is 0x01, Sysgo shall:

   a. Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header shall be the size of the script in bytes. The script shall immediately follow the length value, and shall be stored as ASCII text.

   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

   If Startup Override is 0x02, Sysgo shall:

   a. Fork an executable module stored on the Datakey immediately following the header.

   b. If there is any error loading or forking the module, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking the module, Sysgo shall then exit without forking a shell.

4. If the backspace key was not received and Startup Override Byte is 0xFF:

   a. Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.

   b. If there is any error loading or forking OPEXEC, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking OPEXEC, Sysgo shall then exit without forking a shell.

5. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC file:

   a. Sysgo shall fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.

   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

6. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC and no startup file:

   a. Sysgo shall fork a shell as described in step 2.

9.2.7.3.4 Short Out

A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. ACFAIL/POWER DOWN transitions shall generate an interrupt. The interrupt shall update an OS-9 event named "ACFAIL". The "ACFAIL" event shall set a value 1 indicating an ACFAIL condition occurred for the DOWN transition and set 0 indicating non-ACFAIL condition for the HIGH transition. The IRQ7 and auto-vector 31(7) shall not be used to update the "ACFAIL" event.

In addition, the ACFAIL condition shall generate the OS-9 auto-vector 30(6) interrupt service. Each interrupt service installed shall exit with the "Carry Bit" set allow OS9 to propagate the ACFAIL interrupt. The Contractor shall supply an interrupt handler at priority 255 that acknowledges and clears the interrupt.

Priority 1 shall be reserved for the OS-9 system.

9.2.7.3.5 Long Out

A Long Out is defined as ACFAIL transitions to LOW follow by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

9.2.7.4 Error Handler

9.2.7.4.1 Initialization and Power-Up Test

A manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions. If used, the error report shall be stored in the file /r0/ErrorReport and shall not exceed 11kb in size.

9.2.7.5 Network Requirements

On the MODEL 2070-1E CPU module, an OS-9 SPF Ethernet hardware driver and descriptor for the 68360 (SCC1) shall be provided in the operating system Boot Image. The descriptor shall be named spqe0.

9.2.7.5.1 BOOTOBJS

The following OS-9 modules should be included in the /f0/CMDS/BOOTOBJS flash disk directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links:

1. Drivers and Descriptors for PPP.
2. Drivers and Descriptors for SLIP.
3. LAN Comm Pak modules: spenet, enet, spip, ip4_timeslice, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0, spipcp, ipcp0, splcp, lcp0, sphdlc, hdlc0, spslip, sps10
4. Network modules pkman, pkdvr, pk, pks
5. Network Trap Handler: netdb_local, netdb_dns
6. NFS Modules: nfs, nfsnul and nfs_devices.

The PPP and SLIP descriptors shall have baud rates and ports set as follows and be stored in the /f0/CMDS/BOOTOBJS directory,

hdlc0 and spsl0 configured to use /sp1 and 38400 bps

hdlc1 and spsl1 configured to use /sp2 and 115200 bps

hdlc2 and spsl2 configured to use /sp3 and 115200 bps

hdlc3 and spsl3 configured to use /sp4 and 38400 bps

9.2.7.5.2 CMDS

The following Network utilities shall be included and shall reside in the /f0/CMDS directory as identified in this specification.

arp, dhcp, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, nfsd, mountd, and showmount, sshd, sshkeygen, sftp, sftpserver,openssl, scp, passutil, useradd, userdel, usermod.

9.2.7.5.3 Multi-user functionality

The boot image init module shall be configured with a "default directory name" as /f0wp. This will allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session.

The login and tsmon OS-9 modules should be included in the operating system boot image for the implementation of multi-user mode. A ".login" file with an entry of date shall be included in the /f0 directory. The attributes of the .login file shall be set using the command "attr –pwprwr .login "and the ownership shall be set to group.user ID of "0.0"

The following startup file shall be provided resident in the /f0 directory. The startup file shall have the ownership group.user ID of "20.70".

Include the following startup file:

```
*
*-t -np
*
* Startup File
*/f0wp/sys/startspf
*/f0wp/sys/startnfs
ex tsmon /sp4
*
*
```

9.2.7.5.4 Network Configuration

The modules inetdb, inetdb2 and rpcdb shall be generated by the make utility via the use of a makefile and the network configuration files residing the /f0/ETC directory. The generated inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The modules shall be configured with the network default values as defined in Section 9.2.6 (Data Key) via the

interfaces.conf shell script. The modules shall be configured with the network default values as defined in Section 9.2.6 (Data Key) or via the interfaces.conf shell script and all services shall be comment out in the Internet Daemon Services List inetd.conf located in the /f0/ETC directory.

9.2.7.5.5 Netcfg

A Utility Program named netcfg shall be provided that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid **(Datakey Header Version 2 or greater),**, netcfg shall set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line. The netcfg utility shall create a new inetdb, inetdb2 and rpcdb database module based on the Datakey network parameters or network parameters from the command line. The new inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The netcfg shall also allow the user to read, write and display network parameters to and from the Datakey via the command line prompt. If the Datakey is not present or invalid and the flag option is not "n" netcfg shall display an error and exit without altering the network configuration. The netcfg utility shall reside in /f0/CMDS.

Netcfg options:

a= Write IP Address in Datakey
m= Write Netmask Address in Datakey
g= Write Gateway Address in Datakey

If the checksum is incorrect when executing the –a, -m or –g option the following will occur:

1. The default Datakey data will be loaded.
2. The networking changes will be made to the default networking parameters.
3. The CRC will be recalculated.
4. The networking parameters will be written to the Datakey.

This option loads default networking parameters into the Datakey.

-d= Write Default Networking Parameters in the Datakey

This option will display the networking information contained in the Datakey.

-i= Reads Networking Parameters from the Datakey

This option will set the networking parameters permanently on the controller using values from the Datakey

-c= Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.

Normal operation of this option will be:

1. Read the Datakey networking parameters
2. Delete interfaces.conf and routes.conf from /f0/etc
3. Write new interfaces.conf and routes.conf in /f0/etc.
4. Execute idbgen to create new inetdb and inetdb2
5. Executes rpcdbgen to create a new rpcdb
6. Delete inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.
7. Relocate inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.

This option will display the current Controller Network Parameters such as the IP Address, Netmask, Gateway and MAC Address. This requires the network Stack to be initialized.

-r= Reads current Networking Configuration.

This option will set the networking parameters dynamically on the controller using values from the Datakey

-s= Sets Network Configuration Dynamically from the Datakey.

This option will set the networking parameters permanently on the controller using values from the command line. The option will do the same functions as option “c” with network parameters from the command line.

n= Set Controller Network Parameters without the Datakey

The netcfg -n -a [opts] -m [opts] -g [opts] shall allow the user to permanently set the IP Address, Subnet Mask and Gateway of the Model 2070 Controller when executed by the user at the command line using parameters provided by the user at the command line.

Where opts may be IP Address in the format xxx.xxx.xxx.xxx, netmask in the format xxx.xxx.xxx.xxx and gateway as xxx.xxx.xxx.xxx.

Example, the following sets the IP Address, Netmask and Gateway permanently in the Model 2070 Controller to 10.20.70.51, 255.255.255.0 and 10.20.70.254:

netcfg -n -a 10.20.70.51 –m 255.255.255.0 – g 10.20.70.254

These options will display the help menu on how to use the netcfg utility.

h, ?, blank = displays the help menu

The help menu shall consist of the following:

Netcfg Usage:

netcfg [- a] [-m] [-g] [-n] [-d] [- i] [-r] [-s]

-a follows Ip Address ; Write IP Address in Datakey
-m follows Netmask ; Write Netmask Address in Datakey
-g follows Gateway ; Write Gateway Address in Datakey

-d ;Write Default Networking Parameters in the Datakey

-i ;Reads Networking Parameters from the Datakey

-c ;Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.

-r ;Reads current Controller Networking Configuration.

-s ;Sets Network Configuration Dynamically from the Datakey.

-n <network parameters> ;Set Controller Network Parameters without Datakey

Example of option –n:
netcfg -n –a 10.20.70.51 –m 255.255.255.0 –g 10.20.70.254

See Section 9.2.6 for additional information.

9.2.7.5.6 ETC

A set of example configuration files consistent with the above networking modules shall be provided in the /f0/ETC directory.

The attributes of all files in the /f0/ETC directory shall be set using the following command:

$ attr –nprnpwnpenewr *
and the ownership shall be group.user ID of “0.0”.

This directory shall contain the following text files: hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf. makefile, nfs.map, nfsd.map in addition to the following makefile:

Include the following makefile:

```
#########################################################################
Model 2070 Controller                                   #
#                           Makefile
#########################################################################
# This makefile will make the inetdb,inetdb2 and rpcdb data modules        #
#
#########################################################################

-b
-bo

TRGTS       =     inetdb rpcdb
DEL             =       del -qf
COPY            =       copy
RPCDBGEN    =       rpcdbgen
ATTR            =       attr -rweprpwpe
IDBGEN            =     idbgen
OS          =     OSK
CPU         =     68k


ODIR        =     /f0/CMDS/BOOTOBJS
SDIR        =     /f0/ETC

SFILES            =     $(SDIR)/hosts $(SDIR)/hosts.equiv $(SDIR)/protocols \
                  $(SDIR)/networks $(SDIR)/services $(SDIR)/inetd.conf \
                  $(SDIR)/resolv.conf $(SDIR)/host.conf \
                  $(SDIR)/interfaces.conf $(SDIR)/routes.conf $(SDIR)/rpc
RFILES      =     $(SDIR)/nfs.map  $(SDIR)/nfsd.map
RPCOPT            =  # -s -c -d

all: $(TRGTS)
      $(COPY) -f $? -w=$(ODIR)
      $(COPY) -f inetdb2 -w=$(ODIR)

rpcdb: $(RFILES)
      $(DEL)  $@
      $(RPCDBGEN) -to=$(OS) -tp=$(CPU) -w=$(SDIR) -o=$@ $(RPCOPT)
      $(ATTR) $@

inetdb:  $(SFILES)
      $(DEL)  $@
      $(DEL)  $@2
      $(IDBGEN) -to=$(OS) -tp=$(CPU) -d=$(SDIR) $@
      $(ATTR) $@
      $(ATTR) $@2
clean:
      $(DEL)  $(ODIR)/inetdb
      $(DEL)  $(ODIR)/inetdb2
      $(DEL)  $(ODIR)/rpcdb

#########################################################################
```

The /f0/ETC/SSH directory shall be provided with the ssh configuration file named sshd_config.

9.2.7.6 Standard Microware File System Configuration

9.2.7.6.1 Directories

The 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBJS, /f0/ETC and /f0/SYS directories shall be implemented. Execute permission shall be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS shall contain the modules as identified above and other customizable descriptors and modules. The /f0/SYS shall contain the files named "motd" and "errmsg" as defined elsewhere in this section and the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf and loadnfs.

Include the following startspf file:

```
*-t -np
*
* startspf
* Shell Script to Start SPF System
*
* Set default directories before starting daemon programs
*
* chd /h0
* chx /h0/cmds
*
* Load SPF modules
*
/f0wp/sys/loadspf
*
* Load and start mbuf handler (May be done via p2 list in init module)
* Allow for error returned in case sysmbuf is already initialized.
*
*-nx
* mbinstall
*-x
*
* Start SPF system using ipstart
*
ipstart
*
* Add interfaces not specified in inetdb2
*
*ifconfig enet0 <my_address> binding /<dev>/enet
*ifconfig ppp0 binding /ipcp0
*
* Add any static routes. Even if running routed it may be useful
*   to add multicast routes.
*
*route add -net 224.0.0.0 <my_address>
*
* Start service daemons
*   routed: Dynamic routing server
*   inetd: FTP/Telnet and other protocols server
*   bootpd: Network boot protocol server
```

```
*
*routed <>>>/nil&
*inetd <>>>/nil&
*bootpd /h0/TFTPBOOT/bootptab <>>>/nil&
sshd <>>>/nil&

*
*   spfndpd: Hawk User state debugging daemon
*   spfnppd: Hawk Profiling daemon
*
*spfndpd <>>>/nil &
*spfnppd <>>>/nil &
*
* End
*
```

Include the following loadspf file:

```
*-t -np
*
* loadspf for SPF LAN Communication Package
* Load SPF System Modules
*
load -d /f0wp/cmds/bootobjs/inetdb
load -d /f0wp/cmds/bootobjs/inetdb2
*load -d sysmbuf                        * System Mbuf module
load -d /f0wp/cmds/bootobjs/pkman
load -d /f0wp/cmds/bootobjs/pkdvr
load -d /f0wp/cmds/bootobjs/pk
load -d /f0wp/cmds/bootobjs/pks
*load -d spf                            * SPF file manager
load -d /f0wp/cmds/bootobjs/spip
load -d /f0wp/cmds/bootobjs/ip4_timeslice
load -d /f0wp/cmds/bootobjs/sptcp
load -d /f0wp/cmds/bootobjs/tcp0
load -d /f0wp/cmds/bootobjs/spudp
load -d /f0wp/cmds/bootobjs/udp0
load -d /f0wp/cmds/bootobjs/spraw
load -d /f0wp/cmds/bootobjs/raw0
load -d /f0wp/cmds/bootobjs/sproute
load -d /f0wp/cmds/bootobjs/route0
*
* Load LAN Trap library and Commands
* Load one of the following Netdb name resolution trap handlers
*
*load -d /f0wp/cmds/bootobjs/netdb_local
*
* Load trap handler for DNS name resolution
*
load -d /f0wp/cmds/bootobjs/netdb_dns
*
* Load SPF Ethernet Drivers and Descriptors
*
load -d /f0wp/cmds/bootobjs/spenet
load -d /f0wp/cmds/bootobjs/enet
```

```
* Serial Drivers and Descriptors
*
*load -d spslip    spsl0                * Slip /t1
*load -d spipcp    ipcp0                * PPP IPCP
*load -d splcp     lcp0                 * PPP LCP
*load -d sphdlc    hdlc0                * PPP HDLC
*chd ../..
*load -d chat pppd ppplog pppauth; chd BOOTOBJS/SPF   * PPP Utilities
*
*
* Chd up to CMDS directory
*
*load -d mbinstall                      * Load mbinstall memory handler
                                        * (or can be done within init)
*
load -d /f0wp/cmds/ipstart
*
*
*load -d /f0wp/cmds/routed
*load -d /f0wp/cmds/inetd

*load -d idbgen idbdump ndbmod          ;* Development tools
load -d /f0wp/cmds/ifconfig
load -d /f0wp/cmds/route
*load -d route hostname ifconfig arp    ;* Runtime tools
load -d /f0/cmds/ping
load -d /f0wp/cmds/netstat
* Loads ssl/ssh Daemons and libraries.
load -d /f0wp/cmds/sshd

*
* Loads the Hawk Daemons.
*
*load -d /f0wp/cmds/spfndpd
*load -d /f0wp/cmds/ndpio
*load -d /f0wp/cmds/spfndpdc
*
* End
*
```

Include the following startnfs file:

```
*-t -np
*
* startnfs for NFS provided with LAN Communication Package
*
*
* Shell Script to Start NFS Client System and mount file systems
*
* NOTE: NFS client modules may be loaded into memory using loadnfs
*
chd /f0wp                      ;* Set default directories for NFS mounts
chx /f0wp/cmds                 ;* Programs are located in CMDS directory
SYS/loadnfs
*
* Start NFS client and mount remote file systems
```

```
*
iniz nfs_devices  ;* attach NFS client devices
*
* Example mount commands to connect to server systems remote device
*
*mount -m peer:/ /peer     ;* mount remote file systems
*mount alpha:/h0 /alpha <>>>/nil&
*mount electron:/home/joe/dat/Modules  /h0 <>>>/nil&
*
* Start NFS Server System
*
*
*  Specify file systems to export (Necessary if acting as a NFS Server)
*
*exportfs -s /f0wp       ;* specify remote mountable devices
*exportfs -s /r0    ;* specify remote mountable devices
*
* start rpc services daemons
* Uncomment portmap, mountd and nfsd if acting as a NFS Server
*
*portmap<>>>/nil&          ;* start portmap server      (rpcinfo)
*mountd<>>>/nil&           ;* mount server           (mount, showmount)
*nfsd<>>>/nil&             ;* nfs server               (..)
*
* End
*
```

Include the following loadnfs file:

```
*-t -np
*
* loadnfs for NFS modules provided with LAN Communication Package
*
* Load NFS Client Modules
*
* chd /f0wp/cmds/bootobjs
* NFS file manager, driver and descriptor
load -d /f0wp/cmds/bootobjs/nfs
load -d /f0wp/cmds/bootobjs/nfsnul
load -d /f0wp/cmds/bootobjs/nfs_devices
load -d /f0wp/cmds/bootobjs/rpcdb
*
* Load NFS Client Commands
*
* chd /f0wp
*
*load -d nfsc      mount                * Client connection handler
*load -d rpcdbgen rpcdump nfsstat       * RPC data module utilities
*load -d rpcinfo
*
* Load NFS Server Modules
*
*load -d exportfs portmap * NFS server required utilities/daemons
*load -d nfsd mountd      * NFS server required utilities/daemons
*load -d showmount
*
```

```
* Load RPC Client Modules
*
*load -d rcopy rload rpr on rup rusers spray
*
* Load RPC Server Modules
*
*load -d rldd rexdc rexd rstatd rusersd sprayd
*
*
* End
*
```

The motd file shall contain the Manufacturer's Name and TEES and Erratas Release information. The attributes of the motd file shall be set using the command attr –pwprwr motd and the ownership shall be set to group.user ID of "0.0"

Include the following motd file:

```
**********************************************************        ******
Manufacturer's Name      ******                  **
**     TEES Release 2009, Errata No. 3
**********************************************************
```

The errmsg file shall be the standard OS-9 errmsg file which defines OS-9 error codes 000:001 through 010:068. The attributes of the errmsg file shall be set using the command attr –pwprwr errormsg and the ownership shall be set to group.user ID of "0.0"

9.2.7.6.2 Password

The /f0/SYS shall contain a password encrypted "password" file with one entry, reg user. The password file should follow Microware's password file format for the addition and configuration of multiuser functionality and password protection. A user account with the name "reg", the encrypted password "user" shall be defined as listed in the password file. The attributes of all files in the /f0/sys directory, except for those files as mentioned elsewhere in these specifications, shall be set using the following command:

$ attr –nprnpwnpenewr *
and the ownership shall be group.user ID of "0.0".

Include the following password file:

```
*
* Password File
* Model 2070 Controller*
*
Reg,X.........X,20.70,128,/f0wp/cmds,/f0,shell -p="Reg:"
*
*
```

A Termcap text file shall be include in the /f0/SYS directory. This Termcap file shall contain description fields defining the capability names and values of the front panel DISPLAY.

9.2.7.6.3 utilities

The utilities tar, make, fixmod , mshell and vi shall be included in the /f0/CMDS directory.

9.2.7.6.4 Ver

A Ver utility shall be provided as part of the OS-9 Image and shall allow access to Controller's Manufacturer Name, Image Build Number, TEES Version, Image Build Date and CPU Module Type. Ver should display the contents of a data module named "bootid" which contains in its data area the following structure:

```
/* bootid_body*/
Struct bootid_body {

  char *mfgname;              /* Manufacturer Name */
  char *cpumoduletype;        /* CPU Module Type */
  char *teesrelease;          /* TEES Release */
  char *imagebuilddate;       /* Image Build Date */
  u_int 16 majv;              /* Major Version*/
  u_int 16 minv;              /* Minor Version */
  u_int 16 sv1;               /* Sub-Version 1 */
  u_int 16 sv2;               /* Sub-Version 2 */
  u_int 16 sv3                /* Sub-Version 3 */
  u_int 16 dv;                /* Development Version */
};
```

When run via the command line the Ver utility shall display the following:

Ver options:
-a Shows all information
-b CPU Module Type
-d Image Build Date
-m Controller's Manufacturer Name
-t TEES Version
-v Image Build Version Number
-? Display Help

CPU Type shall display 2070-1A, 2070-1E.

Image Build Date shall be in the form of mm/dd/yyyy

Manufacturer's name shall be shown as one word only.

TEES Version shall be "TEES XXXX EY" where XXXX is the year of the TEES and Y is any Errata if applicable.

Ver without an option shall be the same as Ver -a.

Ver –a shall display all information as shown by the following example:

2070 -1E
03/06/2008
Vendor Name
TEES 2008 E5 ; E5 Would be blank if there are no Erratas.
Build 2.7.3.0.0.0

The help menu shall consist of the following:

Ver Usage:

Ver [- a] [-b] [-d] [-m] [-t] [- v] [-?]

-a Shows all information
-b CPU Module Type
-d Image Build Date
-m Controller's Manufacturer Name
-t TEES Release
-v Image Build Version Number
-? Display Help

Os9 Edimod shall be used to generate the heater file and the "bootid" module using the following config.des file:

```
#include "defines.h" /*this file contains customization for the module */
#include <module.des> /* required for module definitions in modhcom  */

struct bootid_body /* this is the bootid module structure */
{
        pointer u_int32 mfgname = mn, "Manufacturer Name";
   pointer u_int32 cpumoduletype = cmt, "CPU Module Type";
        pointer u_int32 teesrelease = tr, "TEES Release";
   pointer u_int32 imagebuilddate = ibd, "Image Build Date ";
   u_int16 majv, "Major Version";
   u_int16 minv, "Minor Version";
        u_int16 sv1, "Sub-Version 1";
        u_int16 sv2, "Sub-Version 2";
        u_int16 sv3, "Sub-Version 3";
        u_int16 dv, "Development Version";
}, "bootid_body";
```

```
string mn = MfgName;
string cmt = CPUModuleType;
string tr = TEESRelease;
string ibd = ImageBuildDate;
string mod_name = "bootid";

init bootid_body
{
  majv = MajorVer;
  minv = MinorVer;
  sv1 = SubVer1;
  sv2 = SubVer2;
  sv3 = SubVer3;
};

init modhcom
{
  _maccess = 0x555;
  _mtype = MT_DATA;
  _mlang = 0;
  _mattr = 0x80;
  _mrev  = 1;
  _medit = 1;
};

module
{
  modhcom,
  bootid_body
};
```

9.2.8 Model 2070-1C CPU Software

9.2.8.1 Linux Operating System

The model 2070-1C CPU Module shall be supplied with Linux 2.6.35 kernel or later. Platform specific options shall be selected by the manufacturer based on the requirements of the MPC 82xx/ 83xx/85xx, or QorIQ (Power-Architecture-based).

The items marked with an asterisk (*) shall be the minimum Linux kernel configuration features that shall be included in the kernel build; others shall be included when possible:

```
#
# Automatically generated make config: don't edit
# Linux kernel version: 2.6.35
# Thu May 24 21:11:56 2018

#
# General setup
#
CONFIG_LOCK_KERNEL=y
CONFIG_INIT_ENV_ARG_LIMIT=32
CONFIG_CROSS_COMPILE=""
CONFIG_LOCALVERSION=""
# CONFIG_LOCALVERSION_AUTO is not set
CONFIG_SWAP=y
CONFIG_SYSVIPC=y
CONFIG_SYSVIPC_SYSCTL=y
CONFIG_POSIX_MQUEUE=y
CONFIG_POSIX_MQUEUE_SYSCTL=y
# CONFIG_BSD_PROCESS_ACCT is not set
# CONFIG_TASKSTATS is not set
# CONFIG_AUDIT is not set

#
#
# RCU Subsystem
#

CONFIG_MODULES=y *
CONFIG_MODULE_UNLOAD=y *
CONFIG_MODVERSIONS=y
CONFIG_MODULE_SRCVERSION_ALL=y
# CONFIG_TREE_RCU_TRACE is not set
CONFIG_IKCONFIG=y *
CONFIG_IKCONFIG_PROC=y *
CONFIG_LOG_BUF_SHIFT=17
CONFIG_CGROUPS=y
# CONFIG_CGROUP_DEBUG is not set
CONFIG_CGROUP_NS=y
CONFIG_CGROUP_FREEZER=y
CONFIG_CGROUP_DEVICE=y
CONFIG_CPUSETS=y
CONFIG_PROC_PID_CPUSET=y
CONFIG_CGROUP_CPUACCT=y
CONFIG_RESOURCE_COUNTERS=y
CONFIG_CGROUP_MEM_RES_CTLR=y
CONFIG_CGROUP_MEM_RES_CTLR_SWAP=y
CONFIG_CGROUP_SCHED=y
CONFIG_FAIR_GROUP_SCHED=y
CONFIG_RT_GROUP_SCHED=y
CONFIG_BLK_CGROUP=m
# CONFIG_DEBUG_BLK_CGROUP is not set
CONFIG_MM_OWNER=y
# CONFIG_SYSFS_DEPRECATED_V2 is not set
CONFIG_RELAY=y
CONFIG_NAMESPACES=y
CONFIG_UTS_NS=y
CONFIG_IPC_NS=y
```

```
# CONFIG_USER_NS is not set
# CONFIG_PID_NS is not set
CONFIG_NET_NS=y
CONFIG_BLK_DEV_INITRD=y
CONFIG_INITRAMFS_SOURCE=""
CONFIG_RD_GZIP=y
CONFIG_RD_BZIP2=y
CONFIG_RD_LZMA=y
CONFIG_RD_LZO=y
# CONFIG_CC_OPTIMIZE_FOR_SIZE is not set
CONFIG_SYSCTL=y
CONFIG_ANON_INODES=y
CONFIG_EMBEDDED=y *
CONFIG_SYSCTL_SYSCALL=y
CONFIG_KALLSYMS=y
CONFIG_KALLSYMS_ALL=y
# CONFIG_KALLSYMS_EXTRA_PASS is not set
CONFIG_HOTPLUG=y *
CONFIG_PRINTK=y
CONFIG_BUG=y
CONFIG_ELF_CORE=y
CONFIG_BASE_FULL=y
CONFIG_FUTEX=y
CONFIG_EPOLL=y
CONFIG_SIGNALFD=y
CONFIG_TIMERFD=y
CONFIG_EVENTFD=y
CONFIG_SHMEM=y *

#
# GCOV-based kernel profiling
#
CONFIG_GCOV_KERNEL=y
# CONFIG_GCOV_PROFILE_ALL is not set
CONFIG_SLOW_WORK=y
# CONFIG_SLOW_WORK_DEBUG is not set
# CONFIG_HAVE_GENERIC_DMA_COHERENT is not set
CONFIG_SLABINFO=y
CONFIG_RT_MUTEXES=y
CONFIG_BASE_SMALL=0
CONFIG_MODULES=y *
# CONFIG_MODULE_FORCE_LOAD is not set
CONFIG_MODULE_UNLOAD=y *
# CONFIG_MODULE_FORCE_UNLOAD is not set
# CONFIG_MODVERSIONS is not set
CONFIG_MODULE_SRCVERSION_ALL=y
CONFIG_STOP_MACHINE=y
CONFIG_BLOCK=y
CONFIG_BLK_DEV_BSG=y
CONFIG_BLK_DEV_INTEGRITY=y
CONFIG_BLOCK_COMPAT=y

#
# Processor type and features
#

CONFIG_PREEMPT=y *
```

```
CONFIG_PREEMPT_BKL=y

#
# Kernel options
#
CONFIG_TICK_ONESHOT=y *
CONFIG_NO_HZ=y *
CONFIG_HIGH_RES_TIMERS=y *
CONFIG_GENERIC_CLOCKEVENTS_BUILD=y
# CONFIG_HZ_100 is not set
CONFIG_HZ_250=y *
# CONFIG_HZ_300 is not set
# CONFIG_HZ_1000 is not set
CONFIG_HZ=250
CONFIG_SCHED_HRTICK=y
# CONFIG_PREEMPT_NONE is not set
CONFIG_PREEMPT_VOLUNTARY=y
# CONFIG_PREEMPT is not set
CONFIG_BINFMT_ELF=y
CONFIG_COMPAT_BINFMT_ELF=y

#
# Bus options (PCI, PCMCIA, EISA, MCA, ISA)
#
CONFIG_PCI=y
CONFIG_PCI_GOANY=y
CONFIG_PCI_BIOS=y
CONFIG_PCI_DIRECT=y

#
# Executable file formats
#
CONFIG_BINFMT_ELF=y *

#
# Networking
#
CONFIG_NET=y

#
# Networking options
#
CONFIG_PACKET=y *
CONFIG_PACKET_MMAP=y *
CONFIG_UNIX=y *
CONFIG_INET=y *
CONFIG_IP_MULTICAST=y *
CONFIG_IP_FIB_HASH=y
CONFIG_IP_PNP=y *
CONFIG_IP_PNP_DHCP=y *
CONFIG_IP_PNP_BOOTP=y *
CONFIG_IP_PNP_RARP=y
CONFIG_SYN_COOKIES=y *
CONFIG_TCP_CONG_BIC=y

#
# IP: Virtual Server Configuration
```

```
#
CONFIG_IPV6=y
CONFIG_NETFILTER=y *

#
# Device Drivers
#

#
# Generic Driver Options
#
CONFIG_STANDALONE=y
CONFIG_PREVENT_FIRMWARE_BUILD=y
CONFIG_FW_LOADER=m

#
# Block devices
#
CONFIG_BLK_DEV_FD=y
CONFIG_BLK_DEV_LOOP=y *
CONFIG_BLK_DEV_NBD=m
CONFIG_BLK_DEV_RAM=y *
CONFIG_BLK_DEV_RAM_COUNT=16
CONFIG_BLK_DEV_RAM_SIZE=4096
CONFIG_BLK_DEV_RAM_BLOCKSIZE=1024
CONFIG_BLK_DEV_INITRD=y *

#
# SCSI device support
#
CONFIG_SCSI=y *
CONFIG_SCSI_PROC_FS=y *

#
# SCSI support type (disk, tape, CD-ROM)
#
CONFIG_BLK_DEV_SD=y *
#

#
# Network device support
#
CONFIG_NETDEVICES=y
CONFIG_DUMMY=y
#
# Ethernet (10 or 100Mbit)
#
CONFIG_NET_ETHERNET=y *
CONFIG_MII=y
#
# Wan interfaces
#
CONFIG_WAN=y
CONFIG_PPP=y
CONFIG_PPP_FILTER=y
CONFIG_PPP_ASYNC=y
CONFIG_PPP_SYNC_TTY=y
```

```
CONFIG_PPP_DEFLATE=y
CONFIG_PPP_BSDCOMP=y
CONFIG_SLIP=y
CONFIG_SLIP_COMPRESSED=y
CONFIG_SLIP_MODE_SLIP6=y
#
# Input device support
#
CONFIG_INPUT=y
#
# Serial drivers
#
#
# Non-8250 serial port support
#
CONFIG_UNIX98_PTYS=y *
CONFIG_LEGACY_PTYS=y *
CONFIG_LEGACY_PTY_COUNT=256 *

#
#
#
CONFIG_RTC=y
#
#
# I2C support
#
CONFIG_I2C=y
#
# I2C Algorithms
#
CONFIG_I2C_ALGOBIT=m
CONFIG_I2C_ALGOPCF=m
#
# SPI support
#
CONFIG_SPI=y
CONFIG_SPI_MASTER=y
#
# USB support
#
CONFIG_USB_ARCH_HAS_HCD=y
CONFIG_USB_ARCH_HAS_OHCI=y
CONFIG_USB_ARCH_HAS_EHCI=y
CONFIG_USB=y *
#
# Miscellaneous USB options
#
CONFIG_USB_DEVICEFS=y *

#
# NOTE: USB_STORAGE enables SCSI, and 'SCSI disk support'
#
# may also be needed; see USB_STORAGE Help for more information
#
CONFIG_USB_STORAGE=y *
CONFIG_USB_STORAGE_FREECOM=y *
```

```
CONFIG_USB_STORAGE_ISD200=y *
CONFIG_USB_STORAGE_DPCM=y *

#
# USB Input Devices
#
CONFIG_USB_HID=y
CONFIG_USB_HIDINPUT=y

#
#

#
# File systems
#
CONFIG_EXT2_FS=y *
CONFIG_EXT3_FS=y
CONFIG_JBD=y
CONFIG_INOTIFY=y
CONFIG_INOTIFY_USER=y
CONFIG_DNOTIFY=y

#
# DOS/FAT/NT Filesystems
#
CONFIG_FAT_FS=y *
CONFIG_MSDOS_FS=y *
CONFIG_VFAT_FS=y *
CONFIG_FAT_DEFAULT_CODEPAGE=437 *
CONFIG_FAT_DEFAULT_IOCHARSET="iso8859-1" *
CONFIG_NTFS_FS=m
CONFIG_NTFS_RW=y

#
# Pseudo filesystems
#
CONFIG_PROC_FS=y *
# CONFIG_PROC_KCORE is not set
CONFIG_SYSFS=y *
CONFIG_TMPFS=y *

#
# Miscellaneous filesystems
#

#
# Network File Systems
#
CONFIG_NFS_FS=y *
CONFIG_NFS_V3=y *
CONFIG_NFSD=y *
CONFIG_NFSD_V3=y *
CONFIG_NFSD_TCP=y *
CONFIG_ROOT_NFS=y *
CONFIG_LOCKD=y *
CONFIG_LOCKD_V4=y *
CONFIG_EXPORTFS=y *
```

```
CONFIG_NFS_COMMON=y *
CONFIG_SUNRPC=y *

#
# Native Language Support
#
CONFIG_NLS=y
CONFIG_NLS_DEFAULT="iso8859-1" *


#
# Kernel hacking
#
CONFIG_TRACE_IRQFLAGS_SUPPORT=y
# CONFIG_PRINTK_TIME is not set
# CONFIG_MAGIC_SYSRQ is not set
# CONFIG_UNUSED_SYMBOLS is not set
# CONFIG_DEBUG_KERNEL is not set
CONFIG_LOG_BUF_SHIFT=14
# CONFIG_DEBUG_BUGVERBOSE is not set
# CONFIG_DEBUG_FS is not set
# CONFIG_UNWIND_INFO is not set
CONFIG_EARLY_PRINTK=y
# CONFIG_DOUBLEFAULT is not set

#
# Security options
#
# CONFIG_KEYS is not set
# CONFIG_SECURITY is not set

#
# Cryptographic options
#
CONFIG_CRYPTO=y *
CONFIG_CRYPTO_HMAC=y *
CONFIG_CRYPTO_MD4=y
CONFIG_CRYPTO_MD5=y *
CONFIG_CRYPTO_SHA1=y
CONFIG_CRYPTO_DES=y
CONFIG_CRYPTO_AES=y
CONFIG_CRYPTO_ARC4=y

#
# Library routines
#
CONFIG_CRC_CCITT=y
CONFIG_CRC32=y
CONFIG_ZLIB_INFLATE=y*
CONFIG_ZLIB_DEFLATE=y*

#
# Security options
#
CONFIG_DEFAULT_SECURITY_DAC=y
CONFIG_DEFAULT_SECURITY=""
CONFIG_CRYPTO=y *
```

```
#
# Crypto core or helper
#
CONFIG_CRYPTO_ALGAPI=y
CONFIG_CRYPTO_ALGAPI2=y
CONFIG_CRYPTO_AEAD=m
CONFIG_CRYPTO_AEAD2=y
CONFIG_CRYPTO_BLKCIPHER=y
CONFIG_CRYPTO_BLKCIPHER2=y
CONFIG_CRYPTO_HASH=y
CONFIG_CRYPTO_HASH2=y
CONFIG_CRYPTO_RNG=y
CONFIG_CRYPTO_RNG2=y
CONFIG_CRYPTO_PCOMP=y
CONFIG_CRYPTO_MANAGER=y
CONFIG_CRYPTO_MANAGER2=y
CONFIG_CRYPTO_WORKQUEUE=y
CONFIG_CRYPTO_AUTHENC=m

#
# Authenticated Encryption with Associated Data
#
CONFIG_CRYPTO_CCM=m
CONFIG_CRYPTO_GCM=m
CONFIG_CRYPTO_SEQIV=m

#
# Block modes
#
CONFIG_CRYPTO_CBC=y
CONFIG_CRYPTO_CTR=m
CONFIG_CRYPTO_ECB=y
CONFIG_CRYPTO_PCBC=m

#
# Hash modes
#
CONFIG_CRYPTO_HMAC=y *

#
# Digest
#
CONFIG_CRYPTO_CRC32C=m
CONFIG_CRYPTO_GHASH=m
CONFIG_CRYPTO_MD5=y
CONFIG_CRYPTO_SHA256=m

#
# Ciphers
#
CONFIG_CRYPTO_AES=y *

#
# Compression
#
CONFIG_CRYPTO_DEFLATE=m
```

```
#
# Random Number Generation
#
CONFIG_CRYPTO_ANSI_CPRNG=m
CONFIG_CRYPTO_HW=y
```

9.2.8.2 Linux Drivers

All Linux Drivers provided in the Model 2070-1C CPU shall be compliant to the latest version of the AASHTO, ITE and NEMA ATC Standard Annex B and as defined in these specifications. In case of conflict these specifications shall govern over ATC Standard.

GPIO

The GPIO driver allows the user to control the CPU active LED, determine if the Datakey is present, reset peripheral devices, and power down peripheral devices.

`open()`

The following dev entries shall exist:
/dev/datakeypresent
/dev/cpuactive
/dev/powerdown
/dev/cpureset

`read()`

int read(int filp, void *buf, int count);

This allows for reading the state of the power down pin and for reading the state of the whether the Datakey is inserted. The value passed in the count parameter must be 1 or no bytes will be read.

`write()`

int write(int filp, void *buf, int count);

Allows changing the state of the CPU Active LED and the CPU reset signal. Writing a binary one to the /dev/cpuactive device shall turn on the CPU active LED and writing zero will turn off the LED.

`close()`

Closes the file descriptor.

Timers

The Linux Kernel shall be configured to support high resolution timers by setting the CONFIG_HIGH_RES_TIMERS = y as per Section 9.2.8.1.

Time of Day

The Time of Day driver overrides the operating system internal time of day to utilize AC line sync pulses or square wave pulses from the RTC. The time source can be changed via an ioctl command.

Supported Device File Operations:
open();
close();
read();
write();
ioctl();

open()

The dev entry for the timer driver shall be /dev/tod. The device can be opened for read, write, or read/write.

close()

Closes the file descriptor.

read() / write()
int read(int *filp*, void **buf*, int *count*);
int write(int *filp*, void **buf*, int *count*);

Reads / Writes the current time of day value in the following format:
YYYYMMDDHHMMSSFFF
Y = year M = month D = day H = hour M = minute S = second F = fraction

The fractional field shall be a value from 0 to 127 in RTC Square Wave Mode and a value from 0 to 2 * AC Line Sync Frequency - 1 in AC Line Sync Mode.

If the *count* passed to the read() function is greater than 18, only 18 bytes will be read. A read always starts with the 4 byte year in ASCII decimal. If the count is less than 18, then read shall modify *count* bytes in *buf*.

If the *count* passed to write() is less than 17 or the data in *buf* is not in the proper format, then write shall return an error of EINVAL.

ioctl()
ioctl(int *fd*, unsigned int *cmd*, unsigned long *param*);

The ioctl function supports multiple different commands, each described separately.

Command Definitions:
ATC_TOD_SET
ATC_TOD_GET
ATC_TOD_SET_TIMESRC
ATC_TOD_GET_TIMESRC
ATC_TOD_GET_INPUT_FREQ

ATC_TOD_REQUEST_TICK_SIG
ATC_TOD_CANCEL_TICK_SIG
ATC_TOD_REQUEST_ONCHANGE_SIG
ATC_TOD_CANCEL_ONCHANGE_SIG
ATC_DST_ENABLE
ATC_DST_DISABLE
ATC_DST_SET_INFO
ATC_DST_GET_INFO

ATC_SET and ATC_GET

These commands get and set the time and time zone atomically. The parameter to both functions is the same and defined below:

```
Parameter Data:
       typedef struct {
         struct timeval *tv;
         int *tzsec_offset;
         int *dst_offset;
       } atc_time_tz_t
```

The ATC_SET command is only concerned with the *tv* and *tzsec_offset* parameters. If the *tv* member is non-zero and the command is ATC_SET, then the time is set according to the tv_sec and tv_usec members of the struct timeval *tv. Additionally if the *tzsec_offset* parameter is non-zero the time zone offset is also set. The ATC_GET command sets the data pointed to by the *tv, tzsec_offset,* and *dst_offset* for each of those members that are non-zero.

ATC_SET_TIMESRC and ATC_GET_TIMESRC

```
Parameter Definitions:
            ATC_TIMESRC_LINESYNC
            ATC_TIMESRC_RTCSQWR
            ATC_TIMESRC_CRYSTAL
            ATC_TIMESRC_EXTERNAL1
            ATC_TIMESRC_EXTERNAL2
```

These commands get and set the time source. The time source may use AC line sync pulses or the RTC square wave output.

ATC_TOD_GET_INPUT_FREQ

This command gets the current frequency that is driving the time of day clock.

ATC_TOD_REQUEST_TICK_SIG

This command requests a signal to be sent at each tick of the time of day clock as long as the file device remains opened. The *param* value passed to ioctl is the signal number that should be sent to the calling process at each time of day clock tick.

ATC_TOD_CANCEL_TICK_SIG

This releases the signal from being sent when the time of day clock ticks. If the file device is closed, the signal is automatically released.

ATC_TOD_REQUEST_ONCHANGE_SIG

This command requests a signal to be sent each time the time of day clock is changed by more than one tick. The *param* value passed to ioctl is the signal number that should be sent to the calling process.

ATC_TOD_CANCEL_ONCHANGE_SIG

This releases the signal from being sent when the time of day is changed by more than one tick. If the file device is closed, the signal is automatically released.

ATC_DST_ENABLE and ATC_DST_DISABLE

These commands enable and disable daylight saving time to be in effect.

glibc and Busybox

The Model 2070 LX shall use the GNU C Library (glibc) release v 2.23 or later. The Linux system shall use Busybox v1.22.1 or later for all Linux utilities except for those listed on Section 9.2.8.4.

Datakey

This driver provides full capability for manipulating Datakey devices. Datakeys of size 2Mbit and above, as listed in Section 9.2.6 of these specifications, shall be supported.

```
Supported Device File Operations:
open();
close();
read();
write();
lseek();
ioctl();
```

open()

The dev entry for the Datakey shall be /dev/datakey. The Datakey can be opened for Read, Write, or Read/Write.

Examples:

```
fd = open("/dev/datakey", O_RDONLY);
fd = open("/dev/datakey", O_WRONLY);
fd = open("/dev/datakey", O_RDWR);
```

read()

int read(int *filp*, void **buf*, int *count*);

Reads up to *count* bytes into *buf* and returns the number of bytes read. The read occurs at the current position within the device.

> **Note: The current position can be determined using the ioctl. The current position can be changed using the lseek() function.**

Possible Errors:

ENXIO if Datakey is not present
EBUSY if the signature changes
EIO if end of file condition has already been reached

`write()`

int write(int *filp*, void **buf*, int *count*);

Writes *count* bytes to the device at the current file position within the device. If all of the bytes specified by *count* cannot be written before the end of the device no bytes shall be written and an error shall be returned. The number of bytes written shall be returned. If the value returned is less than *count*, then the returned value of bytes was written correctly, but the remaining bytes contain errors. In this case it is necessary to try the write again for the remaining bytes or repeat the same write again until the number of bytes returned matches the *count*.

`Possible Errors:`

ENXIO if Datakey is not present
EBUSY if the device signature changes (ie. Someone switched devices really fast)
EIO if end of file condition would occur writing the number of bytes specified.

`close()`

Closes the file descriptor.

`lseek()`

lseek(int *fd*, int *pos*, int *type*);

Seeks to a specified position in the device. Both absolute and relative types of seeking are supported. If relative seeking is specified the *pos* value may be positive or negative. If absolute seeking is specified the file position is assigned to the *pos* value. If seeking outside the device size is attempted an error is returned and no change to the file position takes place.

`Type Definitions:`
`ATC_DATAKEY_SEEK_ABS`
`ATC_DATAKEY_SEEK_REL`

`ioctl()`

ioctl(int *fd*, unsigned int *cmd*, unsigned long *param*);

The ioctl function supports multiple different commands, each described separately. If the Datakey is not inserted ENXIO is returned as the error code.

Command Definitions:

ATC_DATAKEY_GET_FILE_POS
ATC_DATAKEY_ERASE_ALL
ATC_DATAKEY_ERASE_SECTOR
ATC_DATAKEY_READ_PROTECT_BITS
ATC_DATAKEY_WRITE_PROTECT_BITS
ATC_DATAKEY_GET_DEVICE_SIZE
ATC_DATAKEY_GET_SECTOR_SIZE

ATC_DATAKEY_GET_FILE_POS

Returns the current file position. The *param* value is ignored.

ATC_DATAKEY_ERASE_ALL

Erases all data on the Datakey. The *param* value is ignored. Always returns 0.

Note: When data is erased, all values are read as 0xFF.

ATC_DATAKEY_ERASE_SECTOR

Erases all data in the sector containing the address specified by *param*. Returns 0 on success or EINVAL on invalid address. The sector size can be determined using the appropriate ioctl() in order to know what address ranges will be erased by this command.

ATC_DATAKEY_READ_PROTECT_BITS

Returns the value of the protect bits directly read from the Datakey. The data format will be in accordance with the datasheet for the Datakey being used (not the same for different device sizes). This function is provided so the user can ensure that the device is not protected. The *param* value is ignored.

ATC_DATAKEY_WRITE_PROTECT_BITS

Writes the value specified in *param* directly to the Datakey protection byte. The data format varies in accordance with the datasheet for the Datakey being used. This function is provided primarily so that the user can remove protection if writing is being prevented.

ATC_DATAKEY_GET_DEVICE_SIZE

Returns the size of the Datakey device in bytes. The *param* value is ignored.

ATC_DATAKEY_GET_SECTOR_SIZE

Returns the sector size of the Datakey in bytes. The *param* value is ignored.

Constants Defined by this specification

The content of atc_spxs.h is displayed on this page.

```
#ifndef __ATC_SPXS_H
#define __ATC_SPXS_H

#define ATC_SPXS_WRITE_CONFIG   0
#define ATC_SPXS_READ_CONFIG    1

#define ATC_LKM_SP1S            1
#define ATC_LKM_SP2S            2
#define ATC_LKM_SP3S            3
#define ATC_LKM_SP5S            5
#define ATC_LKM_SP8S            8

#define ATC_SDLC                0
#define ATC_SYNC                1
#define ATC_HDLC                2

#define ATC_B1200               0
#define ATC_B2400               1
#define ATC_B4800               2
#define ATC_B9600               3
#define ATC_B19200              4
#define ATC_B38400              5
#define ATC_B57600              6
#define ATC_B76800              7
#define ATC_B115200             8
#define ATC_B153600             9
#define ATC_B614400             10
const int ATC_B[] = { 1200, 2400, 4800, 9600, 19200, 38400,
                      57600, 76800, 115200, 153600, 614400 };

#define ATC_CLK_INTERNAL        0
#define ATC_CLK_EXTERNAL        1

#define ATC_GATED               0
#define ATC_CONTINUOUS          1

typedef struct atc_spcx_config_t {
    unsigned char protocol;
    unsigned char baud;
    unsigned char transmit_clock_source;
    unsigned char transmit_clock_mode;
} atc_spxs_config;

#endif
```

The content of atc.h is displayed on the following two pages.

```
#ifndef __ATC_H
#define __ATC_H

// Device File Names
#define ATC_DATAKEY_DEV "/dev/datakey"
#define ATC_GPIO_POWERDOWN_DEV "/dev/powerdown"
#define ATC_GPIO_DATAKEY_DEV "/dev/datakeypresent"
#define ATC_GPIO_CPUACTIVE_DEV "/dev/cpuactive"
#define ATC_GPIO_CPURESET_DEV "/dev/cpureset"
#define ATC_TIMING_TOD_DEV "/dev/tod"

#define ATC_SP1 "/dev/sp1"
#define ATC_SP2 "/dev/sp2"
#define ATC_SP3 "/dev/sp3"
#define ATC_SP4 "/dev/sp4"
#define ATC_SP5 "/dev/sp5"
#define ATC_SP6 "/dev/sp6"
#define ATC_SP8 "/dev/sp8"

#define ATC_SP1S "/dev/sp1s"
#define ATC_SP2S "/dev/sp2s"
#define ATC_SP3S "/dev/sp3s"
#define ATC_SP4S "/dev/sp4s"
#define ATC_SP5S "/dev/sp5s"
#define ATC_SP6S "/dev/sp6s"
#define ATC_SP8S "/dev/sp8s"

// DATAKEY IOCTL CONSTANTS
#define ATC_DATAKEY_GET_FILE_POS 3
#define ATC_DATAKEY_ERASE_ALL 6
#define ATC_DATAKEY_ERASE_SECTOR 7
#define ATC_DATAKEY_READ_PROTECT_BITS 8
#define ATC_DATAKEY_WRITE_PROTECT_BITS 9
#define ATC_DATAKEY_GET_DEVICE_SIZE 10
#define ATC_DATAKEY_GET_SECTOR_SIZE 11

// DATAKEY LSEEK CONSTANTS
#define ATC_DATAKEY_SEEK_REL 0
#define ATC_DATAKEY_SEEK_ABS 1

// Time of Day driver Definitions
#define ATC_TOD_SET_TIMESRC 1
#define ATC_TOD_GET_TIMESRC 2
#define ATC_TOD_GET_INPUT_FREQ 3
#define ATC_TOD_REQUEST_TICK_SIGNAL 5
#define ATC_TOD_CANCEL_TICK_SIGNAL 6
#define ATC_TOD_DST_ENABLE 10
#define ATC_TOD_DST_DISABLE 11
```

```
#define ATC_TOD_DST_SETINFO 12
#define ATC_TOD_DST_GETINFO 13

#define ATC_SET_TIMESRC 1
#define ATC_TIMESRC_LINESYNC 0
#define ATC_TIMESRC_RTCSQWR 1

typedef struct atc_datakey_t {
    unsigned int16 fcs;
    unsigned int8 type;
    unsigned int8 version;
    unsigned int32 latitude;
    unsigned int32 longitude;
    unsigned int16 id;
    unsigned int16 drop;
    unsigned int32 ipaddress;
    unsigned int32 subnet;
    unsigned int32 gataway;
    unsigned int8 reserved[36];

} atc_datakey;

#endif
```

9.2.8.3 Linux Application Kernel

9.2.8.3.1 Boot Sysreset

The provided software shall boot Linux from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the defaults parameters as listed in A9-16.

The default configuration settings for the console port, /dev/sp4, shall be 115.2 kbps, no parity, 8 data bits, and 1 stop bit. The default condition of the console output shall be enabled at power up and the controller shall send any external output to /dev/sp4 during bootup.

9.2.8.3.2 Hardware Initialization

The Engine Board low-level hardware and O/S software initialization shall be completed within a maximum of 4.5 seconds from the release of STARTUP/SYSRESET as shown in A9-17. This startup time shall be measured from the release of STARTUP/SYSRESET to the turn on of the cpuactive LED using a user level program named onled.

9.2.8.3.3 Startup Procedure and initialization

The Linux boot image shall startup as described in the latest version of the AASHTO, ITE and NEMA ATC Standard Section 4.3.5.1. The boot up process shall be completed within the time period specified in Section 9.2.8.3.2 of these specifications. The Linux System shall use a scripted method for initialization compatible with SysVinit methods. Init script names shall take the form 'S' followed by a 2-digit number in the range 00-99 (giving a relative starting order), followed by the service name, e.g. "S40network". The init scripts shall reside in "/etc/init.d/. The /etc/init.d directory shall store various shell scripts which can be used for the following functions:

1. Load kernel drivers (modules).
2. Check and mount file systems.
3. Setup network.
4. Mount remote file systems (such as nfs).
5. Start web server and other services.
6. Run applications

The following syntax shall control various services:

```
# /etc/init.d/NAME start|stop|restart|status
```

OR

```
# /sbin/service NAME start|stop|restart|status
```

Where,

1. **start** : Start a service (such as Secure Shell by typing ‘services sshd start’)
2. **stop** : Stop a service (such as Secure Shell by typing ‘services sshd stop’).
3. **restart** : Restart (stop and then start) a service (such as Secures Shell by typing ‘service sshd restart’) .
4. **status** : Find out whether a service is currently running or not (such as Secure Shell by typing ‘services sshd status’)

The Service Command shall be used to run a System V init scripts.

Linux startup shall be configured to auto run a script or execute Linux binary named startup residing in the USB Memory upon power up with USB Memory inserted. If there is no USB Memory inserted in the Model 2070-1C Module, Linux shall boot normally.

9.2.8.4 Linux Utilities

The following Linux utilities shall be provided resident in the Model 2070-1C CPU Module:

onled, cpureset, fl, vi, bash

The Model 2070LX shall use the GNU Bash v4.3.33 or later as the default Linux shell.

ONLED (onled) program shall be provided in the /bin directory. The onled program shall be a Linux binary and shall toggle the cpuactive LED when executed.

The onled, cpureset and fl utilities shall be resident in the /usr/bin directory per the FHS-3.0 as reference in section 9.2.8.8.

9.2.8.5 Linux Ver

A **Ver** utility and a Dynamically Linked "Shared Object" Library, libbootid.so shall be provided as part of the Linux Image. The library shall be resident in the /usr/lib directory. The Ver utility shall be used to display the contents of a shared memory library libbootid.so:

* Controller's Manufacturer Name
* CPU Module Type
* TEES Conformance Version
* ATC Std Version
* System Image Version
* System Image Build Date

The Shared Object library shall contain the *bootid_body* structure, and shall be readable by all applications.

The **Ver** utility shall have the following required options with the listed functions. Additional manufacturer-specific options are permitted.

-a shall display **A**ll the information from the bootid_body structure in shared memory; this is the default if no command options are given

-c shall display the **C**PU module type, Example "2070-1C"

-d shall display the build **D**ate of the system image in ISO 8601 extended format: *yyyy-mm-dd*

-m shall display the **M**anufacturer's name

-s shall displays the ATC **S**tandard Version

-t shall display the applicable **T**EES conformance document in the format: TEES *yyyy*[E*n*], where *yyyy* is the year of the TEES and *n* is the Errata number, if applicable; examples: "TEES 2009", "TEES 2009 E3"

-v shall display the **V**ersion of the system
-h shall display a command **H**elp message

The C header file bootid.h shall be as follows:

```
/* bootid.h */

#ifndef _BOOTID_H
#define _BOOTID_H

typedef struct _BootId_t
{
        char *mfgname;          /* Manufacturer Name */
        char *cpumoduletype;    /* CPU Module Type */
        char *teesrelease;      /* TEES Release */
        char *atcstdversion;    /* ATC Std Version */
        char *imagebuilddate;   /* Image Build Date */
        unsigned short majv;    /* Major Version*/
        unsigned short minv;    /* Minor Version */
        unsigned short sv1;     /* Sub-Version 1 */
        unsigned short sv2;     /* Sub-Version 2 */
        unsigned short sv3;     /* Sub-Version 3 */
        unsigned short dv;      /* Development Version */
} const BootId_t;

extern BootId_t* get_boot_id(void );

#endif /*_BOOTID_H */
```

The default output of **Ver** :

Manufacturer Name: Company X
CPU Module Type: 2070-1C
TEES Release: TEES 2009 Erratum 3
ATC Std Version: Std 6.31
Image Build Version: 1.1.1.1.14.1
Image Build Date: June 30 2018

The Ver usage information shall be as follows:

Usage: ver [options] Options:
-a All information (default)
-c CPU module type
-d Date of system image
-m Manufacturer name
-s ATC Standard Version
-t TEES release
-v Version of system image
-h This Help message

Usage Examples Usage help:

[admin]$ **Ver -h** Usage: Ver [options] Options:
-a All information (default)
-c CPU module type
-d Date of system image
-m Manufacturer name
-s ATC Std Version
-t TEES release compliance
-v Version of system image
-h This help message

Run with specific information flags: [admin]$ **Ver -mvd**
Company X
1.4.0.0.0.0
2016-08-01

9.2.8.6 Linux cpuinfo

In addition to the default parameters, the following configurable information shall be provided in the content of the /proc/cpuinfo file:

Platform	:	ATC Engine Board
Model	:	MPCXXXX, PXXXX, or

Where XXXX is the Model number of the MPC or the QorIQ processor family.

Example: MPC8340

9.2.8.7 Linux Network Requirements

The following Network utilities not listed under FHS-3.0 shall be provided resident in the Model 2070-1C CPU Module:

arp, ifconfig, netstat, ping, showmount, ntpdate, ntpq, ntptime ntp-wait, and rpcinfo

Full support for NFS and shall have the following daemons resident:

rpc.mountd, and rpc.nfsd

Full support for OpenSSH 7.6 or later and shall have the following daemons and utilities resident:

ssh, scp, sftp, ssh-add, ssh-keysign, ssh-keyscan, ssh-keygen,

sshd, sftp-server and ssh-agent.

Full support for VSFTP in addition to sftp-server and shall have the following daemons resident:

vsftpd release v3.0.3

Full support for NTP and shall have the following daemons resident:

ntpd and ntdpc

9.2.8.8 Linux File System

The Model 2070-1C CPU Module Linux File System Configuration shall meet the requirements and guidelines for files, directories and utility commands as per the Filesystem Hierarchy Standard (FHS-3.0) dated March 15, 2015. The Linux Kernel shall be configured to use the Unsorted Block Image File System (UBIFS).

9.2.9 Re-Flash Utility

A Utility Program shall be provided that would allow the user to upgrade (re-flash) the Boot Image for the Model 2070-1A and E CPU as defined in section 9.2.7. This utility shall provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer. The Utility Program shall provide the capability for the user to dynamically upgrade the Boot Image via the command prompt. The contractor shall also provide a copy in CD-ROM Memory of all files originally stored in the flash drive /f0 so that they can be reloaded as needed.

9.2.10 Communications Loading Test

The Model 2070 Controller using the Model 2070-1A and 1E CPU shall pass a Communications Loading Test consisting of Serial and Network Communications. The test shall run Sp1, Sp2, Sp3, and Sp8 at 9600 bytes per second in a continuous full duplex asynchronous/synchronous communications loop with the network stack initialized and a telnet session established for each port with standard out, in and standard error directed to the telnet session port. The test shall not exceed a maximum CPU load of 30% during test duration of 96 hours for Model 2070 -1E Module. The controller using Model -1C Module shall have a maximum CPU load of 10% for the above test and shall meet all test requirements as defined in Section 8.1.1 of the latest ATC Standard.

9.2.11 Diagnostic Acceptance Test (DAT)

The standard Caltrans DAT Program shall be provided resident in the 2070 Unit as the application program.

9.2.12 QPL or Purchasing Agency

Source and object Software shall be provided to the QPL or Purchasing Agency on both document listing and CD-ROM Memory. It shall provide user descriptions of test logic and reports. The Agency shall possess non- exclusive rights to this program suite.

9.2.13 Deliverables

9.2.13.1 Copies Delivery

Two copies of the following items will be provided to the purchasing AGENCY on a CD disk readable by a PC compatible computer.

1. Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, shall be specified and provided. Written documentation of addresses shall be in PDF form and will have the file name of “Memory Map.pdf”
2. Copies of the vendor kernel, platform drivers and OS-9 utility executable modules.

3. Copy of all provided written manuals in PDF form.
4. RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures shall have the file name of “Reflash Utility Procedures.pdf”.

9.2.13.2 Software Delivery

All Linux Software, except for loadable modules, shall be compliant to the GPL 2.0/3.0 license as published by the Free Software Foundation.

CHAPTER 9-SECTION 3
MODEL 2070-2 FIELD I/O MODULE (FI/O)

9.3.1 Model 2070-2E+ Module
The Model 2070-2E+ Model shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

9.3.2 Model 2070-2C+ Module
The Model 2070-2C+ Model shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

9.3.3 Field I/O Controller Unit (FCU)
The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. The FCU shall be provided with in-circuit re-programmability via a JTAG or BDM port.

9.3.4 Parallel Input Ports
The Parallel Input Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground. The pull-up resistance shall not be less than 10K or more than 50K Ohms.

9.3.4.1 Parallel Ouput Ports
The Parallel Output Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 Mega Ohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

9.3.4.2 Output Operation
Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a LOGIC "0" and retain that state until a new writing. The state of all output circuits at the time of POWER UP or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

9.3.5 Other Module Circuit Functions

9.3.5.1 Maximum Capacitive Load
A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

9.3.5.2 External WDT "Enable" Shunt/Toggle Switch
An External WDT "Enable" Shunt/Toggle Switch shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output 39 (Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to Set Output Command. When the shunt is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.3.5.3 Watchdog Circuit
An FCU Watchdog Circuit shall be provided. It shall be enabled by the Filed I/O firmware at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

9.3.5.4 One KHz Reference
A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

9.3.5.5 32 Bit Millisecond Counter
A 32-bit Millisecond Counter (MC) shall be provided for "time stamping." Each 1 KHz reference interrupt shall increment the MC.

9.3.5.6 Power Up
At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit.

9.3.5.7 Logic Switch
A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. An LED shall be provided on the module front panel labeled "SP3 ON". If LED light is ON, SP3 is active and available at C12S.

9.3.6 Serial Communications/Logic Circuitry

9.3.6.1 System Serial Port 5 (SP5) EIA 485 Signal
System Serial Port 5 (SP5) EIA 485 signal Lines shall enter the Field I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

9.3.6.2 System Serial Port 3 (SP3) EIA 485 Signal

System Serial Port 3 (SP3) EIA 485 signal lines shall enter the Field I/O Module and be isolated, converted back to EIA 485 and then routed to Connector C12S.

9.3.6.3 Linesync and Power Down Lines

Linesync and Power Down Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

9.3.6.4 CPU_Reset and Power Up

CPU_Reset and Power Up (SysReset) Lines shall be isolated and "OR'd" to form NReset. NReset shall be used to reset the FCU and other module devices. NReset shall also, be converted to EIA 485, and then routed to Connector C12S.

9.3.6.5 Module 2070-2C+

If the module is 2070-2C+, routing to FCU doesn't apply.

9.3.6.6 Internal Isolation

Isolation between internal +5DC / DCG#1 and +12 DC ISO/DCG#2 and +12 DC ISO shall be used for board power and external logic.

9.3.7 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU Module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer.

9.3.8 I/O Functions

9.3.8.1 Inputs

Input scanning shall begin at I0 (bit 0) and proceed to the highest input I63, ascending from lsb to msb in increasing input number. Each complete input scan shall finish within 100 μs. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 μs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 μs of the completion of the input scan.

9.3.8.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall

consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	**Enabled**
On and off filter values shall be set to	5
Transition monitoring	Disabled (Timestamps are not logged)

9.3.8.3 Outputs

Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF (Cases A & D), or an optional state synchronized with either phase of LINESYNC (Cases B & C). The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there are no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the Module Status Byte shall be updated to reflect the loss of communication from the CPU Module.

9.3.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module Field I/O frame protocol as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

9.3.8.4.1 Case A

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For optional half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON should remain

ON until otherwise configured. All outputs shall neither glitch nor change state unless configured to do so.

9.3.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - both the 0-1 and 1-0 transitions of the LINESYNC signal shall generate this interrupt. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($\geq$60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($\geq$500 consecutive millisecond interrupts).

9.3.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

For Transmission:

Generate the opening and closing flags
Generate the CRC value
Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
Provide zero-bit insertion

For Receiving:

Detect the opening and closing flags
Provide address comparison, generating an interrupt for messages addressed to the Field I/O Module, and ignoring messages not addressed to the Field I/O Module
Strip out inserted zeros
Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
Generate an interrupt if an abort sequence is received

9.3.8.7 Communication Processing

This task shall be to process the command messages received from the CPU Module, prepare, and start the response transmission. The response message transmission shall begin within 4 ms of the receipt of the last byte of the command message for all command message types.

Processing time for the Set Outputs command shall be less than 1.5ms. The FI/O shall be able to process 1000 Set Outputs command messages within 1.5 seconds, where each command toggles all outputs utilizing Case A and D as defined elsewhere in these specifications. Each output shall consist of a square wave with a 50% duty cycle and a time period of less than 3 ms.

9.3.8.8 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9.3.9 Data Communication Protocols

9.3.9.1 Communications Protocol

Protocol - All communications between the CPU Module and the Field I/O shall be SDLC-compatible command-response, support 0-bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communications and if the command frame is incomplete or there is an error, no Field FI/O response shall be transmitted. The number of bytes of a command or response is dependent upon the Field I/O Module identification.

9.3.9.1.1 Frame Types

The frame type shall be determined by the value of the first byte of the message. The command frames type values 112 – 127 ($70 - $7F) and associated response frame type values 240 – 255 ($F0 - $FF) are allocated for Manufacturer diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types

Module Command	I/0 Module Response	Description	Minimum Message Time	Maximum Message Time
0-43	128-171	Reserved for NEMA TS-2		
44-48	172-176	Reserved		
49	177	Request Module Status	250 µs	275 µs
50	178	**MC Management**	222.5 µs	237.5 µs
51	179	Configure Inputs	344.5 µs	6.8750 ms
52	180	Poll Raw Input Data	317.5 µs	320 µs
53	181	Poll Filtered Input Data	317.5 µs	320 µs
54	182	Poll Input Transition Buffer	300 µs	10.25 ms
55	183	**Set Outputs**	405 µs	410 µs
56	184	Configure Input Tracking	340 µs	10.25 ms
57	185	Configure Complex Outputs	340 µs	6.875 ms
58	186	Reserved / Optional (Configure Watchdog)	222.5 µs	222.5 µs
59	187	Controller Identification	222.5 µs	222.5 µs
60	188	I/O Module Identification	222.5 µs	222.5 µs
61-62	189-190	Reserved (see Section 9.3.9.1.2)	---	---
63	191	Poll variable length raw input (see Section 9.3.9.1.2)	317.5 µs	320 µs
64	192	Variable length command outputs	405 µs	410 µs
65	193	Reserved (see Section 9.3.9.1.2)	---	---
67	195	Reserved (see Section 9.3.9.1.2)	---	---
68-111	196-239	Reserved	---	---
112-127	240-255	Manufacturer Diagnostics	---	---

9.3.9.1.2 ITS Cabinet Monitor

Messages 61/189, and 62/190, and 65/193 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (See Chapter 3). Message 63 /191 shall be the same as Message 52/180 except Byte 2 of Message 63 response shall denote the following number of input data bytes:

Message 64/192 shall be the same as Message 55/183 except Byte 2 of the Message 64 Command shall denote the number of output data bytes plus the following output control bytes:

9.3.9.2 Request Module Status

The Command shall be used to request FI/O Module status information response.

Command/response frames are as follows:

Request Module Status Command

Description	Msb							Lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	Msb							Lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

9.3.9.2.1 Status Bits

The response Status Bits are defined as follows:

- P - Indicates FI/O hardware reset
- E - Indicates a communications loss of greater than 2 seconds
- M - Indicates an error with the MC interrupt
- L - Indicates an error in the LINESYNC
- W - Indicates that the FI/O has been reset by the Watchdog
- R - Indicates that the SCC Receive Error count byte has rolled over
- T - Indicates that the SCC Transmit Error count byte has rolled over
- K - Indicates the Datakey has failed or is not present

9.3.9.2.2 Request Module Status

Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When an SCC error count rolls over (255 - 0), its corresponding roll-over flag shall be set.

9.3.9.3 MC Management

MC Management frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

MC Management Command

Description	msb							Lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	x	x	x	x	x	x	x	Byte 2
New Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3
New Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 4
New Timestamp LSB	x	x	x	x	x	x	x	x	Byte 5

MC Management Response

Description	msb							Lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

9.3.9.4 Configure Inputs Command

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb							Lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response

Description	msb							Lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on error

9.3.9.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	Msb							lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response (2070-2A)

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Raw Input Data Response (2070-8 via 2070-2B)

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

9.3.9.6 Poll Filtered Input Data

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	Msb							lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response (2070-2A)

Description	msb							lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Filter Input Data Response (2070-8 via 2070-2C+)

Description	msb							lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

9.3.9.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	msb							lsb	Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2

Input Transition Buffer Response

Description	msb							lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2
Number of Entries (n)	x	x	x	x	x	x	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(n-1)+7
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+8
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+9
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+10
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+11

The entry types are depicted as follows:

Input Transition Entry

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	x	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

MC Rollover Entry

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

9.3.9.7.1 Active Input

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

- S Indicates the state of the input after the transition
- C Indicates the 255 entry buffer limit has been exceeded
- F Indicates the transition buffer limit has been exceeded
- G Indicates the requested block number is out of monotonic increment sequence
- E Same block number requested, E is set in response

9.3.9.7.2 Block Number Byte

The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

9.3.9.8 Set Outputs

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to “1”. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set to “1”. Loss of LINESYNC reference shall also be indicated in Module Status Response Frame. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command (2070-2A)

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O63 Data	x	x	x	x	x	x	x	x	Bytes 3 to 9
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 10
Outputs O8 to O63 Control	x	x	x	x	x	x	x	x	Bytes 11 to 17

Set Outputs Command (2070-8 via 2070-2B)

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O103 Data	x	x	x	x	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 15
Outputs O8 to O103 Control	x	x	x	x	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	Msb							lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

9.3.9.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to '1' and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb							lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	msb							lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 6

9.3.9.9.1 Definitions are as follows:

E '1' - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

9.3.9.9.2 Timestamp Value

The timestamp value shall be sampled prior to the response frame.

9.3.9.9.3 Outputs Tracks Inputs

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

9.3.9.9.4 Number of Item

The "Number of Item" field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message "V" bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

9.3.9.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	x	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	x	x	x	x	x	Byte 4
Timestamp (NLSB)	x	x	x	x	x	x	x	x	Byte 5
Timestamp (LSB)	x	x	x	x	x	x	x	x	Byte 6

9.3.9.10.1 Bit Field

The bit fields of the command frame are defined as follows:

E	'1'	-	enable complex output function for this output
	'0'	-	disable complex output function for this output
J	'1'	-	During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
	'0'	-	During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.
			Output Number - 7-bit output number identifying outputs
			Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.
			Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.
F	'1'	-	The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
	'0'	-	The trigger or gate shall be derived from the raw input.
R	'1'	-	For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
	'0'	-	For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
			Input Number - 7-bit input number identifying inputs 0 Up.
P	'1'	-	The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
	'0'	-	The output is configured for continuous oscillation.
W	'1'	-	It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
	'0'	-	Operation shall begin within 2 ms of the command receipt.
G	'1'	-	Operation shall be gated active by the specified input.
	'0'	-	Gating is inactive.
L	'1'	-	The LINESYNC based clock shall be used for the time ticks.
	'0'	-	The MC shall be used for the time ticks.
V	'1'	-	Indicates maximum number of configurable outputs is exceeded.
	'0'	-	No error
			Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

9.3.9.10.2 Controlling Input Signals

Controlling input signals shall be sampled at least once per millisecond.

9.3.9.10.3 Number of Items

The "Number of Items" field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message "V" bit shall be set to 1. If an invalid output or input number (the "G" or "W" bits being set to 1 is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The "G" bit (gating) set to 1 takes precedence over the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a Complex Output is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation ("G" bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

9.3.9.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb							lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	x	x	x	x	x	Byte 2

Configure Watchdog Response

Description	msb							lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

9.3.9.11.1 Timeout Value

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

9.3.9.11.2 Watchdog Timeout Value

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the "Y" bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

9.3.9.12 Controller Identification

This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit "K" shall be set and no interrogation shall take place. If an error occurs during the interrogation, Bit "K" shall be set. If "K" bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

Controller Identification Command

Description	msb							lsb	Byte Number
(Type Number = 59)	0	0	1	1	1	0	1	1	Byte 1

Controller Identication Response

Description	msb							lsb	Byte Number
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Byte 3 to 130

9.3.9.13 Module Identification

The Field I/O Identification command frame shall be used to request the FI/O Identification. A value Response of "1" for the 2070-2A, "2" for the 2070-8, and "3" for 2070-2N. Response values 32 to 40 are reserved for the ITS Cabinet (See Chapter 3). The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb							lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

Description	msb							lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
FI/O ID byte	x	x	x	x	x	x	x	x	Byte 2

CHAPTER 9-SECTION 4
MODEL 2070-3 FRONT PANEL ASSEMBLY (FPA)

9.4.1 Model 2070-3 Front Panel Assembly

The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connectors (DB9 and RJ-45), CPU_ACTIVE LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A- FPA controller, two keyboards, AUX switch, alarm bell, C50S, C50J & Display A.

OPTION 3A+- FPA controller, two keyboards, AUX switch, alarm bell, C50J, NET & Display A.

OPTION 3B - FPA controller, two keyboards, AUX switch, alarm bell, C50S, C50J & Display B.

OPTION 3B+ - FPA controller, two keyboards, AUX switch, alarm bell, C50J, NET & Display B.

OPTION 3C - System Serial Port 6 Lines, isolated and vectored to Connector C60P.

OPTION 3D– FPA controller, two keyboards, AUX switch, alarm bell, C50S, C50J & Display D.

OPTION 3D+– FPA controller, two keyboards, AUX switch, alarm bell, C50J, NET & Display D.

9.4.2 Keyboards

Two Keyboards shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 1.764 ounce and 3.527 ounce and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

9.4.3 CPU_ACTIVE LED Indicator

The cathode of the CPU_ACTIVE LED Indicator shall be electrically connected to the CPU_ACTIVE signal and shall be pulled up to +5 VDC.

9.4.4 Display Liquid Crystal Display (LCD)

The Display shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with minimum character dimensions of 0.197 in. wide by 0.411 in. high and an electro-luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 0.104 in. wide by 0.167 in. high and either LED or EL backlight. Display D shall have 16 lines of 40 characters each with minimum dimensions of 0.104 in wide by 0.167 in high and either LED or EL backlight.

9.4.4.1 Characters and Angles of Liquid Crystal Display (LCD)

Each character shall be composed of a 5x7 dot matrix with a underline row or a 5x8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90º) viewing, ±35º vertical, ±45º horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

9.4.4.2 Backlight

The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

9.4.4.3 Cursor Display

Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

9.4.5 FPA Controller

The FPA Controller shall function as the Front Panel Device controller interfacing with the CPU Module.

9.4.5.1 FPA Reset

An FPA Reset Switch shall be provided on the Assembly PCB. The momentary Control switch shall be logic OR'd with the CPU Reset Line, producing a FPA Reset Output. Upon FPA Reset being active or receipt of a valid Soft Reset display command, the following shall occur:

Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.

Each special character shall be set to ASCII SPC (space).

The tab stops shall be set to columns 9, 17, 25, and 33.

The backlight timeout value shall be set to 6 (60 seconds).

The backlight shall be extinguished.

The display shall be cleared (all ASCII SPC).

The cursor display shall be turn OFF

The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware Reset Button is pushed. The string is “ESC [PU”, hex value “1B 5B 50 55”.

9.4.5.2 Key Press

When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

9.4.5.3 Auto Repeat

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second and shall terminate when the key is released, or another key is pressed.

9.4.5.4 AUX

When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

9.4.5.5 Controller Circuitry

The controller circuitry shall be capable of composing and storing eight special graphical characters on command and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication command codes on Page A9-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic ‘1’ shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

9.4.5.6 Character Overwrite

Character Overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one-character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

9.4.5.7 Auto Wrap

Auto-Wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

9.4.5.8 Cursor Positioning

Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

9.4.5.9 Blinking Characters

Blinking characters shall be supported and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

9.4.5.10 Tab Stops

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

Tab stops shall be set based only upon the column (horizontal) position of the cursor; the row position shall be ignored. Each tab that is set shall apply to all rows of the display. In this way, tabs shall operate similarly to a typewriter or line printer. For example, if the cursor is positioned at column 21, row 3 when a Set Tab Stop command (ESC H) is received, a tab stop is placed at column 21 and applies to every row of the display. If the cursor is then positioned to column 21, row 5, and a Clear Tab Stop command (ESC[0g) is received, the tab stop on column 21 is removed and there will be no tab stop on any row of the display at that column position.

9.4.5.11 Auto Scroll

Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

9.4.5.12 Displayable Characters

Displayable characters shall be refreshed at least 20 times per second.

9.4.5.13 Display Back Light Illuminate

The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

9.4.5.14 Command Codes

The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

   Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.
   P1: Ordered and numbered parameter. One of listed known parameters with a specified order and number (Continues with P2, P3, etc.)
   Px: Display column number (1-40), using one ASCII character per digit without leading zero.
   Py: Display line (1-4) one ASCII character
   ...: Continue the list in the same fashion

2. Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

3. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

4. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

9.4.5.15 Controller Circuit

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.
C50 Enable Function
C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

9.4.6 Front Panel

The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB at a distance of 4 feet, for 350±100 ms upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

CHAPTER 9-SECTION 5
MODEL 2070-4 POWER SUPPLY MODULE

9.5.1 Model 2070-4 Power Supply Module
The Model 2070-4 Power Supply Module shall be independent, self-contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

9.5.2 On/Off Power Switch
An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC and 12 VDC are within 5% and of their nominal levels.

9.5.3 Input Protection
Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

9.5.4 +5 VDC Standby Power
+5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 to +2 VDC for over 600 minutes.

9.5.5 Monitor Circuitry
Monitor Circuitry shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

9.5.5.1 AC Fail/Power Down Output Lines
The AC Fail/Power Down Output Lines shall go Low (ground true) immediately upon Power Failure. The Lines shall transition to High immediately after both Power Restoration and supply is fully recovered. The Lines shall be driven separately. The Sysreset/Powerup Output Lines shall transition to Low 525 +/-25 ms after AC Fail/Power Down transition to Low. The Lines shall transition to HIGH 225 +/- 25 ms after both Power Restoration and the supply is fully recovered (e.g. after +5 VDC is within the range as specified in section 9.5.6). The Lines shall be driven separately.

The AC Fail Output line shall transition to High within 300 ms after a Cold Start of the power supply. Cold Start occurs when the power supply has been offline for 3 minutes or longer.

9.5.5.2 Monitor Circuitry
The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

9.5.5.3 60 Hz Square Wave Linesync
The 60 Hz Square Wave Linesync signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ± 1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

9.5.5.4 Linesync
The Linesync shall continue until Sysreset transitions Low and begin then Sysreset transitions High.

9.5.6 Power Supply Requirements

Voltage	Minimum Load	Maximum Load	Load Reg.	Line Reg.	Ripple & Noise
+5 VDC	0.0 Amp	10.0 Amp	± 5%	± 1%	50mV P-P
+12 VDC Serial	0.0 Amp	0.5 Amp	± 5%	± 1%	50mV P-P
-12 VDC Serial	0.0 Amp	0.5 Amp	± 5%	± 1%	50mV P-P
+12 VDC	0.0 Amp	1.0 Amp	± 5%	± 1%	50mV P-P

9.5.6.1 Line / Load Regulation
The Power Supply Module shall meet Line/Load Regulation for input voltage range of 90 to 135 VAC, minimum and maximum loads called out in the table including ripple and noise.

9.5.6.2 Efficiency
70 % minimum.

9.5.6.3 Ripple & noise
Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater.

9.5.6.4 Voltage Overshoot
No greater than 5 %, all outputs.

9.5.6.5 Over voltage Protection
130% Vout for all outputs.

9.5.6.6 Circuit Protection
Automatic recovery upon removal of fault.

9.5.6.7 Inrush Current
Cold Start Inrush shall be less than 25 Amperes at 115VAC.

9.5.6.8 Transient response

Output voltage back to within 1% in less than 500 μs on a 50% Load change. Peak transient not to exceed 5%.

9.5.6.9 Holdup Time

The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

9.5.6.10 Remote Sense

+5 VDC compensates 250 mV total line drop. Open sense load protection required.

9.5.6.11 Power Factor Correction

The Model 2070-4 Power Supply shall include power factor correction circuitry resulting in a minimum full load power factor of 0.96.

CHAPTER 9-SECTION 6
MODEL 2070 UNIT CHASSIS

9.6.1 General

The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the backplane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.6.2 Serial Motherboard

Serial Motherboard shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one-layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the Motherboard PCB (provide strain relief). Test points shall be provided on the FPA side of the Motherboard for PS2 lines. A wiring harness FP shall be provided, linking the Motherboard with the FPA.

CHAPTER 9-SECTION 7
MODEL 2070LX + UNIT CHASSIS

9.7.1 General
The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the backplane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.7.2 Serial Motherboard
Serial Motherboard shall function as support for its connectors, A1 to A8 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one-layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the Motherboard PCB (provide strain relief). Test points shall be provided on the FPA side of the Motherboard for PS2 lines. A wiring harness FP shall be provided, linking the Motherboard with the FPA.

9.7.3 Model 2070LX + Unit Chassis
The Model 2070-LX+ Unit Chassis shall be provided with ethernet network lines as shown in A9-14 and shall contain slots A6, 7 and 8.

The network switch ports resident in the Model 2070-LAN and inserted slot A8 shall be routed to the NetP5 ports of slots A1, A2, A4, A5, A6 and A7.

CHAPTER 9-SECTION 8
MODEL 2070 UNIT DETAILS

CHAPTER 10
MODEL 2070 PERIPHERAL EQUIPMENT SPECIFICATIONS

CHAPTER 10-SECTION 1
MODEL 2070-6 A & B, AE & BE ASYNC/MODEM SERIAL COMMUNICATION MODULES

10.1.1 Fuse Isolation

A fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use. Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse allowed.

10.1.2 Half & Full Duplex Switch

A switch shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.1.3 Circuits

Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard.

Line drivers/receivers shall be socket or surface mounted.

The 2070-6x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.1.4 Modem

Each circuit shall have a common power independent Modem with the following requirements:

Modulation: Phase coherent frequency shift keying (FSK).

Data Format: Asynchronous, serial by bit.

Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive), MARK and SPACE: ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz &2 .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.

Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A, 3.4 KHz for 2070-6AE, 14.7 KHz for 2070-6B and 28.8 KHz for 2070-6BE) continuous or switch selectable.

Receiver Input Sensitivity: 0 to -40 dB.

Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20dB/octave, minimum active attenuation for all frequencies outside the operating band.

Clear-to-Send (CTS) Delay: 11 ±3 ms.

Receive Line Signal Detect Time: 8 ±2 ms mark frequency.

Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

Soft Carrier Turn Off Time: 10 ±2 ms. When the RTS is unasserted; the carrier shall turn off or go to soft carrier frequency.

Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.

Transmit Noise: Less than -50 dB across 600-Ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.

Modem interface: EIA-232 Standards.

Frequencies and Data Rates:

Model	**Mark Hz**	**Space Hz**	**Soft Carrier Hz**	**Data Rate bps**
2070-6A	1200	2200	900	300 - 1200
2070-6AE	2400	4400	1800	300 - 2400
2070-6B	11200	17600	7800	300 - 9600
2070-6BE	19200	38400	13800	300 - 19200

10.1.5 Enable/Disable Feature

The 2070-6x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules**.**

10.1.6 Hot Swappable

The 2070-6x module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

CHAPTER 10-SECTION 2
MODEL 2070-7A & 7B ASYNC / SYNC SERIAL COMM MODULE

10.2.1 Circuits
Two opto-isolated independent circuits designated circuits #1 (Channel 1) and circuits #2 (Channel 2), shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (circuits #1 to SP1 [or SP3] and Connector C21S and circuits #2 to SP2 [or SP4] and Connector C22S). Line drivers/receivers shall be socket or surface mounted.

The 2070-7x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.2.2 2070 -7A
Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

10.2.3 2070 - 7B
Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

10.2.4 LED Indicator
Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled according to function.

10.2.5 Enable/Disable Features
The 2070-7x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

The 2070-7x modules shall provide circuitry to manually disable Channel 1. When Channel 1 is manually disable, the "Ch. A Disable" LED indicator shall be turn ON**.**

10.2.6 Hot Swappable
The 2070-7x module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

CHAPTER 10-SECTION 3
MODEL 2070-6D FIBER OPTIC MODULE

10.3.1 Model 2070-6D Fiber Optics Module
The Model 2070-6D Fiber Optics Module shall provide an RS232/485 Asynchronous communications channel. The FO Module shall be a Plug-in Card style version for the 2070 Controller. The Model 2070-6D Fiber Optics Module (FO Module) shall operate over Single mode Fiber.

10.3.2 Mechanical/Electrical Requirements.
The Plug-in Card FO Module shall have a protective cover or enclosure.

The FO Modules card edge connector shall be fully compatible with the 2070 Controller's Modem card slot.

The Auxiliary Data port shall be a RJ45 connector.

The Serial Port shall be a RJ45 connector.

All DIP Switches shall be accessed externally without disassembly of the FO Module.

The FO Module shall be powered direct from the 2070 Controller's edge connector.

All electro/optical communications circuitry shall be implemented using digital electronics utilizing packetizing techniques, no analog circuitry or adjustable potentiometers is allowed.

10.3.3 FO Module Requirements
All Electro Optics shall be physically protected from external damage and contamination by isolating them from the FO Modules Optical Ports by means of internal replaceable mini patch-cords that connect between the Electro Optics and the Optical Bulkhead Adapters (FO Modules Optical Ports).

The FO Modules Optical Ports (Bulkhead Adapters) shall be metal and shall be ST style and interchangeable with SC and FC style connectors when required.

The Plug-in optical FO Module shall provide Optical Continuity between other FO Modules on either side should external power fail.

10.3.3.1 Network Topologies
The FO Module shall be capable of operating on Single Mode Fiber in all the following Switch Selectable Topologies:

Self-Healing Fault Tolerant Dual Counter Rotating Rings.
Defined as 2 Fiber Rings (closed loop cable ring), one fiber transmitting data clockwise, the other fiber anti-clockwise. Every FO Module will have 4 fibers attached to it, the incoming cable utilizes R1/T2 fiber pair and the outgoing cable utilizes T1/R2 fiber pair. Should an optical communications failure occur, such as a single or dual fiber cut or FO Module failure, the system

will automatically fold back on both sides of the failure point to form a new ring and restore communications. The system shall automatically restore when there is no longer a failure point.

Single Ring
Defined as a Single Fiber Ring (closed loop), only one fiber transmitting data clockwise. Every FO Module will have 2 fibers attached to it R1 & T1, the incoming cable utilizes R1 fiber and the outgoing cable utilizes the T1 fiber. Each fiber starts as transmit and ends as receive.

Daisy Chain
Defined as an "open ended chain of FO Modules". The designated Master, Auxiliary Master and Slave FO Modules may be placed anywhere in the Daisy Chain, i.e., at the beginning, at the end or anywhere in between.

The FO Module shall be immune to optical overloads thus requiring no optical attenuators.

The FO Modules optical output level shall be non-adjustable.

10.3.3.2 Modes of Operation
The FO Module shall support the following modes of operation:

Master
When the optical FO Module is set as a Master, the FO Module supervises the Slave FO Modules and provides an asynchronous, bi-directional communications channel between the Master and the Slave FO Modules.

Auxiliary Master, Co- or Remote Located Master (Disaster Recovery)
When set as an Auxiliary Master, the optical FO Module will monitor optical data transmissions from the Master, should the Master fail, the Auxiliary Master will automatically take over as a temporary Master. Control of the ring will be automatically transferred back to any optical FO Module that is designated as a Master.

Slave
When the optical FO Module is set as a Slave, the FO Module will provide repeater, drop and insert capabilities between the data ports and the optical transport layer.

Display
All FO Modules shall have a Dual Seven Segment Display that graphically indicates the switching status of the transport layer of the fiber system. Switch status information shall graphically show:

Normal Operation
Dual Ring Operation
Single Ring Operation
Daisy Chain Operation
All Optical Routing Conditions
Separate LOS Alarm indication for R1 or R2

10.3.3.3 Fiber Identification

The FO Module shall be capable of Fiber Identification by means of indicating numeral 1 or 2 on the Dual Seven Segment Display to identify which circuit the fiber belongs to.

10.3.3.4 Auxiliary Data Port

The FO Module shall have an Auxiliary Data Port with the following capabilities:

The Auxiliary Data Port shall be capable of being switched to operate as a **DCE** in parallel with the Card Edge Port; communications shall originate to and from the fiber.

The Auxiliary Data Port shall be capable of being switched to operate as a **DTE**. This permits any host attached to the card edge port to appear at the Auxiliary port as a DTE with full handshaking; communications shall originate from the card edge port to and from the auxiliary port and the fiber.

The Auxiliary Ports Carrier Detect (CD) shall be capable of being switched to operate in the following modes:

The Auxiliary Data Port is designed to emulate FSK FO Module handshaking

The Card Edge (EIA-485), Auxiliary Data Port (EIA-232) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200, 2400, 9600, 19.2Kbp/s, 38.4Kbt/s, 56Kbt/s and 115.2Kbp/s.

The RTS/CTS handshaking function shall be switch selectable:

Off position allows the FO Module to stream transmit data without RTS handshaking. On position requires RTS to be asserted to enable data transmission.

The Card edge and Auxiliary Data Ports shall have a switch selectable RTS to CTS Delay of 0ms and 8ms.

10.3.3.5 Anti-Streaming

The FO Module shall include a switch selectable Anti-Streaming (anti-babbling) logic control over electrical to optical signal transmission with a time out changeable by the user, the time-outs shall be switch selectable from 2, 4, 8, 16, 32 & 64 seconds, all times are additive to a max of 126 seconds.

The Anti-Streaming logic shall detect the presence of an RTS signal from the attached device. Should the transmission time from the attached device exceed the selected time, the Anti-Streaming logic will cause the CTS control line to go low, this signals the attached device to stop the transmitting data. At the same time the transmission path from the data port to the optical ring will be disconnected. The circuit will automatically reset should RTS go low and data stops babbling.

When the Anti-Streaming logic has automatically disabled the port, it shall then turn on the Anti-Streaming Alarm (LED), this alarm is latched ON until manually reset.

10.3.4 Electro Optical Requirements

The FO Module Optical Transmitting Device shall use a 1310nm single-mode laser.

Optical Budget

The FO Module shall support a minimum of 20dB Optical budget with a maximum of 1×10^{-9} Bit Error Rate (BER).

M.T.B.F.

Shall be in excess of 100, 000 Hrs.

Optical Ports

Optical Ports shall be Metal Bulkheads, ST style, optional SC or FC.

Data Interfaces

Card Edge	EIA-485
Front Panel Serial Port	EIA-232 (RJ45 EIA 561 Pin Out)
Auxiliary Data Port	EIA-232 (RJ45 EIA 561 Pin Out)

Switch Selections are as follows:

Battery	ON or OFF
Master or Slave	Selection
Auxiliary Master	ON or OFF
Ring Topologies	Single Ring Dual Counter Rotating Ring (Self-Healing) Daisy Chain
RS232 or RS422	Selection
Baud Rates	1200, 2400, 9600, 38400, 5760, 115200 bps
Parity Selections	None, Odd, Even
RTS/CTS Handshaking	ON or OFF
RTS to CTS Delay Timing	0 or 8ms
Anti-Streaming	ON or OFF
Anti-Streaming Delay Times	2, 4, 8, 16, 32 & 64 seconds or any addition.
Auxiliary Port	DCE or DTE Selection

Indicators shall be Super Bright LED

TX DATA	Green	Transmit EIA-232/485 Data
RX DATA	Green	Transmit EIA-232/485 Data
ANTI- STRM	Red	Anti- Streaming
RING STATUS DISPLAY	Red	Dual Seven Segment Display
PWR Fail	Red	Dual Seven Segment Display

10.3.5 Form Factor

See A10-3 for Details

10.3.6 Power Requirements

The power requirements of the FO Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in these specifications.

10.3.7 Environmental

The FO Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 4
MODEL 2070-FX NETWORK COMMUNICATIONS MODULE

10.4.1 Model 2070-Fx Network Module

The Model 2070-Fx Module shall provide 5 ports for Network Communications to and from the Model 2070 Controller.

An integrated 5-Port Store-and-Forward Network Switch shall be used as the core for the Model 2070-Fx Module. A network port shall be used to route Ethernet Traffic across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively. Two network ports shall be brought to RJ-45 Connectors on the Front Panel and two network ports shall route to 100Base-FX modules.

The 10/100Base-FX Module outputs shall be optically linked through short patch cords (Mini Patch Cords) to ST connectors on the Front Panel. The 10/100Base-FX modules shall operate over Single Mode Fiber.

The Model 2070-Fx Module shall be a Plug-in Card style version for the 2070 Controller.

10.4.2 Mechanical/Electrical Requirements.

The Model 2070-Fx Modules card edge connector shall be fully compatible with the 2070 Controller's Motherboard Ax Card Slots.

The Model 2070-Fx Module shall be powered direct from the 2070 Controller's edge connector.

10.4.3 Model 2070-Fx Module Requirements

The 10/100Base-FX modules of the Model 2070-Fx Module shall be connected by means of internal replaceable Mini Patch-Cords that connects between the 10/100Base-FX modules and the Optical Bulkhead Adapters (Model 2070-Fx Module Ports).

Model 2070-Fx Modules Optical Ports (Bulkhead Adapters) shall be metal and shall be ST style and interchangeable with SC and FC style connectors when required.

10.4.4 Network Standards

The Model 2070-Fx Module shall meet the IEEE802.3 10Base-T, IEEE 802.3u, IEEE 802.3x, 100Base-TX, and 100Base-FX Standards.

The Model 2070-Fx Module shall have 10/100Base-TX auto-negotiation on all RJ-45 ports and Auto-negotiation 10/100Mbps connection speed and Half/Full-Duplex mode on all 10/100Baset-TX ports.

The Model 2070-Fx Module shall have MDIX for all 10/100Baset-TX ports.

10.4.5 Modes of Operation

The Model 2070-Fx Module shall have Half/Full-Duplex mode selection on the fiber ports.

10.4.6 Network Media Support

The Model 2070-Fx Module shall be configured as a Multiple Channel Media Converter to route network traffic between the Model 2070 CPU, Two RJ-45 Front Panel Connectors and the two 10/100Base-FX Front Panel Ports.

The Model 2070-Fx Module shall support the following Media:

100Base-FX: Single-Mode fiber optic cable 9/125 μm.

100Baset-TX: Cat. 5, EIA/TIA-568 100-Ohm UTP cable.

10.4.7 Electro Optical Requirements

The 10/100Base-FX Modules shall use a 1300nm Single Mode Lasers.

M.T.B.F.

Shall be in excess of 100, 000 Hrs.

Optical Ports

Optical Ports shall be Metal Bulkheads, ST style, optional SC or FC.

10.4.8 Form Factor

See A10-4 for Details

10.4.9 Power Requirements

The power requirements of the 2070-Fx Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in these specifications.

10.4.10 Environmental

The 2070-Fx Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 5
MODEL 2070-6W WIRELESS MODEM COMM MODULE

10.5.1 Model 2070-6W Wireless Modem

The Model 2070-6W Wireless Modem shall provide two EIA-485/ EIA-232 Asynchronous communications channels. The Model 2070-6W Wireless Modem shall be a 2070 plug-in module with EIA-232 activity LEDs on the front edge. The Model 2070-6W Wireless Modem shall convert EIA-485 data to frequency hopping spread spectrum data.

10.5.2 Circuits

Two circuits, designated Circuits #1 and Circuits #2, shall be provided. Both circuits functions shall be identical, except for Circuit #1 which shall be routed to a Spread Spectrum Radio and Circuit #2 shall route directly to the front panel's DB-9 connector. Each circuit shall provide full isolation from the Model 2070 Motherboard.

Line drivers/receivers shall be socket or surface mounted.

The Model 2070-6W Wireless Modem's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.5.3 Mechanical/Electrical Requirements

The Model 2070-6W Wireless Modem shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-6W Wireless Modem shall be provided with LED indicators for as shown in detail A10-5 of these specifications.

The User Serial port shall be a DB9 Female connector accessible from the front and shall be used to configure the Spread Spectrum Radio and as Serial Port Com2.

The Model 2070-6W Wireless Modem shall be powered direct from the 2070 Controller's edge connector.

The Model 2070-6W Wireless Modem shall have a MTBF of over 60,000 hours.

10.5.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200 bps, 2400 bps, 9600 bps, 19.2 Kbps, 38.4 Kbps, 56 Kbps and 115.2 Kbps.

10.5.5 Local Mode

The Model 2070-6W Wireless Modem shall be provided with a switch allowing the user to switch Com 2 into local mode. Local mode shall allow the user to perform modem configuration on the Spread Spectrum Radio. On non-local mode, Com 2 shall meet the requirements as specified for the Model 2070-7A Module as specified elsewhere in these specifications.

10.5.6 Spread Spectrum Radio

The Model 2070-6W Wireless Modem shall meet the following Spread Spectrum Radio requirements:

Frequency Range	902-928 MHz
Output Power	100mW to1000mW
Software Programmable	Yes
Min Hop Patterns	Based on Network Address, > 4 Million
Number of RF Channels	90
RF Channel Spacing	280KHs
Error Checking	32Bit-CRC
Encryption	128 Bit, AES Encryption
Receiver Sensitivity/BER	-108dBm @ 10-6 BER
System Gain	36dBm
Antenna Port	RP TNC-F
Certification	FCC Approved
Operation Mode	Transceiver
Error Correction	Forward Error Correction
System Configuration	Point-to-Point, Point-to-Multipoint

10.5.7 Modem Configuration

The Model 2070-6W shall be configurable as a master, repeater or slave using the AT command set.

The modems shall have the default configuration as set as a slave with the following S- Register Parameters (AT&V):

&F2			
E1 DCD &C1 DTR &D0 Handshaking &K0 DSR &S1			
Operating Mode	S101=2	Serial Baud Rate	S102=7
Wireless Link Rate	S103=2	Network Address	S104=1234567890
Unit Address	S105=2	Static Mask	S107=0

Output Power (dBm)	S108=30	Output Power (dBm)	S108=30
Packet Retransmissions	S113=5	Data Format	S110=1
Repeat Interval	S115=3	Character Timeout, ms	S116=2
Average RSSI value (dBm)	S123=-255	Destination Address	S140=1
Serial Channel Mode	S142=0	Protocol Type	S217=0
Roaming	S118=1	Fast Sync Timeout, hops	S151=100
Sleep Mode	S143=0	Sync mode	S150=0
Network Type	S133=0	Address Tag	S153=0
Sync Timeout	S248=512	FEC Mode	S158=0

10.5.8 Data Interfaces

Channel 1 and 2 Model 2070 Card Edge Connector

User Serial Port EIA-232 (DB9 Female)

10.5.9 LED Indicators

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

Multiple Mini-LEDs indicating Field Strength.

10.5.10 Power Requirements

The power requirements of the Model 2070-6W Wireless Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specification.

10.5.11 Environmental

The Model 2070-6W Wireless Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.5.12 Form Factor

See A10-5 Details

CHAPTER 10-SECTION 6
MODEL 2070-9A, B & E FSK/DIAL-UP MODEM COMM MODULES

10.6.1 2070-9A, B & E Modem

The Model 2070-9x Modem shall consist of a Dial-Up and an FSK Modem. The 9x Modem Module shall be a Plug-in Card style version for the 2070 Controller.

10.6.2 Dial-Up Modem

The Dial-Up Modem shall consist of a 33.6Kbps dial-up modem meeting the V.34 AT Command set standard. The Modem shall contain two RJ-11 connectors, one designated as the Line and the second as Phone. An internal speaker shall be provided as an indicator for phone call progress. The speaker shall be controlled through AT standard commands. Front Panel LED indicators shall also be provided as shown in the A10-6 of these specifications.

10.6.2.1 Modem default configuration

The Dial-Up Modem shall contain the following default configurations:
ACTIVE PROFILE:
B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:138
S08:002	S48:007
S09:006	S95:000
S10:014	

STORED PROFILE 0:
B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0

S00:001	S12:050
S02:043	S18:000
S06:002	S36:007
S07:050	S40:104
S08:002	S41:195
S09:006	S46:138
S10:014	S95:000
S11:095	

Profile 0 should be configured as shown above and default as the active profile on wake up. Factory default shall wake up at 2400 Baud, Parity 8, N, 1 and no handshaking.

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Lock
2	"SMART Modem DB-9 Aux" Sel	DTE	DCE
3	RTS Overide	Normal	RTS High
4	"Modem /DB9 DTE Serial" Sel	Modem	DB9-DTE

All switches shall be OPEN position as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity.

10.6.2.2 Modulation

The Dial-Up Modem shall use Quadrature Amplitude Modulation and Operate within the following frequencies:

Data Carrier 1800 ± 0.5 Hz
Calling Tone 1300 ± 10 Hz
Answering Tone 2100 ± 15 Hz

The Modem shall have Receiver Frequency Tolerance of ± 14 Hz

10.6.2.3 Modem Standards

The Dial-Up Modem shall be ITU V.90, V.34 and Rockwell V.FC compatible. It shall meet the standards:

V.90, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, V.21, Bell 212, Bell 103, V.33, V.17, V.29, V.27 ter, and V.21 Channel 2.

10.6.2.4 Data Rates

The Dial-Up Modem shall support the following data rates:

33.6Kbps, 31.3Kbps, 28.8Kpbs, 26.4Kbps, 24.0Kbps, 21.6Kbps, 19.2Kbps, 16.8Kbps, 14.4Kbps, 12.0Kbps, 9.6Kpbs, 7.2Kpbs, 4.8Kpbs, 2.4Kpbs, 1.2Kpbs, and 300 baud.

The Modem shall automatically select the best operating speed as indicated in Section 10.6.2.1 of these specifications.

10.6.2.5 Error Correction & Data Compression
The Modem shall use V.42 LAPM, MNP2-4 and MNP 10 for error correction and V.42 Bis, MNP 5 for Data Compression.

10.6.2.6 Tx/Rx Power Level
The transmit level shall be fixed at -11± 2 dB and the receiver shall have a S/N Ratio of -26 dB with a Dynamic Range of 12 dBm to -42 dBm.

The Ring detect Sensitivity shall be 38 VRMS.

10.6.2.7 Line Interface
The Dial-Up Modem shall have a Ring Equivalent of 1 Bel and a terminating Impedance of 600 Ohms. It shall have return loss of better than 14 dB.

10.6.3 FSK Modem

10.6.3.1 Fused Isolated +5 VDC
eA fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use. Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Reset-able Fuse allowed.

10.6.3.2 Half & Full Duplex Switch
A switch on for FSK modem shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.6.3.3 Modem
The FSK modem circuit shall have meet the requirements as listed in Section 10.1.4 for the corresponding match (6A, 6B and 6BE).

10.6.3.4 Enable/Disable Feature
The FSK modem shall provide circuitry to disable Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules**.**

10.6.4 Circuits
Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard.

Line drivers/receivers shall be socket or surface mounted.

The 2070-9x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.6.5 Hot Swappable

The 2070-9x module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

10.6.6 Power Requirements

The power requirements of the Model 2070-9x Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in these specifications.

10.6.7 Environmental

The Model 2070-9x Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.6.8 Form Factor

See A10-6 for Details

CHAPTER 10-SECTION 7
MODEL 2070-6E SERIAL 2 NETWORK COMM MODULE

10.7.1 Model 2070-6E Serial 2 Network Module

The Model 2070-6E Serial 2 Network (S2NET) Module shall provide two EIA-485/ EIA-232 Asynchronous communications channels. The Model 2070-6E S2NET Module shall be a 2070 plug-in module with EIA-232 activity LEDs on the front edge. The Model 2070-6E S2NET Module shall communicate over standard IEEE 802.3 networks using both TCP (point-to-point) and UDP (point-to-multipoint) protocols.

10.7.2 Circuits

Two circuits, designated Circuits #1 and Circuits #2, shall be provided. Both circuits functions shall be identical, except for Circuit #1 which shall be routed to the terminal server and Circuit #2 shall route directly to the front panel's DB-9 connector. Each circuit shall provide full isolation from the Model 2070 Motherboard.

Line drivers/receivers shall be socket or surface mounted.

The Model 2070-6E S2NET Module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.7.3 Mechanical/Electrical Requirements

The Model 2070-6E S2NET Module shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-6E S2NET Module shall be provided with LED indicators for 10/100 and Half/Full Duplex Network Communications.

The User Serial port shall be a DB9 Female connector accessible from the front.

The Network port shall be a RJ45 modular jack connector accessible from the front. DIP switches shall be externally accessible.

The Model 2070-6E S2NET Module shall be powered direct from the 2070 Controller's edge connector.

10.7.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200 bps, 2400 bps, 9600 bps, 19.2 Kbps, 38.4 Kbps, 56 Kbps and 115.2 Kbps.

The Model 2070-6E S2NET Module Network Interface shall meet IEEE 802.3 and ANSI 8802-3 Standards and support 10/100 Mbps.

10.7.5 Echo Mode

The Model 2070-6E S2NET Module shall be provided with a switch allowing the user to switch module into Echo Mode. In Echo Mode communications from the external network shall be routed serially to the DB-9 on the front panel. An LED indicator shall be provided to indicate the Echo Mode communications.

10.7.6 Network Configuration

The Model 2070-6E S2NET Module shall support the following features:

Provide TCP and UDP over IP protocol communications.

Subnet masks for Class A, B, and C networks (see table below):

NETWORK CLASS	HOST BITS	Subnet Mask	Example IP Address
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100
C	8	255.255.255.0	192.168.0.100

Allow Manual or Automatic TCP/IP socket connections configuration.

Provide Telnet access for both configuration and communications.

Provide Dumb Terminal access using a User Serial port for configuring network parameters.

Provide the Ability to adjust packet size and packing algorithm.

The Model 2070-6E S2NET Module shall be provided with a Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and Serial Settings using a Web Browser.

10.7.7 Data Interfaces

Channel 1 and 2 Model 2070 Card Edge Connector
User Serial Port EIA-232 (DB9 Female)
Ethernet Data Port RJ45 EIA 568B Pin Out

10.7.8 LED Indicators

RTS Green or Red: DTE Request to Send
CTS Green or Red: Network Clear to Send
TXD Green or Red: DTE Transmit EIA-232 Data
RXD Green or Red: DTE Receive EIA-232 Data
DCD Green or Red: Network Data

10.7.9 Power Requirements

The power requirements of the Model 2070-6E S2NET Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in these specifications.

10.7.10 Environmental

The Model 2070-6E S2NET Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.7.11 Form Factor

See A10-7 for Details

CHAPTER 10-SECTION 8
MODEL 2070-9D DIAL-UP MODEM COMM MODULE

10.8.1 2070-9D Modem
The Model 2070-9D Modem shall consist of a Dial-Up Modem and shall be a Plug-in Card style version for the 2070 Controller.

10.8.2 Dial-Up Modem
The Dial-Up Modem shall consist of a 33.6Kbps dial-up modem meeting the V.34 AT Command set standard. The Modem shall contain two RJ-11 connectors, one designated as the Line and the second as Phone. An internal speaker shall be provided as an indicator for phone call progress. The speaker shall be controlled through AT standard commands. Front Panel LED indicators shall also be provided as shown in the A10-8 of these specifications.

10.8.2.1 Modem default configuration
The Modem shall contain the following default configurations:

ACTIVE PROFILE:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:138
S08:002	S48:007
S09:006	S95:000
S10:014	

STORED PROFILE 0:
B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0

S00:001	S12:050
S02:043	S18:000
S06:002	S36:007
S07:050	S40:104
S08:002	S41:195
S09:006	S46:138
S10:014	S95:000
S11:095	

Profile 0 should be configured as shown above and default as the active profile on wake up. Factory default shall wake up at 2400 Baud, Parity 8, N, 1 and no handshaking.

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Lock
2	"SMART Modem DB-9 Aux" Sel	DTE	DCE
3	RTS Overide	Normal	RTS High
4	"Modem /DB9 DTE Serial" Sel	Modem	DB9-DTE

All switches shall be OPEN position as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity.

10.8.2.2 Modulation

The Dial-Up Modem shall use Quadrature Amplitude Modulation and Operate within the following frequencies:

Data Carrier 1800 ± 0.5 Hz
Calling Tone 1300 ± 10 Hz
Answering Tone 2100 ± 15 Hz

The Modem shall have Receiver Frequency Tolerance of ± 14 Hz

10.8.2.3 Modem Standards

The Dial-Up Modem shall be ITU V.90, V.34 and Rockwell V.FC compatible. It shall meet the standards:

V.90, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, V.21, Bell 212, Bell 103, V.33, V.17, V.29, V.27 ter, and V.21 Channel 2.

10.8.2.4 Data Rates

The Dial-Up Modem shall support the following data rates:

33.6Kbps, 31.3Kbps, 28.8Kpbs, 26.4Kbps, 24.0Kbps, 21.6Kbps, 19.2Kbps, 16.8Kbps, 14.4Kbps, 12.0Kbps, 9.6Kpbs, 7.2Kpbs, 4.8Kpbs, 2.4Kpbs, 1.2Kpbs, and 300 baud.

The Modem shall automatically select the best operating speed as indicated in Section 10.6.2.1 of these specifications.

10.8.2.5 Error Correction & Data Compression

The Modem shall use V.42 LAPM, MNP2-4 and MNP 10 for error correction and V.42 Bis, MNP 5 for Data Compression.

10.8.2.6 Tx/Rx Power Level

The transmit level shall be fixed at -11± 2 dB and the receiver shall have a S/N Ratio of -26 dB with a Dynamic Range of 12 dBm to -42 dBm.

The Ring detect Sensitivity shall be 38 VRMS.

10.8.2.7 Line Interface

The Dial-Up Modem shall have a Ring Equivalent of 1 Bel and a terminating Impedance of 600 Ohms. It shall have return loss of better than 14 dB.

10.8.3 Circuit

The Model 2070-9D shall be provided with full isolation from the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-9D module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less.

10.8.4 Hot Swappable

The 2070-9 D Module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

10.8.5 Power Requirements

The power requirements of the Model 2070-9D Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in these specifications.

10.8.6 Environmental

The Model 2070-9D Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.8.7 Form Factor

See A10-8 for Details

CHAPTER 10-SECTION 9
MODEL 2070-7G UNIVERSAL TIME BASE MODULE

10.9.1 Model 2070-7G Universal Time Base Module

The Model 2070-7G Universal Time Base Module shall consist of a GPS receiver with antenna and a microprocessor-based circuit. It shall read raw GPS time data and accept user commands via Com 2 as defined elsewhere in these specifications. The Model 2070-7G Universal Time Base Module shall be a Plug-in Style Card version for the Model 2070 Controller. The Model 2070-7G shall be provided with two communications channels Com 1 and Com 2. Com 1 shall be used to establish serial communications between the Model 2070 Controller and a GPS receiver resident in the Model 2070-7G Universal Time Base Module. Com 2 shall be switch selectable between a Config Mode to the GPS receiver and a straight serial port for the Model 2070 Controller.

10.9.2 GPS Receiver/Antenna

The Model 2070-7G shall be provided with a Land-Based L1, C/A code GPS Receiver operating at a frequency of 1575.42MHz. The GPS Receiver shall contain a minimum of 16 Channels. The receiver shall have a tracking sensitivity level greater than -141dBm at the receiver input.

The Model 2070-7G shall be provided with an active permanently mount GPS Antenna. The Antenna mount shall consist of GPS roof-mount antenna with double threaded bolt, through hole, wing nut fastener, and locking nuts. The mounting shall consist of a Bulkhead mount with 0.8-inch threaded wing nut.

The Antenna System shall be comprised of an Antenna Element, Cable and Connector, and Low Noise Amplifier (LNA).

The Cable and Connector shall consist of a 2 Meter RG174/U Coaxial cable terminated at the non-antenna end with a BNC male/SMA female straight connector.

The Antenna Element shall use Right-Handed Circular Polarization (R.H.C.P) and shall have a minimum Gain of +5 dBi. The antenna shall have a VSWR of 1.5:1 max. and an output impedance of 50 Ohms.

The Low Noise Amplifier shall operate from a 3.3 to 5.5 V DC source and shall provide an Outer Band Attenuation of 20dB min. at Fo ± 50 MHz and a Gain of 31dB min.

The Overall Performance of the Antenna System including Antenna Element, LNA and Coax Cable shall be as follow:

Center Frequency: 1575	1575.42 MHz
Gain	26dB min.
Noise Figure	2.0 dB max.
Axial Ratio	3.0 dB max.
Bandwidth	2 MHz min.
VSWR	2.0:1 max.
Output Impedance	50 Ohms

10.9.3 Default Configurations

The Model 2070-7G Universal Time Base Module shall have the following default configuration parameters:

Baud Rate	1200 bps
Time Zone	8, Pacific Time Zone
New Line Character	ASCI Carriage Return, Except QC, which CR+LF
Hour Format	24 hour (Military Time)
Daylight Savings Time	Enabled
Begin DST Clock Correction	March, Second Sunday at 02:00AM
End DST Clock Correction	November, First Sunday at 2:00 AM

These parameters shall configurable using the Q & S Command Set as defined in Section 10.9.4 of these specifications.

10.9.4 Q & S Command Set

The "Q" Commands

"Q" commands shall be used to request information from the Model 2070-7G, such as global position, date and time. The Model 207-7G shall support the "Q" commands as listed in the following table.

Model 2070-7G "Q" COMMANDS

COMMAND	RETURNS	FORMAT	EXAMPLES
QA n1 n2 0 0	Status, DOY, time	13-byte Binary string	See detail comments below
QD	Date and Day of year	YY/MM/DD/day {newline}	02/02/05/036
QT	TIME	mHH:MM:SS:Thtd {newline}	A10:51:21:697 _17:45:05:489D
QC	Date, time status and day of week	YYMMDDHHmmSSThtLW {cr+lf}	020821231706945Y6
QD, QT, QL & QC	Message	ASCII string "NOT LOCKED ON"	NOT LOCKED ON
QM	Data stored in ROM	Bw:Dx:My:Ncr:Oz Baud: DST: 12/24: new line: Time Zone	B7:D0:M1:Ncr:O6 {newline}
QV	Firmware version	ASCII version number	v1.2

QI	Get Daylight saving time configuration	bMbsbhbmeMesehem{newline}	0302020011010200 {newline}
QL	Get Position (latitude and longitude)	DD.MM.SS.THTA ddd.mm.ss.thtO	38.53.23.123N 077.00.27.123W

"Q" Commands

QD When the "QD" command is received by the Model 2070-7G it shall respond with either the ASCII message "NOT LOCKED ON" or with the date in the format YY/MM/DD/day followed by the new line character. "doy" is the day of the year in a 3-digit format, January 1 being 001. If the Model 2070-7G has not yet found at least one satellite to ensure correct data, the response shall be "NOT LOCKED ON".

An example of a normal response from the Model 2070-7G to a "QD" command sent to it would be "02/02/05/036(new line character)". This sample data stream would represent February 5, 2002 and that date would be the 36th day of the year 2002.

Note: If the device is configured for a time zone other than the local time zone, the date and "doy" shown could differ from the local date, depending on the time of day.

QT When the "QT" command is received by the Model 2070-7G it shall respond with either the ASCII message "NOT LOCKED ON" or with the time of day in the format of an A or a P or an ASCII space (to signify A.M. or P.M. or 24 hour time format) immediately followed by "HH:MM:SS:Tht" and a "D", if Daylight Savings Time function is "Enabled" and ending with the new line character.

Two sample "QT" responses are:
"A10:51:21:697{NEW LINE}", which could be interpreted as 10:51 A.M. plus 21.697 seconds and not corrected for daylight savings time.
"_17:45:05:489D{new line}", which could be interpreted as 1745 plus 5.489 seconds (using the 24 hour format), with Daylight Savings Time Enabled. The "_" represents an ASCII "space" character and signifies that the output is in 24-hour format.

As with the "QD" command, if the Model 2070-7G is not receiving a valid signal from at least one satellite, the response to a "QT" command shall be the ASCII message "NOT LOCKED ON".

QC This command reply shall provide a combination of the information found in the "QT" and "QD" commands but in slightly different format and with some additional information.

As with the “QT”, “QL” and “QD” commands, the message “NOT LOCKED ON” shall be the reply if the Model 2070-7G does not have at least one satellite in view to determine the precise time and date.

A special synchronization character in the data stream (either Y or N) shall signify whether or not the date and time data are synchronized with UTC (Universal Coordinated Time).

In order for the Model 2070-7G to report fully synchronized data with the special character changed to “Y”, the unit must be tracking at least 4 satellites. If the synchronization character is “N” the time reported will be less precise but still within a few milliseconds of the UTC synchronized time. The “QC” command hour format is always 24 hour (military time) since there is no character in the data stream to indicate A.M. or P.M. An additional bit of information included in the “QC” data stream is a “day of the week” number. The number 0 (zero) indicates Sunday, 1 indicates Monday and so on through 6, which indicates Saturday. Unlike the “QT” and “QD” commands, the “new line” character shall not be changed. It shall always be ASCII “carriage return + line feed”. The format of the “QC” data stream shall be YYMMDDHHmmSSThtLW followed by an ASCII carriage return and line feed.

A sample “QC” data steam generated by the Model 2070-7G would be:

“02032123176945Y6{cr+lf}”. This data stream would be interpreted as March 21, 2002, the time, in 24 hour format, would be 2317 plus 6.945 seconds, the time is synchronized to UTC (Y) and the day of the week is Saturday (6). Note that the data stream does not indicate whether or not Daylight savings time is “Enabled or Disabled”.

QM The “QM” command shall reply with the parameters stored in non-volatile memory, which shall be the baud rate, daylight savings time enable-disable, time format, new line character and time zone. Parameters shall be separated by a colon and the data stream shall be terminated with the new line character. The data stream B7:DO:M1:Ncr:O6{newline} would represent a baud rate = 19200 bps, Daylight savings time = disabled, 12 hour time reporting format, new line character = carriage return and Time Zone = Central. This command shall be used to determine the current configuration.

QV When the “QV” command is received by the Model 2070-7G it shall reply with the firmware version number. The format for the firmware version shall be as VX.X where X.X shall digit from 0 to9. An example of a response to the QV command would be “V1.2” without the quotation marks. The “NOT LOCKED ON” message shall never reply to this query command.

QI The “QI” command shall replay the currently loaded Daylight-saving time parameters; these shall be stored in the non-volatile memory. A total of 8 parameters are shall be sent. The data stream is bMbsbhbmeMesehem{newline} and the parameters are as follow:

Begin Month (bM). The month when starts to observe the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
Begin Sunday (bs). The Sunday number of “begin month (bM)”. This value shall be a two digits number.

Begin Hour (bh) and Begin Minutes (bm). The time when starts to observe the DST. This time shall be expressed in a 24-hour format.
End Month (eM). The month when ends the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
End Sunday (es). The Sunday number of "end month (eM)". This value shall be a two digits number.
End Hour (eh) and End Minutes (em). The time when the DST observation ends. This time shall be expressed in a 24-hour format.

An example data stream 0302020011010200{newline} would represent DST clock adjust will begin at second Sunday of March at 02:00 AM and DST will end at first Sunday of November at 02:00 AM.

When the Model 2070-7G module detects any of both DST conditions, either Begin or End, it corrects the time by adding or subtracting one hour to local time. Once "begin DST" conditions met (Month, Sunday and time) it adds one hour to local time. When "end DST" conditions met (Month, Sunday and time) it subtracts one hour to local time.
The Model 2070-7G shall always respond to this command.

QL The "QL" command will replay the latitude and longitude of the current Global Position expressed in degrees, minutes, seconds and milliseconds, north (N) or south(S) for Latitude, east (E) or west (W) for longitude. The data stream shall be expressed as follows, DD.MM.SS.THTA_ddd.mm.ss.thtO{newline}.

DD = latitude degrees
MM = latitude minutes
SS = latitude seconds
THT = latitude milliseconds
A = latitude, North or South
ddd = longitude degrees
mm = longitude minutes
ss = longitude seconds
tht = longitude milliseconds
O = longitude, East or West

An example data stream 38.53.23.123N_077.00.27.123W{newline} would represent 38 degrees latitude north, with 53 minutes, 23 seconds and 123 milliseconds and 077 degrees longitude west with 00 minutes, 27 seconds and 123 milliseconds. As with the "QT", "QC" and "QD" commands, the message "NOT LOCKED ON" shall be the response if the Model 2070-7G does not have at least one satellite in view to determine the precise position.

Please note: the "_" represent an ASCII space.

QA The "QA" command differs from the other Q commands in that it must include two additional user selected variables n1 and n2, and two fixed variables n3 and n4, which are always zero. The output from the QA command depends on the variables sent with the command. It also differs

from the other Q commands in that the information returned is not ASCII but rater binary. A list of the user defined variables and the information returned follows.

User defined variables
n1– Time zone. The variable entered must be the sum of an ASCII 0 + (0 – 11) depending on the time zone desired. For example, ASCII 38 signifies time zone 8, Pacific.
n2 – Daylight savings time correction, 0 = disabled, 1 = enabled.

Possible replies from the Model 2070-7G to a QA command
Byte 0
Bits 1-3 are not used.
Bit 4 is 0 if valid time is not currently available and 1 if time is valid.
Bit 5 is 1 during the initialization phase only (before first lock on, i.e. LED changes to green for the first time. This bit changes to 0 at the first lock on and never changes even in subsequent amber conditions.
Bit 6 is 1 if GPS detects internal fault that could affect time reporting, otherwise is 0.
Bit 7 is normally 0 but if no satellite information is received for 24 hours, this bit will be 1.
Bit 8 is not used.

Byte 1
Bits 1-4 are not used, always zero.
Bits 5-6 are always 0 indicating that the time is in 24-hour format.
Bit 7, Daylight Savings Time indicator is 1 when DST is enabled, and the date is within the DST period. This bit is 0 if DST correction is disabled or the date is outside of the DST period.
Bit 8 is not used, always zero.

Bytes 2 and 3
Milliseconds portion of current time, the Hex equivalent of BCD.

Byte 4
Seconds portion of current time, the Hex equivalent of BCD.
Byte 5
Minutes portion of current time, the Hex equivalent of BCD.
Byte 6
Hours portion of current time, the Hex equivalent of BCD.
Bytes 7 and 8
Day of Year, the Hex equivalent of BCD.
Byte 9
Year (this byte is actually the offset from 1986) i.e. 18 = 2004, the Hex equivalent of BCD.
Bytes 10 and 11
Always zero.
Byte 12
Always a new line character (CR).

The “S” Commands

The Model 2070-7G shall accept instructions from the user in the form of “S” (Set) commands. The “S” commands, their variables, and their meanings that shall be supported shall consist of the following:

Model 2070-7G “S” COMMANDS

COMMAND	NAME OF COMMAND	"n" variable	SETTING (default)	(Notes)
SBn	SET BAUD RATE	0	Reserved	
		1	Reserved	
		2	Reserved	
		3	**(1200)**	
		4	2400	
		5	4800	
		6	9600	
		7	19200	
		8	38400	
SDn	SET DAYLIGHT SAVINGS TIME	0	Disabled	
		1	**(Enabled)**	
SMn	SET 12 OR 24 HOUR TIME FORMAT	**0**	**(24 Hour)**	
		1	12 Hour (AM/PM)	
SNn	SET NEW LINE CHARACTER	ASCII characters except colon and /	**(carriage return)**	
SOn	SET TIME ZONE	0	Time zone 0	UTC
		1	Time zone 1	
		2	Time zone 2	
		3	Time zone 3	
		4	Time zone 4	
		5	Time zone 5	Eastern
		6	Time zone 6	Central
		7	Time zone 7	Mountain
		8	**(Time zone 8)**	**Pacific**
		9	Time zone 9	Alaska
		: (colon)	Time zone 10	Hawaii
		; (semi-colon)	Time zone 11	

SI1bMbsbhbmeMeseh em	SET DAYLIGHT SAVING TIME CONFIGURATION	bM (Begin month)	03	
		bs (Begin Sunday)	02	
		bh (Begin hour)	02	
		bm (Begin minutes)	00	
		eM (End month)	11	
		es (end Sunday)	01	
		eh (end hour)	02	
		em (End minutes)	00	

"S" Commands

"S" Commands shall be sent to the Model 2070-7G without an "end of line" character.

The Model 2070-7G shall not send any acknowledgement when it receives an "S" command however the QM command can be used to confirm the change was made. All setting changes shall be stored in non-volatile memory and used in place of the factory default settings.

The following describes the "S" commands that shall be supported by Model 2070-7G:

SBn (Set Baud Rate). This command shall be used to change the Model 2070-7G's serial communication speed. The baud rate of the controller and the Model 2070-7G must be the same. When the unit is first powered up it shall be configured with the factory default baud rate of 1200.

When communications between the Model 2070-7G and the controller is established, the SB command can be used to change the baud rate to the preferred speed. The available baud rates are shown in "S" Commands table. Generally, the highest baud rate, that provides reliable communication, should be used. For example, to change the unit's default baud rate to 4800 baud, the proper "S" command to send would be "SB5" (without quotation marks). Any baud rate changes will go onto effect immediately.

SDn (Enable/Disable Daylight Savings Time). This command shall be used to enable or disable the device's one hour offset to accommodate Daylight Savings Time rules. If the unit is to be used to output local time in an area that observes Daylight Savings Time rules, the "SD1" command should be used. The factory default setting is "Enabled", which means the Model 2070-7G will

automatically adjust the local time output by one hour at the beginning and end of the Daylight Savings Time period. Users can change the configuration when these changes must occur with the SI1 command. If the unit will be used in areas that do not observe Daylight Savings Time, the appropriate "S" command to use would be "SD0".

SMn (Set time output format). This command shall be used to specify how the time of day data will be formatted. The factory default setting is the 24 hour, Military Time, format. If the user prefers to have the data output in a 12 hour format, (with A.M. or P.M. noted) the "SM1" (without the quotation marks) command must be sent once to change the format setting.

SNn (Set new line character). The Model 2070-7G's response to a valid "Q" command shall be a data stream that ends with a "new line" character. The default new line character is an ASCII carriage return. If the user prefers to have the data stream end in different ASCII character it can be changed using the "SN" command. Any ASCII character except the "/' (slash) and the ":" (colon) characters may be used as the variable. For example, to use "#" as the new line character the proper command to send would be "SN#" (without the quotation marks). Only one "new line character" is permitted.

SOn (Set time zone). This command allows the user to set the Model 2070-7G's output to reflect the local time. Each time zone is assigned a number or ASCII character that is used as the variable for the "SO" command. The Model 2070-7G firmware shall accommodate time zones 0 through 11. Time zone 0 shall be used to output UTC (Universal Coordinated Time) or GMT (Greenwich Mean Time) if the user prefers that reference instead of local time. The default factory value shall be 8, as listed under default configurations, which shall represent Pacific Standard Time in the United States.

SI1bMbsbhbmeMesehem (Set daylight saving time parameters). This command shall allow the user to set the Model 2070-7G's daylight saving time settings. The modification of these parameters will determine when DST begin & end:

Begin Month(bM). The month when starts to observe the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
Begin Sunday(bs). The Sunday number of "begin month (bM)". This value shall be a two digits number.
Begin Hour(bh) and Begin Minutes(bm). The time when starts to observe the DST. This time shall be expressed in a 24 hour format.
End Month(eM). The month when ends the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
End Sunday(es). The Sunday number of "end month(eM)". This value shall be a two digits number.
End Hour(eh) and End Minutes(em). The time when the DST observation ends. This time shall be expressed in a 24 hour format.

These parameters shall be set in the Non-Volatile memory.

10.9.5 Config Mode

The Model 2070-7G Module shall be provided with a switch allowing the user to switch Com 2 into Config Mode. In Config Mode, Com 2 loops back to the GPS Receiver and provides the user with a communications port to run Q and S Commands to configure the GPS receiver or query it for data. During Config Mode, the Config Mode LED indicator shall be turn ON to indicate configuration mode. When the Config Model is OFF, Com 2 shall consist of a serial port (serial pass through) to the Model 2070 Controller.

10.9.6 Connectors

The Model 2070-7G Universal Time Base Module shall contain the following connectors in the Faceplate:

Antenna	SMA Connector
Com 2 Port (C22S)	DB9 Female Connector

10.9.7 Data Output

When communicating to the GPS Receiver, the Date, Time, Day of Week, Signal Status, and Global Position shall be available. Data format shall be as defined in Section 10.9.4 of these specifications and the NMEA 0183 Standard. Serial Communications shall be software selectable at 1200, 2400, 4800, 9600, 19200 or 38400 bps.

10.9.8 Protocols

The Model 2070-7G shall support the NMEA 0183 Standard, Version 2.1 or later, as defined by the National Marine Electronics Association and the QC Command Set as defined in Section 10.9.4 of these specifications. A dipswitch marked "CMode" shall be provided which allows for the selection of one of three modes. The communication modes shall consist of a "NORM" (Normal Mode), "NB" (Normal Broadcast Mode) and GPS. When the CMode is in the "NORM" (Normal Mode) ON position, the Model 2070-7G shall respond to the QS command set as defined elsewhere in these specifications. When the dipswitch CMode is in the "NB", (Normal Broadcast Mode) ON Position, and the Model 2070-7G shall operate in a broadcast mode and shall not respond to the QS command set. When operating in the NB mode, the Model 2070-7G shall use the default settings as defined in section 10.9.2.

When the CMode is in the "GPS", (GPS pass through mode) ON position, the Model 2070-7G shall act like a standard NMEA 0183 compliant GPS receiver. As a minimum, when set on GPS mode, the Model 2070-7G shall support the following NMEA 2.0 Standard sentences: RMC, GGA, GSA, GSV, GLL and ZDA. The sentences shall be preceded by the standard generic Global Positioning System (GPS) talker ID "GP".

=== GLL - Geographic Position - Latitude/Longitude ===

	1	2	3	4	5	6	7	8
$--GLL	,llll.ll	,a	,yyyyy.yy	,a	,hhmmss.ss	,a	,m	,*hh

$--GLL,llll.ll,a,yyyyy.yy,a,hhmmss.ss,a,m,*hh<CR><LF>

Field Number:

1. Latitude
2. N or S (North or South)
3. Longitude
4. E or W (East or West)
5. Universal Time Coordinated (UTC)
6. Status A - Data Valid, V - Data Invalid
7. FAA mode indicator (NMEA 2.3 and later)
8. Checksum

3. N or S (North or South)
4. Longitude=== GGA - Global Positioning System Fix Data ===

Time, Position and fix related data for a GPS receiver.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$--GGA	,hhmmss.ss	,llll.ll	,a	,yyyyy.yy	,a	,x	,xx	,x.x	,x.x	,M	,x.x	,M	,x.x	,xxxx	*hh

$--GGA,hhmmss.ss,llll.ll,a,yyyyy.yy,a,x,xx,x.x,x.x,M,x.x,M,x.x,xxxx*hh<CR><LF>

Field Number:

1. Universal Time Coordinated (UTC)
2. Latitude

5. E or W (East or West)
6. GPS Quality Indicator,
   - 0 - fix not available,
   - 1 - GPS fix,
   - 2 - Differential GPS fix
     (values above 2 are 2.3 features)
   - 3 = PPS fix
   - 4 = Real Time Kinematic
   - 5 = Float RTK
   - 6 = estimated (dead reckoning)
   - 7 = Manual input mode
   - 8 = Simulation mode
7. Number of satellites in view, 00 - 12
8. Horizontal Dilution of precision (meters)
9. Antenna Altitude above/below mean-sea-level (geoid) (in meters)

10. Units of antenna altitude, meters
11. Geoidal separation, the difference between the WGS-84 earth ellipsoid and mean-sea-level (geoid), "-" means mean-sea-level below ellipsoid
12. Units of geoidal separation, meters
13. Age of differential GPS data, time in seconds since last SC104 type 1 or 9 update, null field when DGPS is not used
14. Differential reference station ID, 0000-1023
15. Checksum

Example:
$GPGGA,180844.000,3211.10532,N,11055.20380,W,0,00,99.0,779.59,M,-27.7,M, ,*69

=== RMC - Recommended Minimum Navigation Information ===

	1	2	3	4	5	6	7	8	9	10	11	12	13
$--RMC	,hhmmss.ss	,A	,llll.ll	,a	,yyyyy.yy	,a	,x.x	,x.x	,xxxx	,x.x	,a	,m	*hh

$--RMC,hhmmss.ss,A,llll.ll,a,yyyyy.yy,a,x.x,x.x,xxxx,x.x,a,m*hh<CR><LF>

Field Number:

1. UTC Time
2. Status, V=Navigation receiver warning A=Valid
3. Latitude
4. N or S
5. Longitude
6. E or W
7. Speed over ground, knots
8. Track made good, degrees true
9. Date, ddmmyy
10. Magnetic Variation, degrees
11. E or W
12. FAA mode indicator (NMEA 2.3 and later)
13. Checksum

A status of V means the GPS has a valid fix that is below an internal quality threshold, e.g. because the dilution of precision is too high or an elevation mask test failed.

Example:
$GPRMC,180845.000,V,3211.105,N,11055.204,W,0.0,0.0,271009,9.4,E*6E

=== ZDA - Time & Date - UTC, day, month, year and local time zone ===

	1	2	3	4	5	6	7

$--ZDA	,hhmmss.ss	,xx	,xx	,xxxx	,xx	,xx	*hh

$--ZDA,hhmmss.ss,xx,xx,xxxx,xx,xx*hh<CR><LF>

Field Number:

1. UTC time (hours, minutes, seconds, may have fractional subsecond)
2. Day, 01 to 31
3. Month, 01 to 12
4. Year (4 digits)
5. Local zone description, 00 to +- 13 hours
6. Local zone minutes description, apply same sign as local hours
7. Checksum

Example: $GPZDA,160012.71,11,03,2004,-1,00*7D

10.9.9 LED Indicators

Function		LEDs
Com 1	TxD	Green or Red
	RxD	Green or Red
Com 2	TxD	Green or Red
	RxD	Green or Red
Config Mode		Green or Red
Tracking		Tri-Color

10.9.10 Model 2070-7G Tracking

The Model 2070-7G Universal Time Base Module shall be provided with the following tracking functionality:

The Model 2070-7G shall be equipped with a tri-color LED (Light Emitting Diode) to indicate the unit's status during operation; the LED shall be located at the faceplate and labeled as TRACKING as shown in detail A10-9.

The various states of the TRACKING LED indicator and their meanings shall be as described in the section below.

Power up phase: At power up, the 2070-7G's microprocessor shall read the five parameters stored in the unit's non-volatile memory. These parameters are Baud Rate, Daylight Savings Time mode and configuration, Time Zone, Military Time format and new line character. The default values shall be read from memory if they have not been modified. Next, the communications port shall be initialized and the speed set to the stored baud rate parameter. The remaining three communications parameters shall be fixed at 8 data bits, no parity and 1 stop bit.
The power up process shall take no more than 200 milliseconds. During this period the unit may not respond to any "S" or "Q" commands and the LED shall be amber for less than one second.

GPS initialization phase: After the power, up phase is complete the unit will query the GPS receiver to see if it is already initialized. This is usually the case when the unit is powered up. If there is no data output, the GPS receiver will be initialized by the firmware program, using initialization commands and known variables.

This process shall not take longer than take 6 seconds. During this period, the Model 2070-7G reply to the commands "QA", "QD", "QT", and "QC" shall be the message "NOT LOCKED ON" and the LED shall flash red, once per second.

Signal acquisition phase: Once the GPS initialization phase is complete, it shall take from 3 to 180 seconds for the unit to acquire and process the first satellite's signal.

When the Model 2070-7G has received and processed the first satellite's information, unsynchronized time/date information shall be available using the "QC" data stream and the synchronization character shall be "N". When the synchronization character is "N", the "QC", and "QT" and "QD" replies will be complete, but time is not fully synchronized to UTC. When unsynchronized data is available, the LED shall flash amber, once per second.

Fully synchronized phase: When the 2070-7G has acquired information from 4 satellites its output will be synchronized to UTC (Universal Coordinated Time. When the unit is synchronized to UTC it is said to be "LOCKED ON". At this point the "QT", "QD", "QL" and "QC" replies will contain the most accurate information (time and location) possible. When the unit is fully synchronized (LOCKED ON); the synchronization character shall the letter "Y" in the "QC" data stream and the LED indicator shall flash green, once per second.

10.9.11 Power Requirements

The power requirements of the Model 2070-7G Universal Time Base Module shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in these specifications.

10.9.12 Environmental

The Model 2070-7G Universal Time Base Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.9.13 Form Factor

See A10-9 for details

CHAPTER 10-SECTION 10
MODEL 2070-EX NETWORK SWITCH MODULE

10.10.1 Model 2070-Ex Network Switch Module

The Model 2070-Ex Module shall provide 4 ports for Network Communications to and from the Model 2070 Controller.

An integrated Store-and-Forward Network Switch shall be used as the core for the Model 2070-Ex Module. A network port shall be used to route Ethernet Traffic across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively. Three network ports shall be brought to RJ-45 Connectors on the Front Panel.

The Model 2070-Ex Module shall be a Plug-in Card style version for the 2070 Controller.

10.10.2 Mechanical/Electrical Requirements.

The Model 2070-Ex Modules card edge connector shall be fully compatible with the 2070 Controller's Motherboard Ax Card Slots.

The Model 2070-Ex Module shall be powered direct from the 2070 Controller's edge connector.

10.10.3 Model 2070-Ex Module Requirements

The Model 2070-Ex shall be provided with Network Magnetics for each port including the network port routed to the Controller's Motherboard.

10.10.4 Network Standards

The Model 2070-Ex Module shall meet the IEEE802.3 10Base-T, IEEE 802.3u, and IEEE 802.3x.

10.10.5 Modes of Operation

The Model 2070-Ex Module shall have auto-negotiation for 10/100 Mbps Connection speed and Half/Full-Duplex modes on all RJ-45 ports.

The Model 2070-Ex Module shall be provided with Auto-MDIX for all RJ-45 ports.

The network port routed to the Controller's Motherboard shall have Auto-negotiation for 10/100Mbps connection speed and the Half/Full-Duplex communications mode shall be manually settable.

10.10.6 Network Media Support

The Model 2070-Ex Module shall be configured as a Multiple Channel Media Converter to route network traffic between the Model 2070 CPU, Three RJ-45 Front Panel Connectors.

The Model 2070-Ex Module shall support the following Media:

100Baset-TX: Cat. 5, EIA/TIA-568B, 100-Ohm UTP cables.

10.10.7 LED Indicators

The Model 2070-Ex Module shall be provided with RJ-45 Connectors containing Link/Activity and 10/100 Speed LED indicators. Network Link/Activity and 10/100 Speed indicators for the port routed to the Controller's Motherboard shall be provided on the Front Plate of the Model 2070-Ex Module.

10.10.8 Form Factor

See A10-10 for Details

10.10.9 Power Requirements

The power requirements of the 2070-Ex Module be within the power limitations of the Model 2070 Unit as describe in Section 9.2.5 of these specifications.

Models	**5 VDC**	**+12 VDC iso**	**+12 VDC ser**	**-12 VDC ser**
2070-6A & Others	900mA		300 mA	300 mA

10.10.10 Environmental

The 2070-Ex Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 11
MODEL 2070-WE WIRELESS ETHERNET COMM MODULE

10.11.1 Model 2070-WE Wireless Ethernet Communications Module

The Model 2070-WE Wireless Ethernet Communications Module shall provide a channel for Ethernet communications over wireless between the Model 2070 controller and other remote controllers/network devices. A second channel shall be provided for serial communications from and to the Model 2070 controller. The Model 2070-WE Wireless Ethernet Communications Module shall be a 2070 plug-in module. The Model 2070-WE Wireless Ethernet Communications Module shall convert Ethernet data to frequency hopping spread spectrum data.

10.11.2 Channels

The two Channels shall be designated as Comm 1 and Comm 2. Comm 1 shall be routed, via magnetic, to the integrated switch in the Model 2070 controller. Comm 1 shall be used for Ethernet communications over Spread Spectrum Radio.

Comm 1 port shall be used to route Ethernet Traffic across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively.

Comm 2 shall route directly to the front panel's DB-9 connector. Comm 2 circuit shall provide full isolation from the Model 2070 Motherboard.

Line drivers/receivers shall be socket or surface mounted.

The Model 2070-WE Wireless Ethernet Communications Module's Comm 2 isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

The channel shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.11.3 Mechanical/Electrical Requirements

The Model 2070-WE Wireless Ethernet Communications Module shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-WE Wireless Ethernet Communications Module shall be provided with LED indicators for as shown in detail A10-11 of these specifications.

The Comm 2 port shall be a DB9 Female connector accessible from the front and maybe be used to configure the Spread Spectrum Radio.

The Model 2070-WE Wireless Ethernet Communications Module shall be powered direct from the 2070 Controller's edge connector.

The Model 2070-WE Wireless Ethernet Communications Module shall have a MTBF of over 60,000 hours.

10.11.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200 bps, 2400 bps, 9600 bps, 19.2 Kbps, 38.4 Kbps, 56 Kbps and 115.2 Kbps.

10.11.5 Local Mode

The Model 2070-WE Wireless Ethernet Communications Module shall be provided with a switch allowing the user to switch Comm 2 into local mode. Local mode shall allow the user to perform Ethernet configurations on the Spread Spectrum Radio. On non-local mode, Comm 2 shall meet the requirements as specified for the Model 2070-7A Module as specified elsewhere in these specifications.

10.11.6 Spread Spectrum Radio

The Model 2070-WE Wireless Ethernet Communications Module shall meet the following Spread Spectrum Radio requirements:

Frequency Range	902-928 MHz
Output Power	100mW to 1000mW
Software Programmable	Yes
Min Hop Patterns	Based on Network Address (> 4 Million)
Number of RF Channels	90
RF Channel Spacing	280KHs
Error Checking	32Bit-CRC
Encryption	128 Bit, AES Encryption
Receiver Sensitivity/BER	-108 dBm/BER=10-6
System Gain	36 dBm
Antenna Port	RP TNC-F
Certification	FCC Approved
Operation Mode	Transceiver
Error Correction	Forward Error Correction
System Configuration	Point-to-Point, Point-to-Multipoint

10.11.7 Ethernet Communications Module Configuration

The Model 2070-WE shall be configurable as a master, repeater or slave using the Ethernet Web Interface.

10.11.8 Ethernet Web Interface

The Model 2070-WE shall support the following features:

Provide TCP and UDP over IP protocol communications.

Subnet masks for Class A, B, and C networks (See Table Below):

Network	Host BITS	Subnet Mask	Example IP Address
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100
C	8	255.255.255.0	192.168.0.100

The Model 2070-WE shall be provided with Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and all system configurations using a Web Browser.

As a minimum a user shall be able to do the following via the Web Browser:

1 System Configuration
2 Network Configuratiton
3 Radio Configuration
4 Security Configuration
5 Comm Port Configuration
6 Network Status

The Model 2070-WE shall have a default IP Address of 192.168.11.51, Subnet Mask as 255.255.255.0.

10.11.9 Data Interfaces

Channel 1 and 2 Model 2070 Card Edge Connector

User Serial Port EIA-232 (DB9 Female)

10.11.10 LED Indicators

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

Multiple Mini-LEDs indicating Field Strength.

10.11.11 Power Requirements

The power requirements of the Model 2070-WE Wireless Ethernet Communications Module shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specification.

10.11.12 Environmental

The Model 2070-WE Wireless Ethernet Communications Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.11.13 Form Factor
See A10-11 Details

CHAPTER 10-SECTION 12
MODEL 2070-J ETHERNET JACK MODULE

10.12.1 Model 2070-J Ethernet Jack Module
The Model 2070-J Ethernet Jack Module shall provide an interface for Ethernet communications to the Model 2070 controller via the Motherboard. The Model 2070-J Module shall function as an extended third Ethernet port for the Model 2070-1E/IC CPU.

10.12.2 Channels
The Model 2070-J's RJ-45 Jack and Network Magnetics shall interface with the Network Lines, NetP5 TX+, TX-, RX+ and RX- respectively of the Model 2070 controller.

10.12.3 Mechanical/Electrical Requirements
The Model 2070-J Module shall be designed to fit in a single slot of a Model 2070 Controller.

10.12.4 Power Requirements
The power requirements of the Model 2070-j Module shall be within the power limitations of the Model 2070 Unit as describe elsewhere in this specification.

10.12.5 Environmental
The Model 2070-J Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.12.6 Form Factor
See A10-12 Details

CHAPTER 10-SECTION 13
MODEL 2070-LAN MODULE

10.13.1 Model 2070-LAN Local Area Network Module

The Model 2070-LAN Module shall provide 8 ports for Network Communications to and from network modules in the Model 2070 Controller Ax Slots and the front panel.

An integrated Store-and-Forward 8 port Network Switch shall be used as the core for the Model 2070-LAN Module. Network ports from the switch residing in the Model 2070-LAN Module shall be used to route Ethernet Traffic across the Motherboard to the "Ax" Connector's Network Lines. The Motherboard shall be designed to maintain 100 ohms impedance on all differential Ethernet lines. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively. One network port shall be brought to a RJ-45 Connector on the Faceplate.

The Model 2070-LAN Module shall be a Plug-in Card style version for the 2070 Controller.

A microcontroller shall be provided to allow for switch configurations including setting up VLANS and rate limiting on ports.

10.13.2 Mechanical/Electrical Requirements.

The Model 2070-LAN Modules card edge connector shall be fully compatible with the 2070 Controller's Motherboard Ax Card Slots.

The Model 2070-LAN Module shall be powered direct from the 2070 Controller's edge connector.

10.13.3 Model 2070-LAN Module Requirements

The Model 2070-LAN shall be provided with Network Magnetics for each port.

10.13.4 Network Standards

The Model 2070-LAN Module shall meet the IEEE802.3 10Base-T, IEEE 802.3u, and IEEE 802.3x.

10.13.5 Modes of Operation

The Model 2070-LAN Module shall have auto-negotiation for 10/100 Mbps connection speed and Half/Full-Duplex modes on the RJ-45 port.

The Model 2070-LAN Module shall be provided with Auto-MDIX for the RJ-45 port.

The network ports routed to the Controller's Motherboard shall have Auto-negotiation for 10/100Mbps connection speed.

10.13.6 Network Media Support

The Model 2070-LAN Module shall be configured as a Multiple Channel Media Converter to route network traffic between network modules in the Ax Slots and the RJ-45 Faceplate Connector.

The Model 2070-LAN Module shall support the following Media:

100Baset-TX: Cat. 5, EIA/TIA-568B, 100-Ohm UTP cables.

10.13.7 LED Indicators

The Model 2070-LAN Module shall be provided with an RJ-45 Connector containing Link/Activity and 10/100 Speed LED indicators. Network Link/Activity and 10/100 Speed indicators for the port routed to the Controller's Motherboard shall be provided on the Face Plate of the Model 2070-LAN Module as shown in A9-18

10.13.8 Form Factor

See A10-13 for Details

10.13.9 Power Requirements

The power requirements of the 2070-LAN Module be within the power limitations of the Model 2070 Unit as describe in Section 9.2.5 of these specifications.

Models	**5 VDC**	**+12 VDC iso**	**+12 VDC ser**	**-12 VDC ser**
2070-LAN	1 A			

10.13.10 Environmental

The 2070-LAN Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 14
MODEL 2070-CELL CELLULAR COMM MODULE

10.14.1 Model 2070-CELL Cellular Communications Module

The Model 2070-CELL Cellular Communications Module shall consist of Cellular System Module combined with Network switch allowing functionality of multiple network channels. The Model 2070-CELL shall provide a channel for Cellular communications over Cellular between the Model 2070 controller and remote controllers/network devices. It should also provide two additional channels for direct communications via cellular from devices connected to the faceplate network ports.

The Model 2070-CELL Cellular Communications Module shall be a 2070 plug-in module.

10.14.2 Integrated Network Switch

The Model 2070-CELL shall include a 5-port integrated Store-and-Forward Network Switch shall. A network port shall be interfaced to the Cellular System Module. A second network port shall be used to route Ethernet Traffic via magnetics across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively. Two network ports shall be brought via magnetics to RJ-45 Connectors on the Model 2070-CELL's faceplate.

These two ethernet ports shall be labeled as Eth1 and Eth2 as listed in A10-14. Each Ethernet shall be capable of reliably passing a minimum of 100 Mbps.

10.14.3 Mechanical/Electrical Requirements

The Model 2070-CELL Cellular Communications Module shall be designed to fit in a single slot of a Model 2070 Controller and placed into a 2070-6A & Others slot.

The Model 2070-CELL Cellular Communications Module shall be provided with LED indicators for as shown in detail A10-14 of these specifications.

The Eth1 and Eth2 ports shall be standard Ethernet ports supporting 10/100 MB speeds. These two ports may be used to verify cellular network connectivity and to connect to network devices in the cabinet.

The Model 2070-CELL Cellular Communications Module shall be powered direct from the 2070 Controller's edge connector. The Model 2070-CELL Module shall be connected to power pins 28A (+12 VDC Ser) and 27A (ground) of the 2070-Motherboard.

The Model 2070-CELL Cellular Communications Module shall have a MTBF of over 60,000 hours.

Connections:
Cellular Antenna: Female SMA
Cellular Antenna Aux/Diversity: Female SMA
GPS Antenna: Female SMA

SIM: Standard 1.8/3V SIM receptacle (G2 & H4 models), Micro-Std.

10.14.4 GPS Support

The Model 2070-CELL Cellular Communications Module shall have the capabilities to provide GPS support over ethernet to the Model 2070-1X CPU. The Model 2070-CELL shall be provided with a Land-Based L1, C/A code GPS Receiver operating at a frequency of 1575.42MHz. The GPS Receiver shall contain a minimum of 12 Channels. The receiver shall have a tracking sensitivity level greater than -161dBm at the receiver input.

10.14.5 GPS Protocol

The Model 2070-CELL shall support the NMEA 0183 Standard, Version 2.01 or later, as defined by the National Marine Electronics Association.

Model 2070-CELL shall act like a standard NMEA 0183 compliant GPS receiver. As a minimum, the Model 2070-CELL shall support the following NMEA 2.0 Standard sentences: RMC, GGA, GSA, GSV, GLL and ZDA. The sentences shall be preceded by the standard generic Global Positioning System (GPS) talker ID "GP".

=== GLL - Geographic Position - Latitude/Longitude ===

	1	2	3	4	5	6	7	8
$--GLL	,llll.ll	,a	,yyyyy.yy	,a	,hhmmss.ss	,a	,m	,*hh

$--GLL,llll.ll,a,yyyyy.yy,a,hhmmss.ss,a,m,*hh<CR><LF>

Field Number:

1. Latitude
2. N or S (North or South)
3. Longitude
4. E or W (East or West)
5. Universal Time Coordinated (UTC)
6. Status A - Data Valid, V - Data Invalid
7. FAA mode indicator (NMEA 2.3 and later)
8. Checksum

3. N or S (North or South)
4. Longitude=== GGA - Global Positioning System Fix Data ===

Time, Position and fix related data for a GPS receiver.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$--GGA	,hhmmss.ss	,llll.ll	,a	,yyyyy.yy	,a	,x	,xx	,x.x	,x.x	,M	,x.x	,M	,x.x	,xxxx	*hh

$--GGA,hhmmss.ss,llll.ll,a,yyyyy.yy,a,x,xx,x.x,x.x,M,x.x,M,x.x,xxxx*hh<CR><LF>

Field Number:

1. Universal Time Coordinated (UTC)
2. Latitude

5. E or W (East or West)
6. GPS Quality Indicator,
   - 0 - fix not available,
   - 1 - GPS fix,
   - 2 - Differential GPS fix
     (values above 2 are 2.3 features)
   - 3 = PPS fix
   - 4 = Real Time Kinematic
   - 5 = Float RTK
   - 6 = estimated (dead reckoning)
   - 7 = Manual input mode
   - 8 = Simulation mode
7. Number of satellites in view, 00 - 12
8. Horizontal Dilution of precision (meters)
9. Antenna Altitude above/below mean-sea-level (geoid) (in meters)
10. Units of antenna altitude, meters
11. Geoidal separation, the difference between the WGS-84 earth ellipsoid and mean-sea-level (geoid), "-" means mean-sea-level below ellipsoid
12. Units of geoidal separation, meters
13. Age of differential GPS data, time in seconds since last SC104 type 1 or 9 update, null field when DGPS is not used
14. Differential reference station ID, 0000-1023
15. Checksum

Example:
$GPGGA,180844.000,3211.10532,N,11055.20380,W,0,00,99.0,779.59,M,-27.7,M, ,*69

=== RMC - Recommended Minimum Navigation Information ===

	1	2	3	4	5	6	7	8	9	10	11	12	13
$--RMC	,hhmmss.ss	,A	,llll.ll	,a	,yyyyy.yy	,a	,x.x	,x.x	,xxxx	,x.x	,a	,m	*hh

$--RMC,hhmmss.ss,A,llll.ll,a,yyyyy.yy,a,x.x,x.x,xxxx,x.x,a,m*hh<CR><LF>

Field Number:

1. UTC Time
2. Status, V=Navigation receiver warning A=Valid
3. Latitude
4. N or S
5. Longitude
6. E or W
7. Speed over ground, knots
8. Track made good, degrees true
9. Date, ddmmyy
10. Magnetic Variation, degrees
11. E or W
12. FAA mode indicator (NMEA 2.3 and later)
13. Checksum

A status of V means the GPS has a valid fix that is below an internal quality threshold, e.g. because the dilution of precision is too high or an elevation mask test failed.

Example:
$GPRMC,180845.000,V,3211.105,N,11055.204,W,0.0,0.0,271009,9.4,E*6E

=== ZDA - Time & Date - UTC, day, month, year and local time zone ===

	1	2	3	4	5	6	7
$--ZDA	,hhmmss.ss	,xx	,xx	,xxxx	,xx	,xx	*hh

$--ZDA,hhmmss.ss,xx,xx,xxxx,xx,xx*hh<CR><LF>

Field Number:

1. UTC time (hours, minutes, seconds, may have fractional subsecond)
2. Day, 01 to 31
3. Month, 01 to 12
4. Year (4 digits)
5. Local zone description, 00 to +- 13 hours
6. Local zone minutes description, apply same sign as local hours

7. Checksum

Example: $GPZDA,160012.71,11,03,2004,-1,00*7D

10.14.6 Cellular Carrier Support

The Model 2070-CELL Cellular Communications Module shall support major cellular carriers. It shall support 5G or 4G LTE (Cat3 or Cat4) with features to fall back earlier cellular technologies.

The model 2070-CELL shall have two antenna connectors on the faceplate to allow the reception of 4G LTE signal (MIMO).

10.14.7 Ethernet Communications Configuration

The Model 2070-CELL shall be configurable for its Ethernet communication module. The Model 2070-CELL shall have a default IP Address of 192.168.222.100 Subnet Mask as 255.255.255.0.

The Model 2070-CELL shall have a DHCP server to automatically assign an IP address to each client device within the range of 192.168.222.101 and 192.168.222.254.

10.14.8 System Configuration

The Model 2070-CELL shall support the following features:

- Linux operation system
- Provide TCP and UDP over IP protocol communications.
- Firmware upgrade and system debug via the USB host port on the faceplate.
- Basic firewall, including port forwarding, allowed inbound and outbound IP addresses. Allow access to the modem through SSH using port 2658.
- System health monitoring and remote management
- Hardware watchdog

10.14.9 Web Interface

The Model 2070-CELL shall be provided with Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and all system configurations using a Web Browser.

As a minimum a user shall be able to do the following via the Web Browser:

- System and Network Status
- WAN Configuration
- LAN Configuration
- Firewall / Security
- System Configuration / Administration

10.14.10 Data Interfaces

The Model 2070-CELL has the following data interfaces:

- USB 2.0
- Two RJ-45 Network Ports

10.14.11 LED Indicators

As shown in A10-14, the Model 2070-CELL has the following LED lights on the faceplate:

PWR	Red light on indicating power is on.
Net	A light indicating the connection state with the Model 2070 Controller
Act	A light indicating the connection state with the Model 2070 Controller
Signal Strength	Multiple Mini-LEDs indicating Cellular Signal Strength.
10/100	A light indicating the connection state with a connected Ethernet device
LNK/ACT	A flashing green light indicates the activity with a connected Ethernet device

10.14.12 Power Requirements

The power requirements of the Model 2070-CELL Cellular Communications Module shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specification. The Model 2070-CELL UNIT shall draw power from the 5 VDC.

10.14.13 Environmental
The Model 2070-CELL Cellular Communications Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.14.14 Form Factor
See A10-14 Details

CHAPTER 10-SECTION 15
2070 COMM MODULE DETAILS

CHAPTER 11
2070 / NEMA STANDARD
CONTROLLER UNITS

CHAPTER 11-SECTION 1
NEMA 2070

11.1.1 2070 / NEMA Standard Controller Units

This specification covers two versions of 2070 / NEMA Standard Controller Units. The versions associate with NEMA TS1/TS2 Type 2 and NEMA TS2 Type 1 Standards. They are as follows:

Model 2070 (E, M, LX or LX+) N1 Controller Unit (TS1/TS2 Type 2)
Model 2070 (E, M, LX or LX+) N2 Controller Unit (TS2 Type-1)

11.1.2 N1 Unit Consisting

The Model 2070 (E, M, LX or LX+) N1 Controller Unit consists of:

Unit Chassis
2070- 1E, 1M or 1C CPU Module
2070-2C Field I/O Module
2070-3B or 3B+ Front Panel Module
2070-4NA Power Supply Module
2070-5 VME Cage Assembly, if required)
2070-8 Field I/O Module

11.1.3 N2 Unit Consisting

The MODEL 2070 (E, M, LX or LX+) N2 CONTROLLER UNIT consists of:

Unit Chassis
2070-1E, 1M or 1C CPU Module
2070-2N Field I/O Module
2070-3B or 3B+ Front Panel Module
2070-4N (A) Power Supply Module
2070-5 VME Cage Assembly, if required)

11.1.4 Address

The Serial Port 5 Frame Address for 2070-2N and 2070-8 shall be “20”

CHAPTER 11-SECTION 2
2N FIELD IO MODULE

11.2.1 2070-2N Field I/O Module

The 2070-2N Field I/O Module provides a TS2 Type 1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor LOGIC Output via SP5 on output O78 (similar to the 2070-8) to the NEMA TS2 Malfunction Management Unit (MMU). The communications timeout operation shall function in a manner similar to the 2070-8 (see sections 11.4.11.6 and 11.4.11.7 for details)

11.2.2 Requirements Exceptions

The Module shall meet the 2070–2E+ Module Requirements with the following exceptions:

No C1, C11 and C12 Connectors on the front panel of the module
No 64 inputs / 64 outputs requirements
Serial Port 5 routed to the FCU MPU Device only
Serial Port 3 shall not have a disabling switch
No Watchdog output
No Muzzle Shunt

11.2.3 Types

The module shall be a 4X type board/front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a Port 1 DA-15S connector labeled as either "C15S" or "Port 1". The Port 1 (C15S) connector shall be a 15 pin metal shell DA-15 connector with female contacts. The connector shall be equipped with latching blocks and shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1, or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent.

11.2.4 Power

Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle with equipment ground also connected to the face plate. Connector A shall intermate with a NEMA TS2 Type 1 (MS3106( )-18-1S) cable.

11.2.5 Isolation

The module shall isolate 2070 Serial Port 3 from the A3 Connector and reconvert the lines to external EIA 485 drivers/receivers which shall be terminated at C15S Connector. The Port shall be clocked at 153.6 Kbps.

11.2.6 FCU Output

An FCU output shall drive an open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 mA at 30 VDC.

11.2.7 Connectors A, C15S pin out and functions

Connector A and C15S pin_out and functions are as follows:

CONNECTOR A

Pin	Function	Pin	Function	Pin	Function
A.	AC Neutral	E.	NA	I.	NA
B.	NA	F.	Fault Monitor	J.	NA
C.	AC Line	G.	DCG #2		
D.	NA	H.	EG (Equip Ground)		

CONNECTOR C15S

Pin	Function	Pin	Function	Pin	Function
1	SP3TXD+	6	DCG #2	11	SP3TXC-
2	DCG #2	7	SP3RXC+	12	EG (Equip Ground)
3	SP3TXC+	8	DCG #2	13	SP3RXD-
4	DCG #2	9	SP3TXD-	14	NA
5	SP3RXD+	10	Port 1 Disable	15	SP3RXC-

11.2.8 Serial Port 3

Serial Port 3 shall control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards. SP3DCD shall be allocated to Port 1 Disable where 0 VDC input on C15S pin 10 equals DCD inactive (False). SP3DCD shall be opto-isolated from Port 1 Disable.

CHAPTER 11-SECTION 3
4N (A) POWER SUPPLY MODULE

11.3.1 2070-4N Power Supply Module

The 2070-4N Power Supply Module supports the NEMA TS 1 and TS2 Standards. The module is identical to the 2070-4A Power Supply Requirements except for the following:

The power cord shall have a 15 inch ± 1-inch length as measured from the panel to the plug tips.

The AC Power Fail voltage shall be 85VAC ±2VAC.

The AC Power Restore voltage shall be 90VAC ±2VAC.

The 2070-4N (A) power supply shall have proper marking Example “2070 4N (A)”. A permanent sticker shall be an acceptable marking method.

CHAPTER 11-SECTION 4
MODEL 2070- 8 FIELD I/O MODULE

11.4.1 Module Consisting

The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS shall be made of 0.06 in. minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

11.4.2 Module Front Panel

The Module Front Panel shall be furnished with the following:

1. ON/OFF POWER Switch mounted vertically with ON in the UP position.
2. LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 3% and the +24 VDC is within 8%.
3. Incoming VAC fuse protection.
4. Two DB-25S COMM connectors labeled "EX1" & "EX2."
5. Four NEMA Connectors A, B, C, & D.

11.4.3 Label

A permanent Label shall be affixed to the Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

11.4.4 Module Power Supply

A Module Power Supply shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control.

The supply shall meet the following requirements.

Input Protection: Specification 9.5.3 Input Protection

Power Supply Requirements: the power supply shall meet the specification as listed in Section 9.5.6 Power Supply.

Tolerances: DC Voltage tolerances shall be ±3% for 5 VDC and ±8% for 24 VDC.

11.4.5 Incoming AC Power

The supplied Incoming AC Power shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

11.4.6 Module PC Boards

All Module PC Boards shall be mounted vertically.

11.4.7 POWERDOWN, NRESET, and LINESYNC

POWERDOWN, NRESET, and LINESYNC are incoming EIA-485 differential signals and shall be routed to the module via C12S Connector. The state of the module output ports at the time of POWERDOWN transition to LOW State and until NRESET goes HIGH shall be an open circuit.

11.4.8 Requirements

The Module shall meet all requirements under CHAPTER 9 SECTION 3 with the following exceptions:

11.4.8.1 Parallel Ports

118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12, Ground False ("0") exceeds 16.0 VDC, and Ground True (“1”) is less than 8.0 VDC.

11.4.8.2 Serial Communication Circuitry

The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. HAR 1 Harness shall be 23 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to SP5 being routed to the FCU Controller interface, the SP3 EIA-485 Signal lines shall be routed only to the EX1 Connector.

11.4.9 EIA-232 Serial Port

An EIA-232 Serial Port on the FCU shall be provided with baud rate selection by Shunt of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector. This hardware is provided for future expansion capability and its use/protocol is currently undefined.

11.4.10 HAR 2 Harness

A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces between the 2070 UNIT and the outside world. The two EG (Equipment Ground) lines within HAR 2 shall be connected between EX2 and the 2070-8 module chassis.

11.4.11 Fault and Voltage Monitor Circuitry

NEMA TS1 Controller Fault and Voltage Monitor functions (outputs to cabinet monitor) shall be provided.

11.4.11.1 OR Gates

Conceptually, two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (Fault Monitor) and gate 2 output shall be connected to Connector A, Pin C. Any False state input shall cause a gate output False (+24VDC) state.

11.4.11.2 FCU Output O78

The FCU output O78 shall normally change its state every 100 ms. A module Watchdog circuit shall monitor the output. No state change for 2 ±0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the Watchdog output shall return to TRUE (0 VDC) state.

11.4.11.3 Operation

The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (±0.25). If the voltage exceeds the limits, the circuit output shall generate a False output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

11.4.11.4 Microprocessor Output

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

11.4.11.5 Message Outputs

CPU Port 5 Set Output Command Message Outputs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

11.4.11.6 CPU / FCU Operations

CPU / FCU operation at POWER UP shall be as follows:

1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
2. CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and FCU responds to CPU with "E" bit reset.
3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
4. * If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
5. Performs items 2 & 3 above User Software.

11.4.11.7 CPU / FCU Communications

A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm. Loss Flag. FM and VM outputs shall be in FALSE state.

CHAPTER 11-SECTION 5
2070N1 DETAILS

***Notes: Module sheet metal tolerance shall be 0.015 inch or less.**

CHAPTER 12
REFER TO GREEN TECHNOLOGY BATTERY BACKUP SYSTEM SPECIFICATIONS

CHAPTER 13
REFER TO MODEL 700 CHANGEABLE MESSAGE SIGN SPECIFICATIONS

APPENDIX A
CHAPTER DETAILS

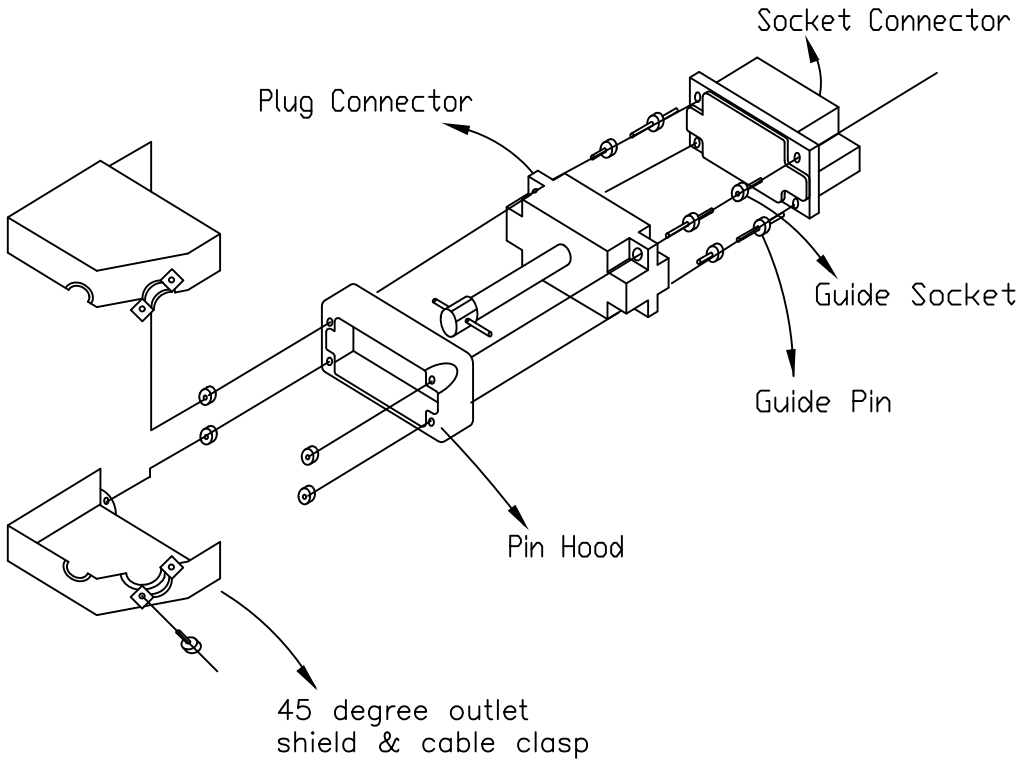
APPENDIX A1
CHAPTER 1 DETAILS

Section Notes:

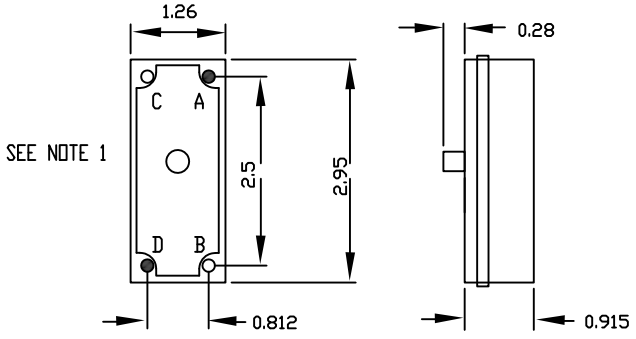
M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 Mega Ohms. The contacts shall be secured in the blocks with stainless steel springs.

M Type connector corner guides shall be stainless steel. The guide pins shall be 27.86 in length and the guide sockets shall be 15.66 in length.

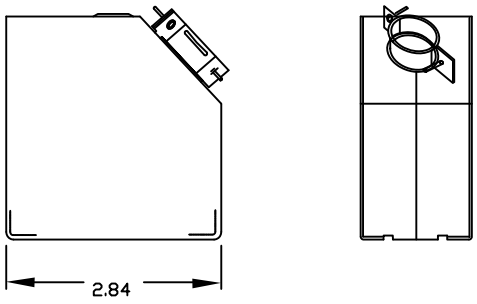
Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated, heat stabilized and fire resistant.



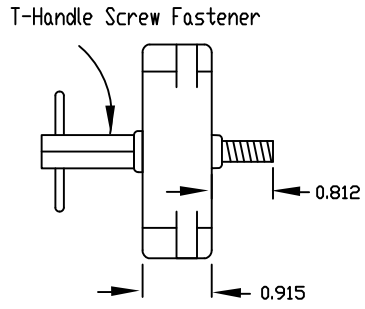
M104 CONNECTOR C1 DETAIL

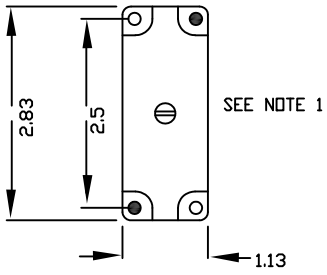


M104 SOCKET CONNECTOR

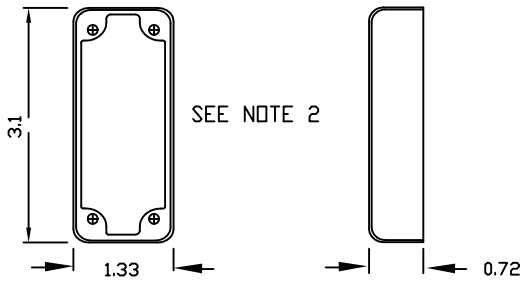


M104 SHIELD





CONNECTOR C1P

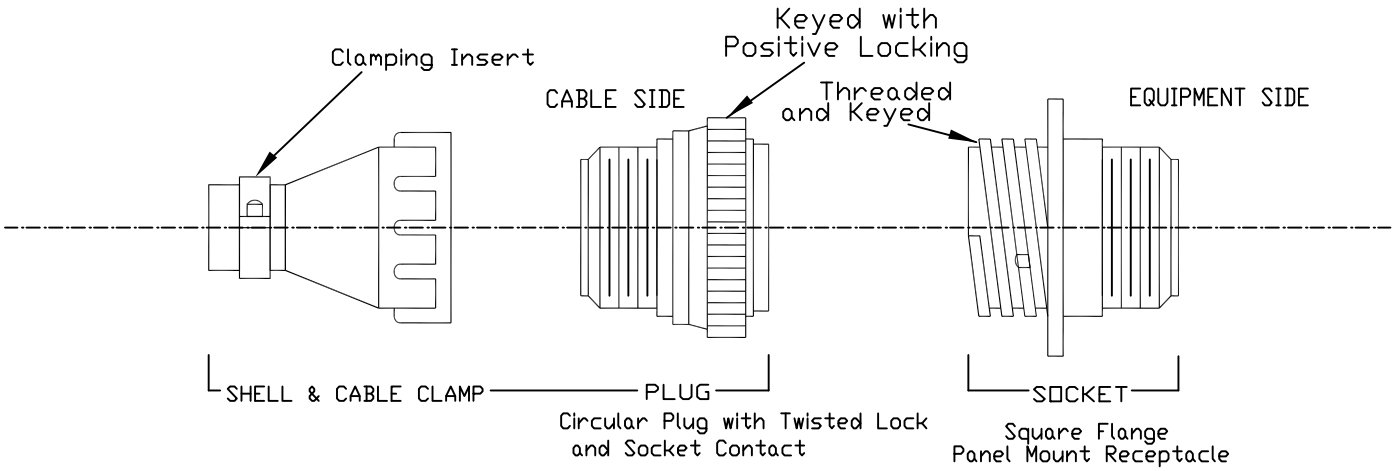


M104 HOOD

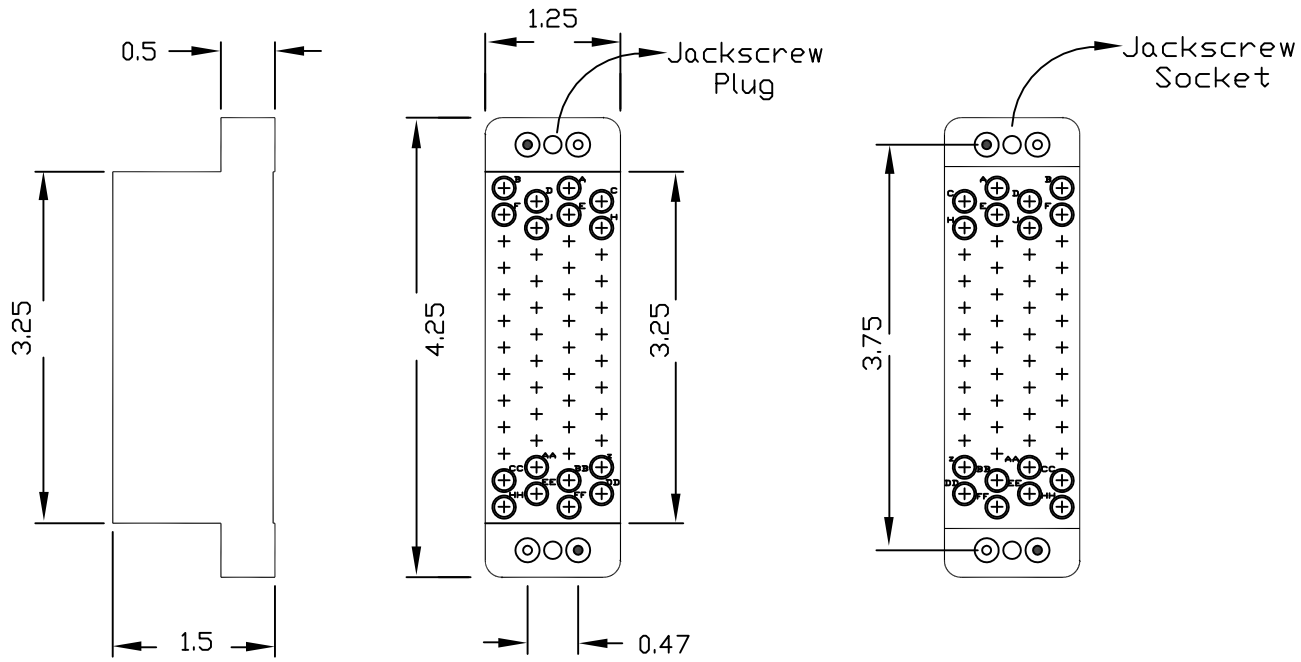
NOTES:

1. The darker circles denote guide pin location and the open circles are guide sockets.
2. Provide clearance for M104 plug with hood when mounting to it's socket.
3. All dimensions shown are in inches.

TITLE: CONNECTOR DETAIL-M104	
	NO SCALE
TEES 2020	A1-1



PLASTIC CIRCULAR PLUG AND SOCKET CONNECTOR



CONNECTOR PIN ARRANGEMENT

NOTES:

1. Guide Pins & Sockets, and Jackscrews are centered symmetrical to connector.
2. Key: – socket
   – plug
3. All dimensions shown are in inches.

TITLE: CONNECTOR DETAIL M50 & CIRCULAR PLASTIC CONNECTOR	
	NO SCALE
TEES 2020	A1-2

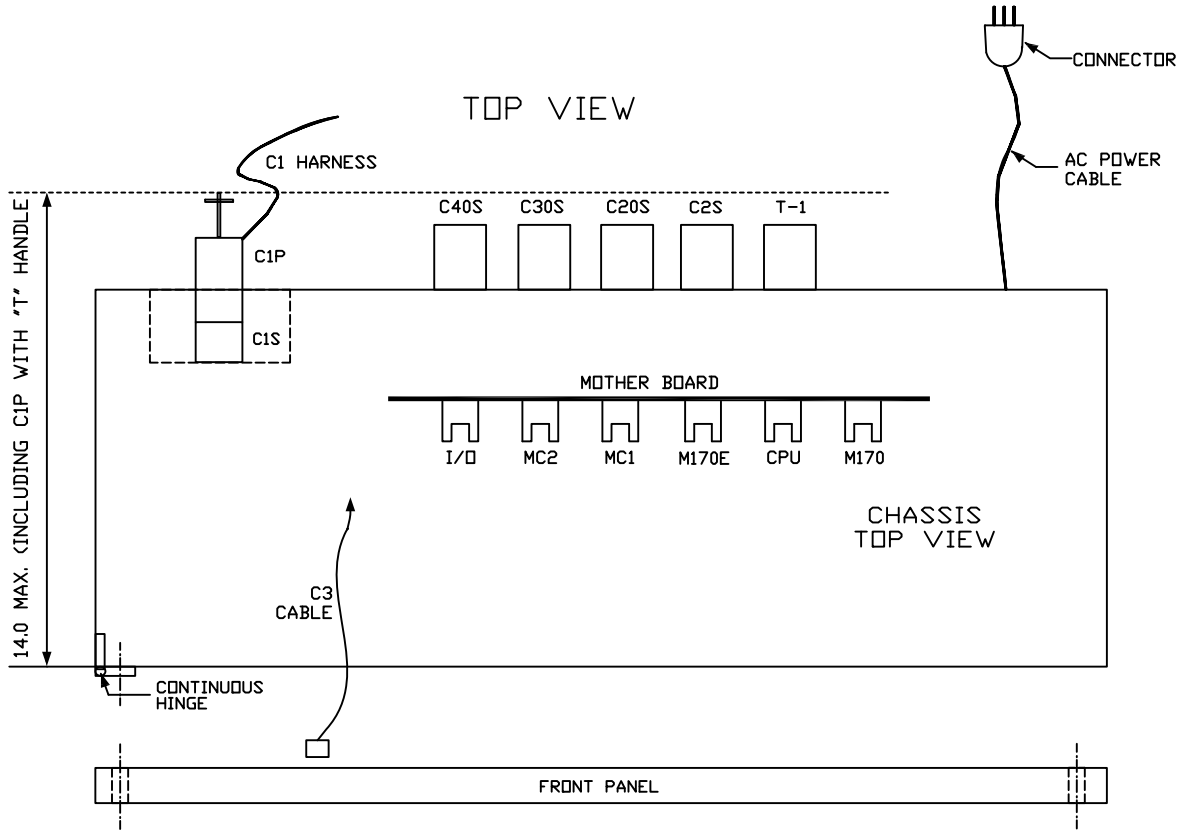
APPENDIX A2
CHAPTER 2 DETAILS

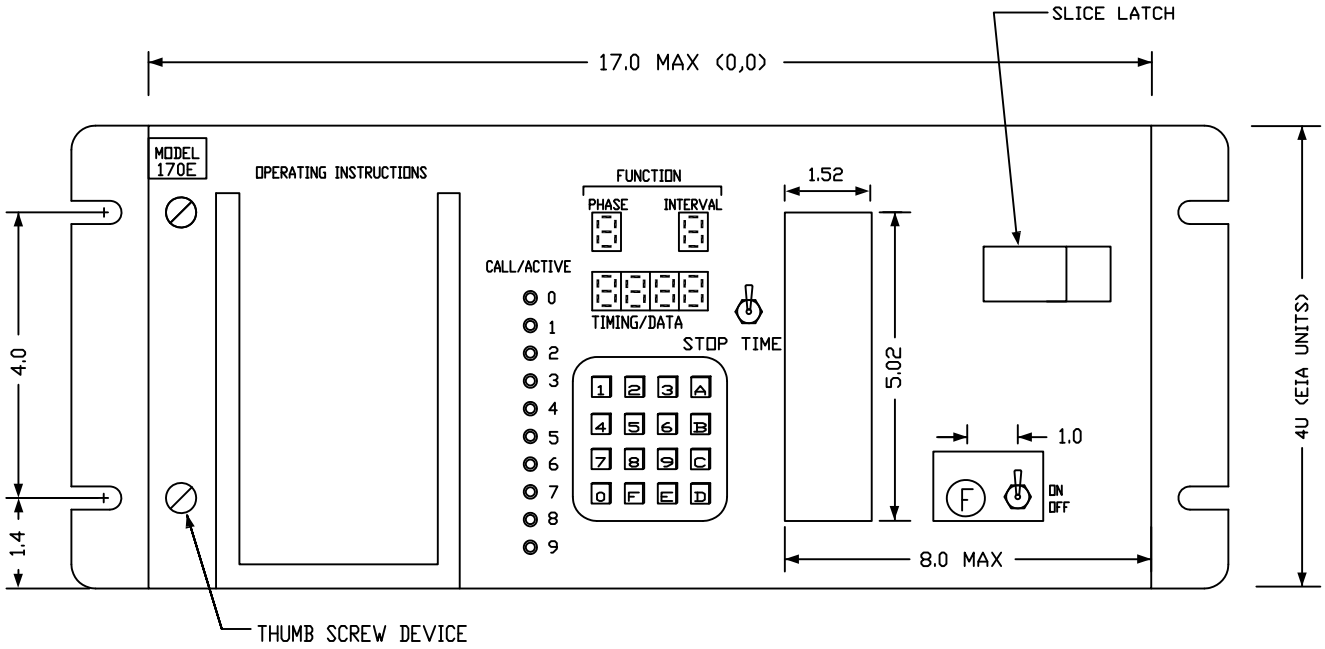
NOTES:

1. Program module' height and width dimensions are maximum.
2. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.
3. All function under connector C2 & the terminal block T-1 are in reference to the MODEM
4. Detail Definitions:

BL = BLANKING
CC = CHARACTER CONTROL OR STROBE
CD = CARRIER DETECT
CH = CHARACTER
CTS = CLEAR TO SEND
DP = DECIMAL POINT
LS = LEAST SIGNIFICANT
MS = MOST SIGNIFICANT
NA = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
NLS = NEXT LEAST SIGNIFICANT
NMS = NEST MOST SIGNIFICANT
P&I = PHASE AND INTERVAL
RTS = REQUEST TO SEND

MODEL 170E CONTROLLER UNIT DIAGRAM





FRONT PANEL DISPLAY AND UNIT DETAIL

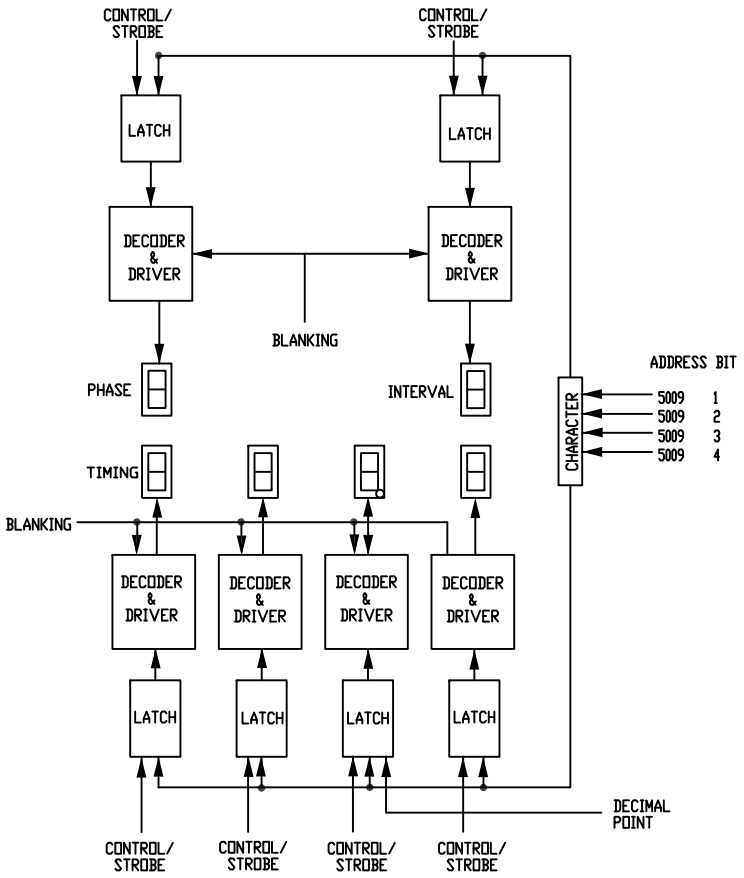
NOTE:

All dimensions shown are in inches.

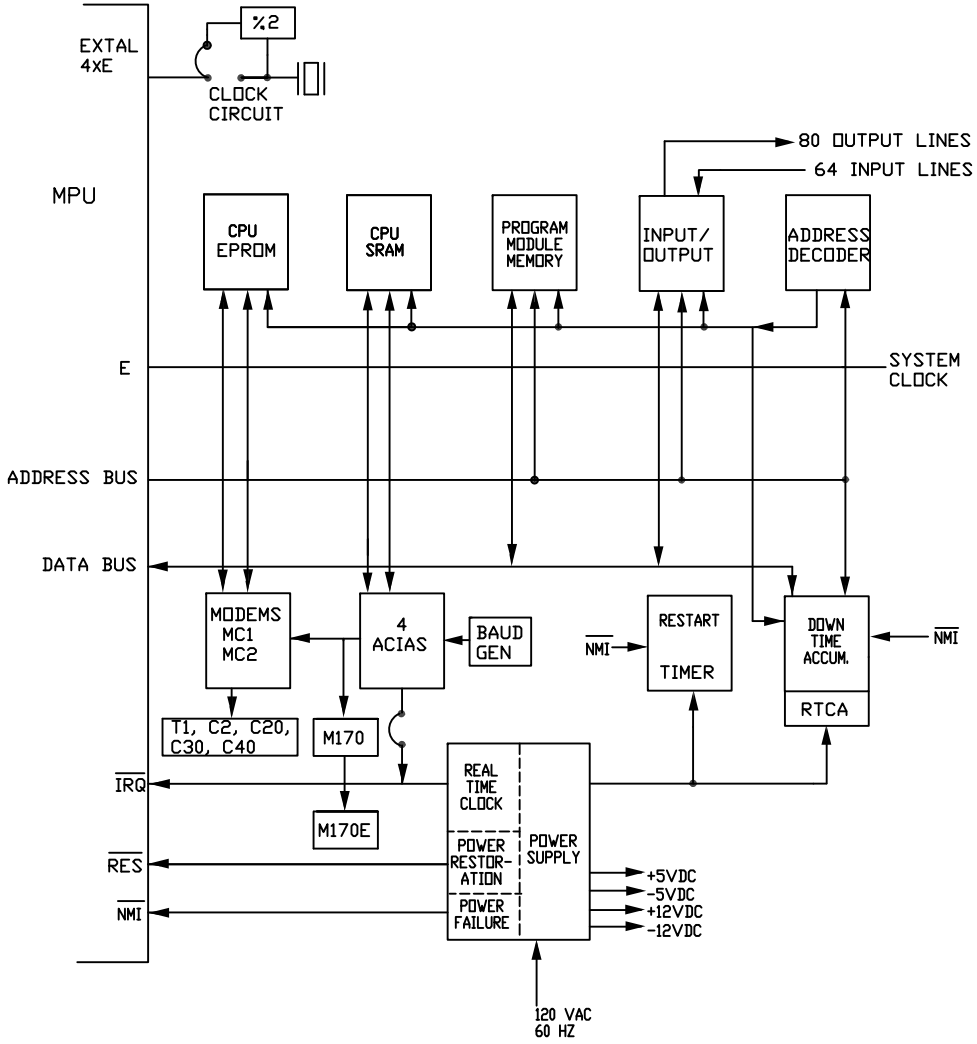
TITLE: MODEL 170E CONTROLLER UNIT DIAGRAM	
	NO SCALE
TEES 2020	A2-1

MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

FRONT PANEL DISPLAY BLOCK DIAGRAM



ORGANIZATION OF MODEL 170E CONTROLLER UNIT BLOCK DIAGRAM



TITLE:
MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

TEES 2020

NO SCALE

A2-2

INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

INPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET	C3 CONTACTS
5001	1	39	
5001	2	40	
5001	3	41	
5001	4	42	
5001	5	43	
5001	6	44	
5001	7	45	
5001	8	46	
5002	1	47	
5002	2	48	
5002	3	49	
5002	4	50	
5002	5	51	
5002	6	52	
5002	7	53	
5002	8	54	
5003	1	55	
5003	2	56	
5003	3	57	
5003	4	58	
5003	5	59	
5003	6	60	
5003	7	61	
5003	8	62	
5004	1	NA	
5004	2	NA	
5004	3	NA	
5004	4	NA	
5004	5	63	
5004	6	64	
5004	7	65	
5004	8	66	

INPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET	C3 CONTACTS
5005	1	67	
5005	2	68	
5005	3	69	
5005	4	70	
5005	5	71	
5005	6	72	
5005	7	73	
5005	8	74	
5006	1	75	
5006	2	76	
5006	3	77	
5006	4	78	
5006	5	79	
5006	6	80	
5006	7	81	
5006	8	82	
5007	1		KEYBORAD CONTROL
5007	2		KEYBOARD CH LS
5007	3		KEYBOARD CH NLS
5007	4		KEYBOARD CH NMS
5007	5		KEYBOARD CH MS
5007	6		STOP TIMING
5007	7		NA
5007	8		NA
5008	1		NA
5008	2		NA
5008	3		NA
5008	4		NA
5008	5		NA
5008	6		NA
5008	7		NA
5008	8		NA

CONNECTOR C2 SOCKET ASSIGNMENT (C20, C30 & C40) C2	
SOCKET CONTACT	FUNCTION
A	Audio In
B	Audio In
C	Audio Out
D	+5VDC
E	Audio Out
F	−5VDC
H	CD
J	RTS
K	Data IN
L	Data OUT
M	CTS
N	DC GND
P	NA
R	NA

TERMINAL BLOCK T−1 ASSIGNMENTS	
1	Audio In
2	Audio In
3	CD
4	RTS
5	Data IN
6	CTS
7	Data Out
8	Audio Out
9	Audio Out
10	DC GND

TITLE: MODEL 170E INPUT ADDRESS	
	NO SCALE
TEES 2020	A2−3

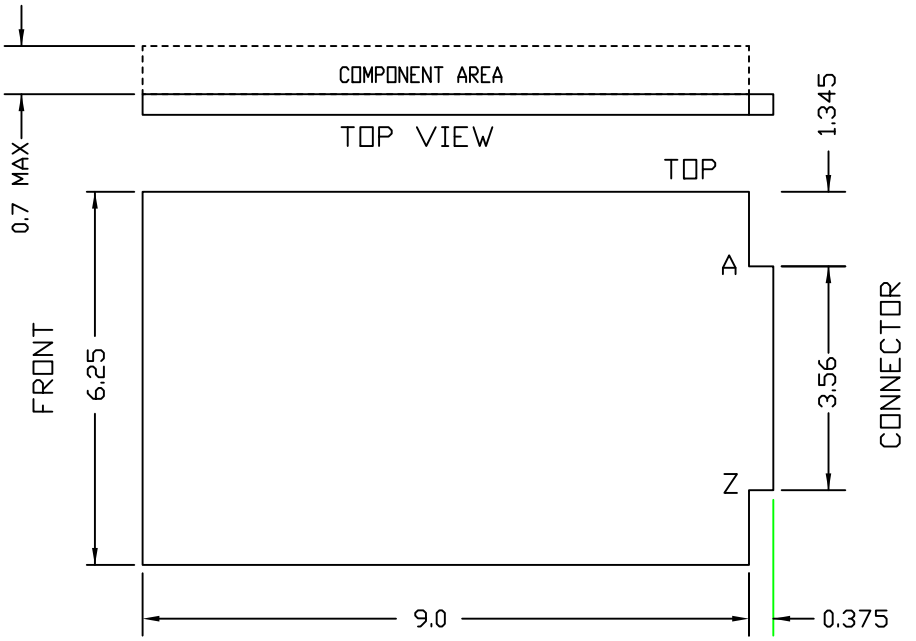
OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

Output Port Address	Bit	Connector C1 Socket Contacts
5001	1	2
5001	2	3
5001	3	4
5001	4	5
5001	5	6
5001	6	7
5001	7	8
5001	8	9
5002	1	10
5002	2	11
5002	3	12
5002	4	13
5002	5	15
5002	6	16
5002	7	17
5002	8	18
5003	1	19
5003	2	20
5003	3	21
5003	4	22
5003	5	23
5003	6	24
5003	7	25
5003	8	26
5004	1	27
5004	2	28
5004	3	29
5004	4	30
5004	5	31
5004	6	32
5004	7	33
5004	8	34
5005	1	35
5005	2	36
5005	3	37
5005	4	38
5005	5	100
5005	6	101
5005	7	102
5005	8	103

Output Port Address	Bit	Connector	
		C1	C3
		Socket Contacts	
5006	1	83	
5006	2	84	
5006	3	85	
5006	4	86	
5006	5	87	
5006	6	88	
5006	7	89	
5006	8	90	
5007	1	91	
5007	2	93	
5007	3	94	
5007	4	95	
5007	5	96	
5007	6	97	
5007	7	98	
5007	8	99	
5008	1		CC-PHASE
5008	2		CC-INTERVAL
5008	3		CC-TIMING LS
5008	4		CC-TIMING NLS
5008	5		CC-TIMING MLS
5008	6		CC-TIMING MS
5008	7		CALL LT 8
5008	8		CALL LT 9
5009	1		CH-LS
5009	2		CH-NLS
5009	3		CH-NMS
5009	4		CH-MS
5009	5		DP
5009	6		BL-P&I
5009	7		BL-TIMING
5009	8		NA
500A	1		CALL LT 0
500A	2		CALL LT 1
500A	3		CALL LT 2
500A	4		CALL LT 3
500A	5		CALL LT 4
500A	6		CALL LT 5
500A	7		CALL LT 6
500A	8		CALL LT 7

TITLE: OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 & C3	
	NO SCALE
TEES 2020	A2-4

MODEL 400, 400B & 400BE MODEM MODULE



SIDE VIEW

MODEL 400, 400B & 400BE MODULE CONNECTOR ASSIGNMENT

COMPONENT SIDE

CONTACT	MODEL 400 FUNCTION
1	NA
2	AUDIO INPUT
3	AUDIO INPUT
4	NA
5	NA
6	NA
7	NA
8	NA
9	NA
10	NA
11	NA
12	NA
13	NA
14	NA
15	NA
16	NA
17	NA
18	NA
19	NA
20	NA
21	NA
22	NA

CIRCUIT SIDE

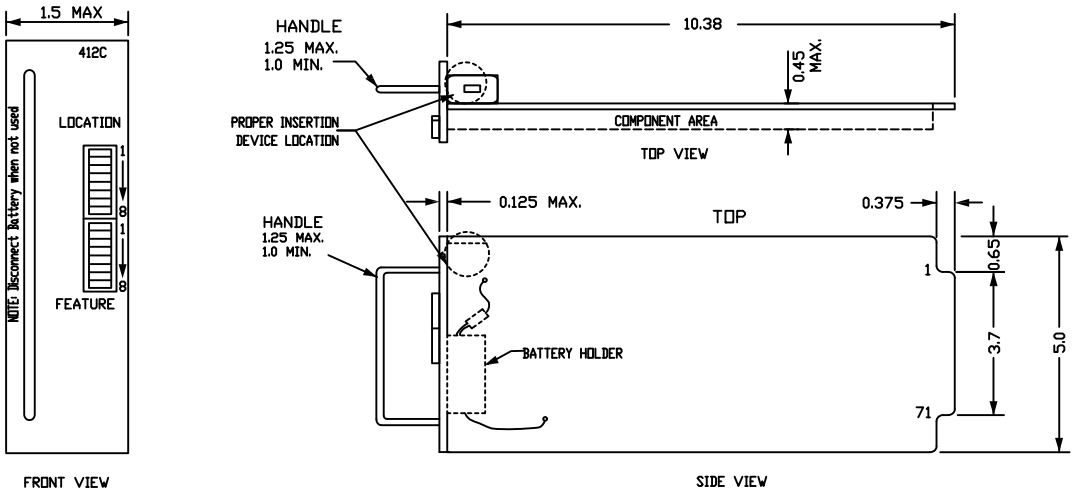
CONTACT	MODEL 400 FUNCTION
A	DC GROUND
B	DC GROUND
C	12 VDC
D	12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	CARRIER DETECT
L	REQUEST TO SEND
M	DATA INPUT
N	CLEAR TO SEND
P	DATA OUTPUT
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	AUDIO OUTPUT
Y	AUDIO OUTPUT
Z	NA

NOTE:

All dimensions shown are in inches.

TITLE: MODEL 400, 400B & 400BE MODEM MODULE	
	NO SCALE
TEES 2020	A2-5

MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E



M170, M170E, AND 412C
PROGRAM MODULE CONNECTOR ASSIGNMENTS

CIRCUIT SIDE		COMPONENT SIDE		M170 ONLY
FUNCTION	PCB CONNECTOR		FUNCTION	NOT REQUIRED BY 412C
A0	1	2	A1	
A2	3	4	A3	
A4	5	6	A5	
A6	7	8	A7	
A8	9	10	A9	
A10	11	12	A11	
A12	13	14	A13	
A14	15	16	A15	
$\overline{D0}$	17	18	$\overline{D1}$	
$\overline{D2}$	19	20	$\overline{D3}$	
$\overline{D4}$	21	22	$\overline{D5}$	
$\overline{D6}$	23	24	$\overline{D7}$	
$\overline{VMA}$ / Q2(E)	25	26	NA	RES
READ/WRITE	27	28	NA	NMI
NA	29	30	NA	ROT
NA	31	32	NA	
NA	33	34	EQUIP. GND	
NA	35	36	NA	RTS ACIA 4
NA	37	38	NA	CTS ACIA 4
NA	39	40	NA	DCD ACIA 4
NA	41	42	NA	TXD ACIA 4** (SEE NOTE)
NA	43	44	NA	RXD ACIA 4** (SEE NOTE)
NA	45	46	NA	
NA	47	48	NA	
NA	49	50	NA	
NA	51	52	NA	
NA	53	54	NA	
NA	55	56	NA	
NA	57	58	NA	
12 VDC	59	60	12 VDC	
-12 VDC	61	62	-12 VDC	
	KEY			
-5 VDC	63	64	-5 VDC	
5 VDC	65	66	5 VDC	
5 VDC	67	68	5 VDC	
GND	69	70	GND	
GND	*71	*72	GND	

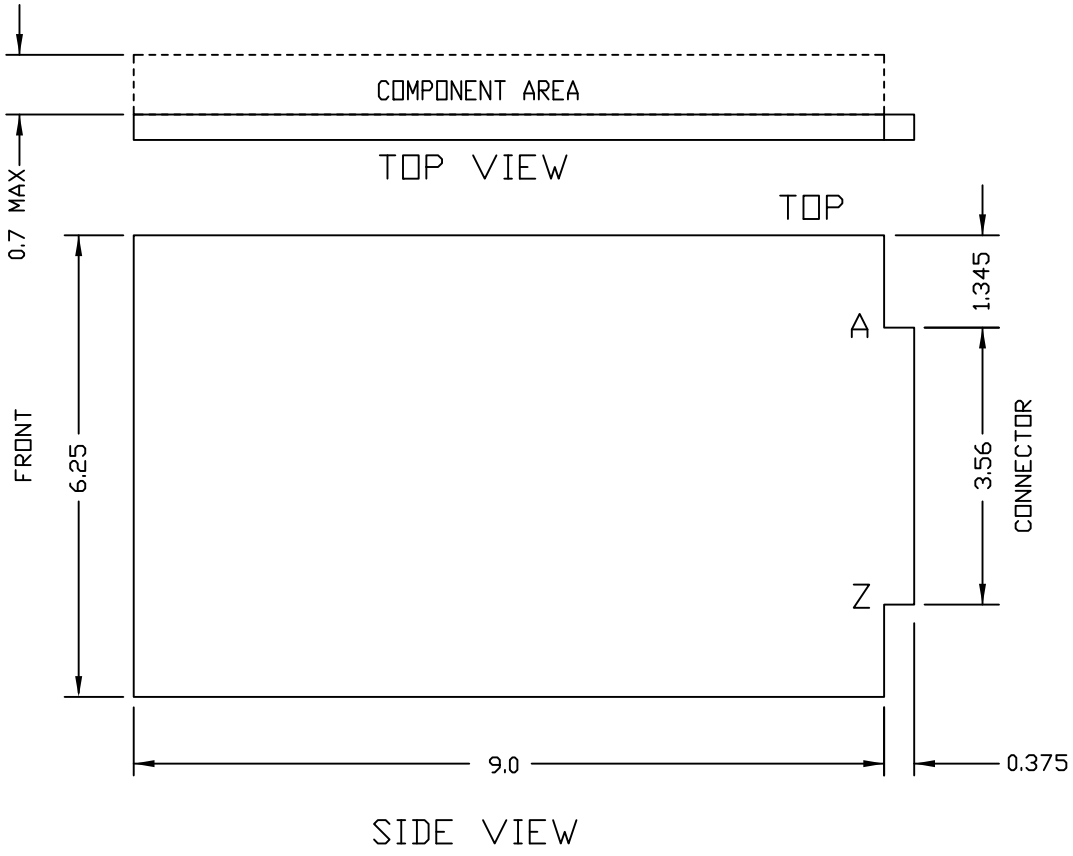
NOTES:

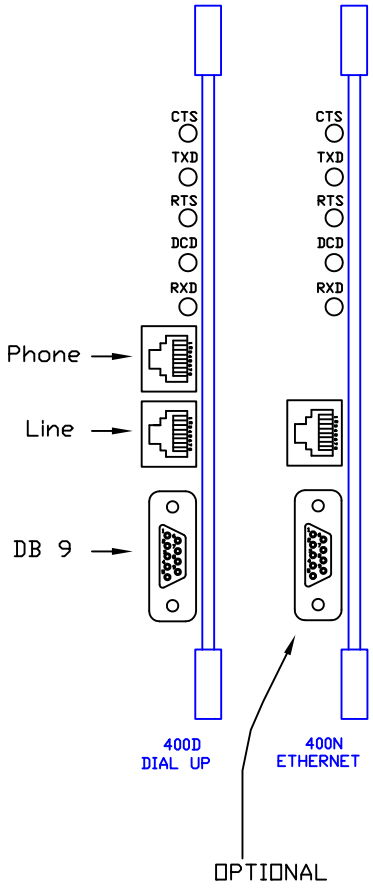
* Pins 71 & 72 on M170 & 170E connectors shall be commoned. Pins 71 & 72 on the Model 412C shall be tied to pins 69 & 70.

** Relative to the ACIA.

1. All dimensions shown are in inches.
2. "U" shape rod handle shall be fabricate of 0.18 in to 0.26 in diameter, Aluminum stock.
3. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E	
	NO SCALE
TEES 2020	A2-6





CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA

DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

RJ45 ETHERNET PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	NA
3	RX +	7	NA
4	RX-	8	NA

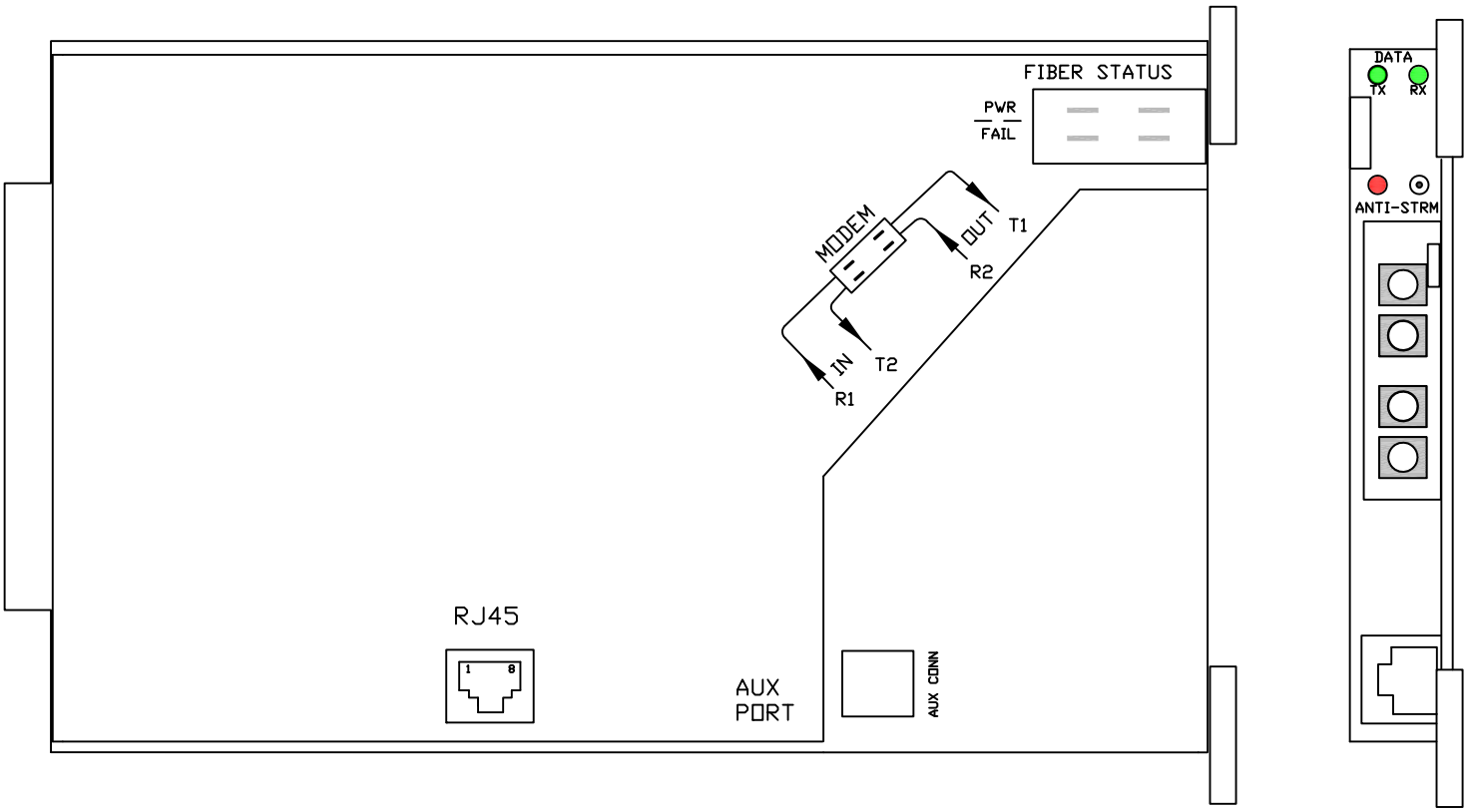
NOTE:

All dimensions shown are in inches.

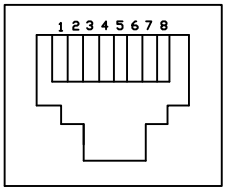
TITLE:

MODEL 400D & 400N

	NO SCALE
TEES 2020	A2-7



CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA



RJ45 (detail)

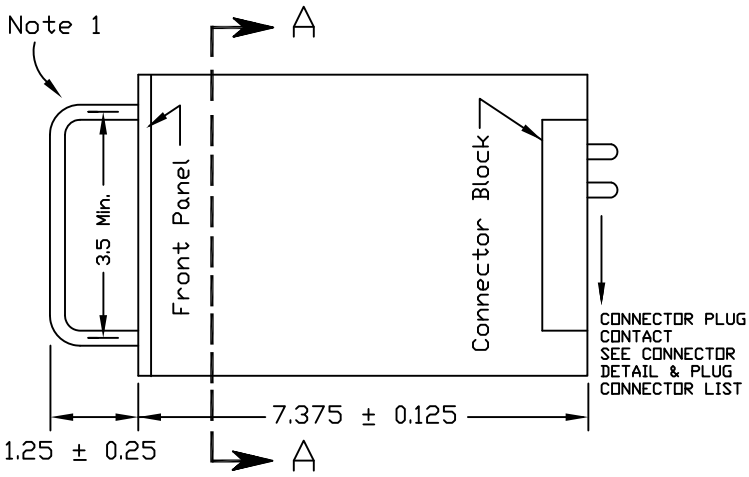
RJ45 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	NA	5	RXD
2	CD	6	TXD
3	NA	7	CTS
4	GND	8	RTS

TITLE:

MODEL 400F FIBER MODULE

	NO SCALE
TEES 2020	A2-8

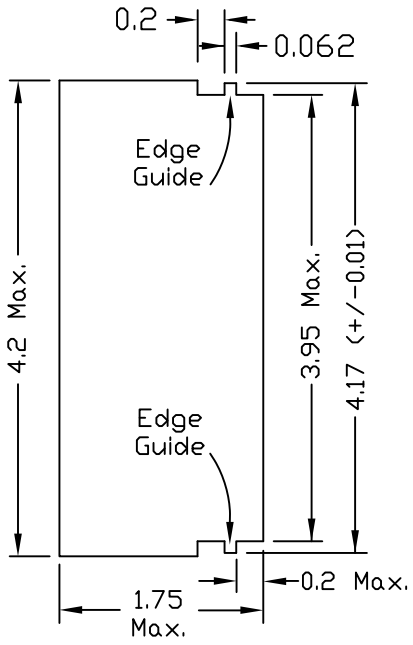
APPENDIX A3
CHAPTER 3 DETAILS



SIDE VIEW

MODEL 200 CONNECTOR DETAIL

PIN	FUNCTION
1	AC+
2	Equip. Ground
3	Red Output
4	Not Assigned
5	Yellow Output
6	Red Input
7	Green Output
8	Yellow Input
9	+24 VDC
10	Green Input
11	Not Assigned
12	Not Assigned



CROSS SECTION A-A

MODEL 204 CONNECTOR DETAIL

PIN	FUNCTION
7	Load Circuit #1
8	Load Circuit #2
9	Equip. Ground
10	AC-
11	AC+
12	Not Assigned

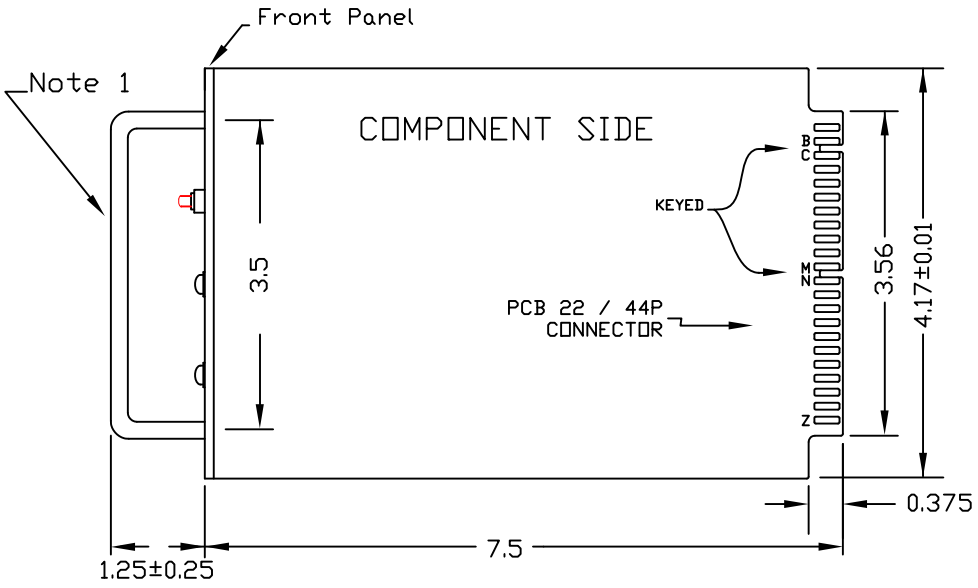
PLUG CONNECTOR LIST

MODEL 200 - BEAU P-5412-LAB (Or Equal)
MODEL 204 - BEAU P-5406-LAB (Or Equal)

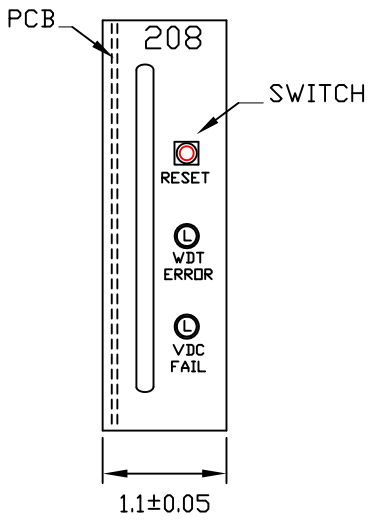
NOTES:

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26in diameter, Aluminum stock to form a handle.
2. Front Panel shall be Aluminum stock or Stainless Steel.
3. All dimensions shown are in inches.

TITLE: MODEL 200 SWITCH PACK & 204 FLASHER CONNECTOR DETAILS	
	NO SCALE
TEES 2020	A3-1



SIDE VIEW



FRONT VIEW

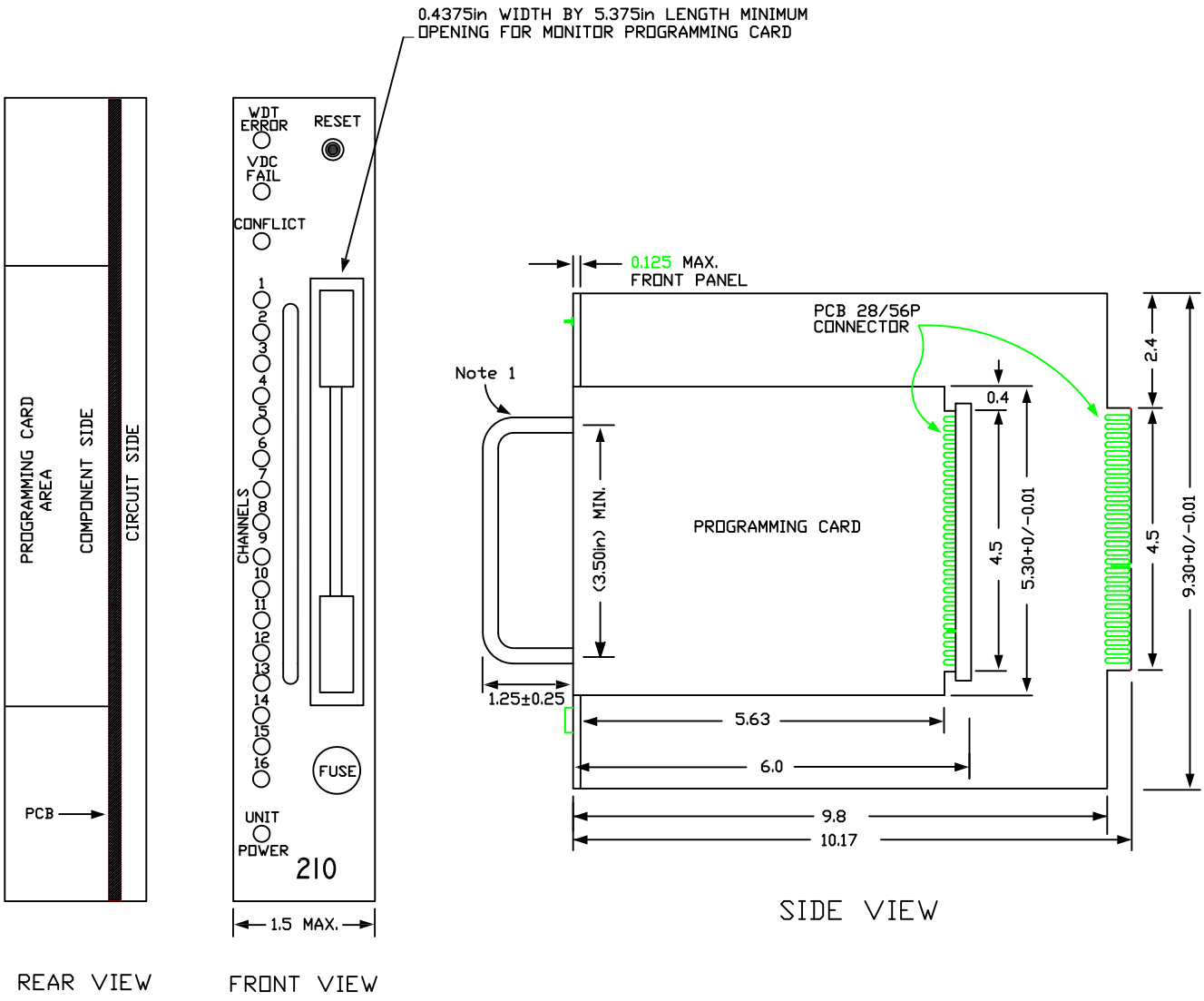
MODEL 208 MONITOR UNIT PIN ASSIGNMENT

PIN	FUNCTION
1 / A	DC GROUND
2 / B	WDT Ext. Reset
5 / E	WDT IN
10 / L	+24 VDC
15 / S	AC-
17 / U	Normally Open, Circ. #2
19 / W	AC+
20 / X	WDT Lamp (External)
21 / Y	Circ. Common #1 & #2
22 / Z	Normally Closed, Circ. #1

NOTES:

1. "U" shape rod handle shall be fabricate of 0.18 to 0.26 in diameter, Aluminum stock to form a handle.
2. Front panel shall be Aluminum stock or Stainless Steel.
3. All dimensions shall be in inches.

TITLE: MODEL 208 T170 MONITOR UNIT	
	NO SCALE
TEES 2020	A3-2



NOTES: (FOR DETAILS A3–3 & A3–4):

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter Aluminum stock or Stainless Steel to form a handle.
2. Model 210 tolerance dimensions are +/– 0.02 in except as noted.
3. Sheet definitions:
   ---= Slotted for keying.
   (C) = Collector
   (E) = Emitter
   * = NA for these connections on models 232 & 242.
4. All dimensions shown are in inches.

TITLE: MODEL 210 T170 MONITOR UNIT	
	NO SCALE
TEES 2020	A3-3

MODEL 210 MONITOR UNIT CONNECTOR WIRING ASSIGNMENTS

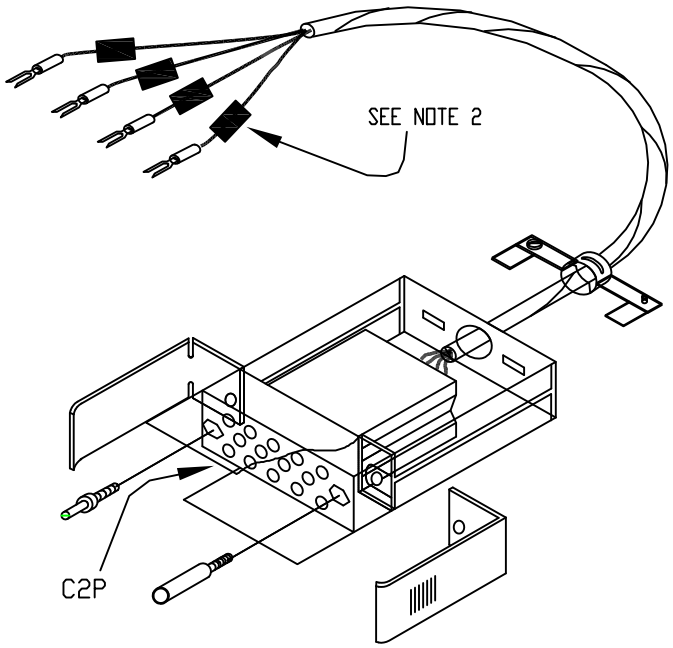
PIN	FUNCTION	PIN	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #6 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #8 Yellow	F	Channel #16 Green
7	Channel #5 Green	H	Channel #5 Yellow
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC− *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25 Tied together)	BB	Stop Time
25		CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

MODEL 210 PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

PIN	FUNCTION (Circuit Side)	PIN	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #16 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

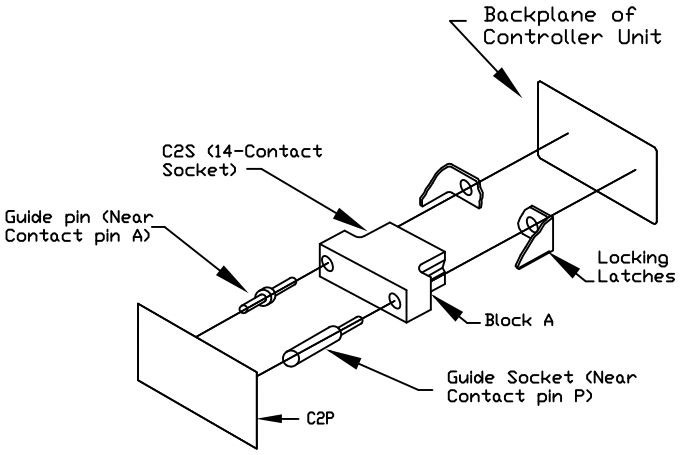
TITLE: MODEL 210 T170 MONITOR UNIT PROGRAMMING CARD CONNECTOR & WIRING ASSIGNMENTS

	NO SCALE
TEES 2020	A3-4

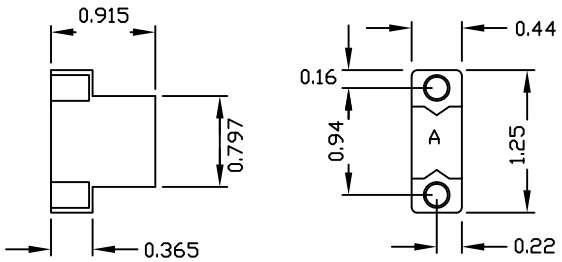


C2 MODEM HARNESS

C2P CONNECTOR ASSIGNMENT		
PIN	FUNCTION	WIRE COLOR
A	AUDIO IN	WHITE
B	AUDIO IN	BLACK
C	AUDIO OUT	RED
E	AUDIO OUT	GREEN



CONNECTOR C2 DETAIL



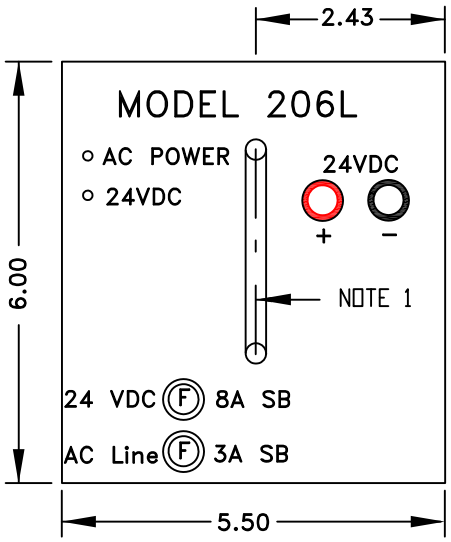
CONNECTOR C2S

NOTES:

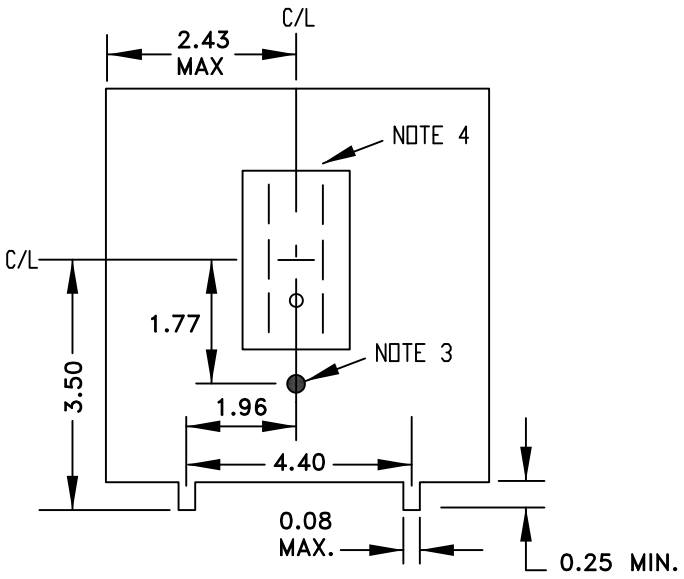
1. Cable length shall be 36.00in minimum. The cable shall be 2–pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.
2. Each conductor (AUDIO IN or AUDIO OUT) shall be labeled.
3. All dimensions shown are in inches.

TITLE: C2 MODEM HARNESS	
	NO SCALE
TEES 2020	A3-5

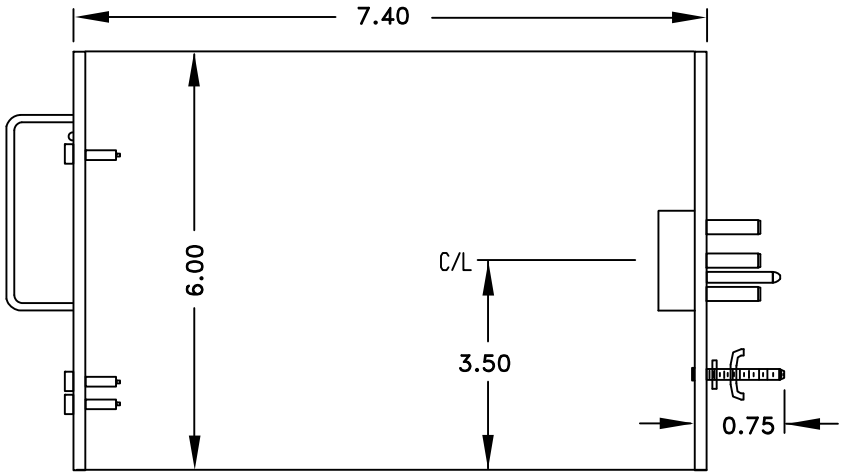
MODEL 206L POWER SUPPLY MODULE



FRONT VIEW

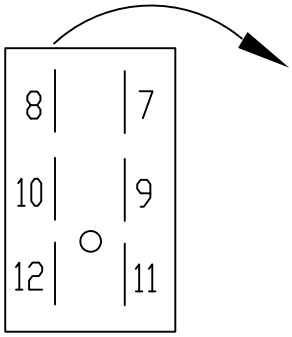


REAR VIEW



SIDE VIEW

POWER SUPPLY MODULE WIRING DETAIL



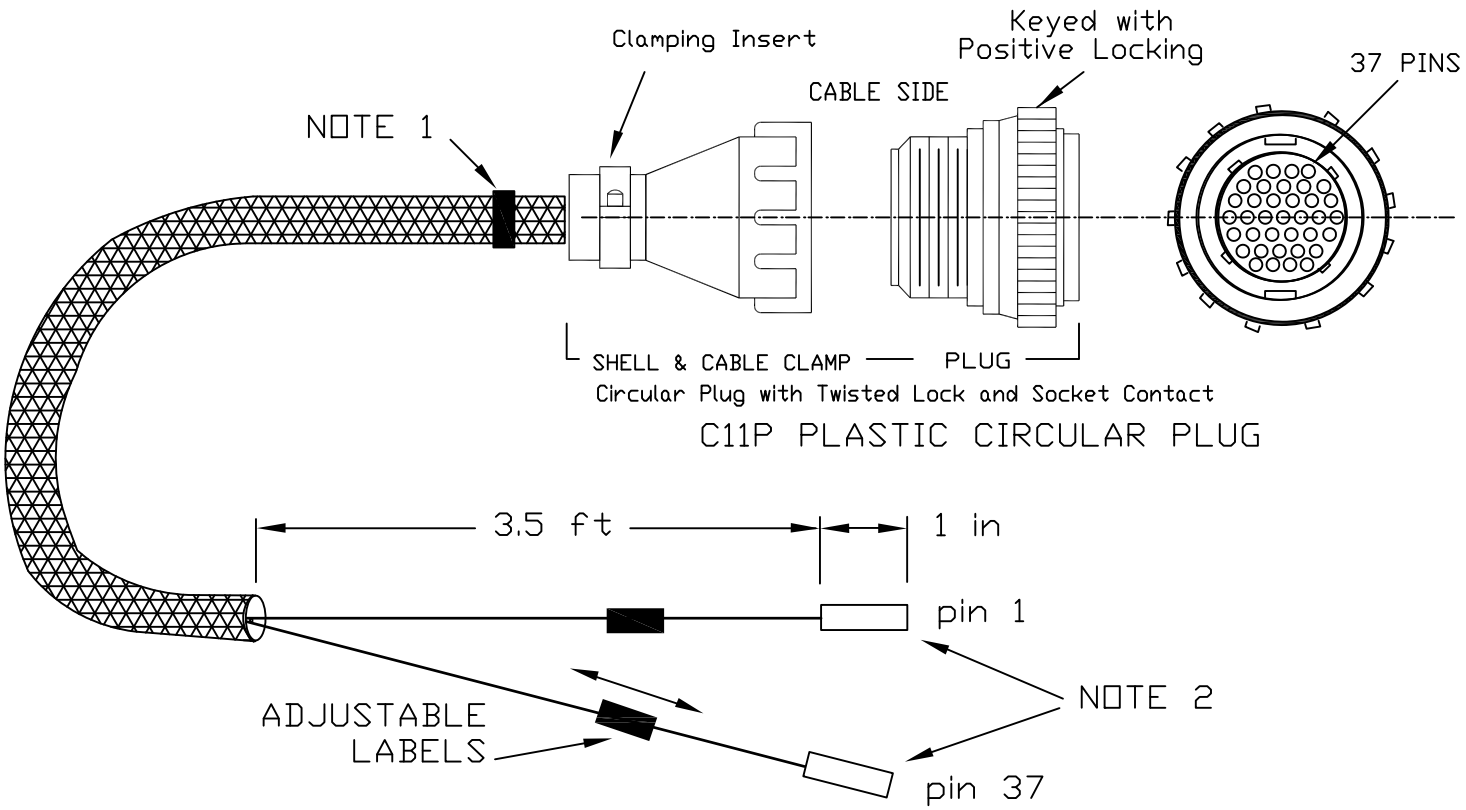
PIN NO.	CIRCUIT
7	+24 VDC
8	DC GND
9	EQUIPMENT GND
10	NA
11	AC− CLEAN
12	AC+ CLEAN

REAR VIEW

NOTE:

1. "U" shaped rod handle fabricated of 0.25±0.05 diameter, Aluminum stock, with 4.00±0.125 length, & rod center to center, shall be provided. The handle shall be vertically centered. The depth from the vertical centerline of the handle rod to the module from panel shall be 1.25±0.125.
2. The power supply module dimension, from front panel to connector plug, shall be 7.375 +0.000, −0.125.
3. A standard 8-32 metal stud retaining screw shall provide proper securing of the power supply when installed in the PDA using washers and a wingnut.
4. Connector BEAU P-5406 or equivalent.
5. Front panel shall be Aluminum stock or Stainless Steel.
6. All dimensions shown are in inches.

TITLE: MODEL 206L POWER SUPPLY	
	NO SCALE
TEES 2020	A3-6



C11P PIN ASSIGNMENT & LABELS

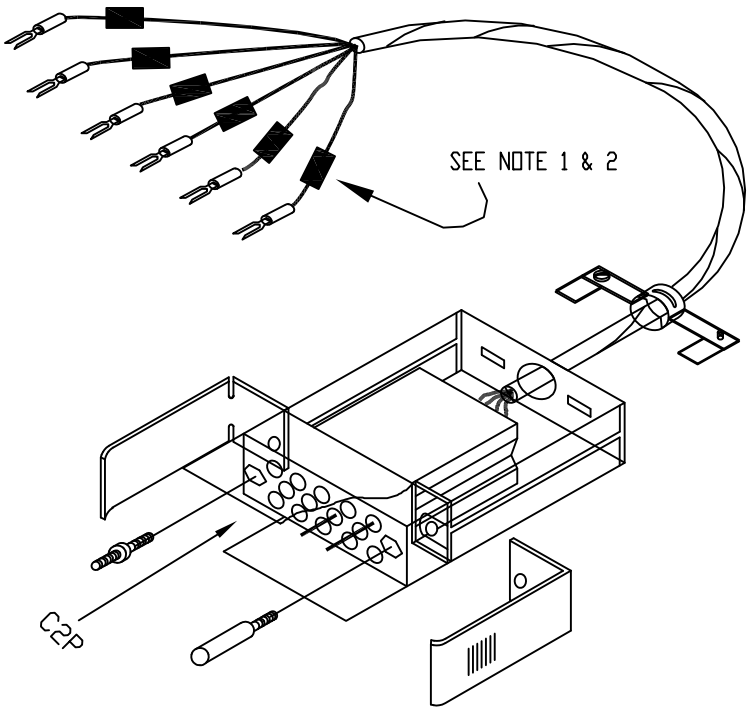
PIN 1 O8-1	PIN 11 I4-2	PIN 21 I7-7	PIN 31 DCG #2
PIN 2 O8-2	PIN 12 I4-3	PIN 22 I7-8	PIN 32 NC
PIN 3 O8-3	PIN 13 I4-4	PIN 23 I8-1	PIN 33 NC
PIN 4 O8-4	PIN 14 DCG #2	PIN 24 I8-2	PIN 34 NC
PIN 5 O8-5	PIN 15 I7-1	PIN 25 I8-3	PIN 35 NC
PIN 6 O8-6	PIN 16 I7-2	PIN 26 I8-4	PIN 36 NC
PIN 7 O8-7	PIN 17 I7-3	PIN 27 I8-5	PIN 37 NC
PIN 8 O8-8	PIN 18 I7-4	PIN 28 I8-6	
PIN 9 DCG #2	PIN 19 I7-5	PIN 29 I8-7	
PIN 10 I4-1	PIN 20 I7-6	PIN 30 I8-8	

TABLE 1

NOTES:

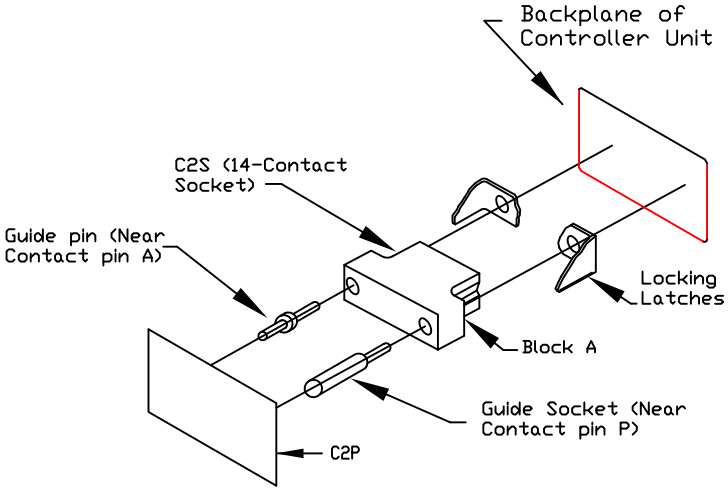
1. C11 label.
2. Heat shrinkable tubing.

TITLE: C11 HARNESS	
	NO SCALE
TEES 2020	A3-7

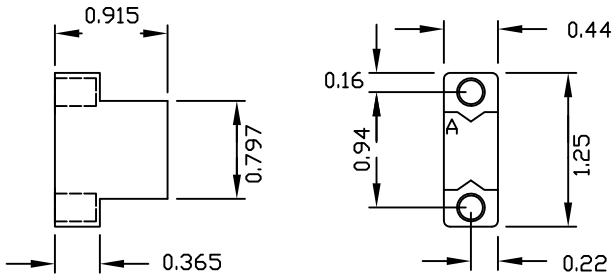


C2 SERIAL HARNESS

C2P CONNECTOR ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
A	NA	J	RTS
B	NA	K	RXD
C	NA	L	TXD
D	NA	M	CTS
E	NA	N	GND
F	NA	P	NA
H	DCD	R	NA



CONNECTOR C2 DETAIL

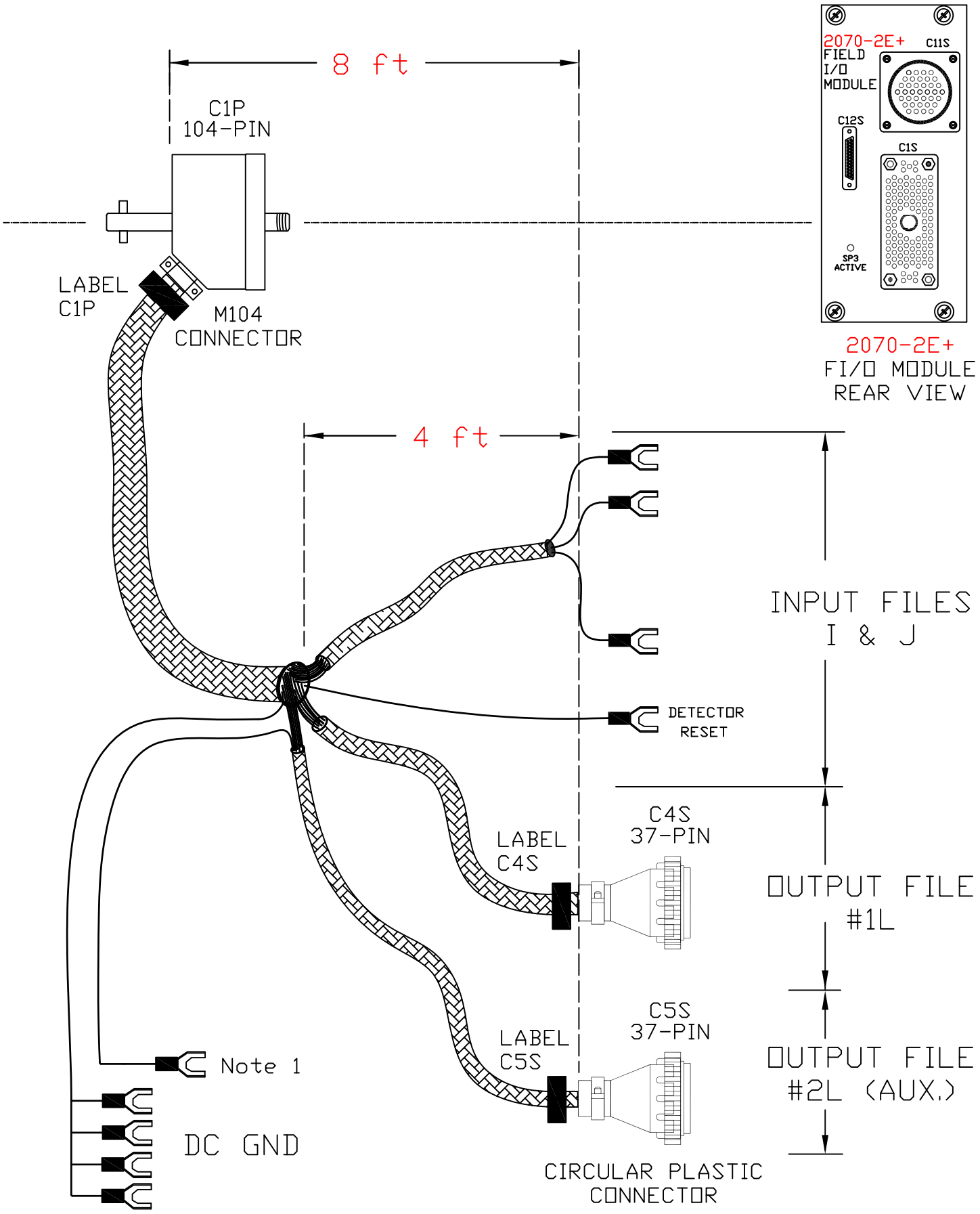


CONNECTOR C2S

NOTES:

1. Cable length shall be 36.00in minimum. The cable shall be 24AWG, 6 conductors, Belden 9536 or equal. The field end connections shall be #6 stud spring spade type.
2. Each conductor (DCD, RTS, RXD, TXD, CTS, GND) shall be labeled.
3. All dimensions shall be in inches.

TITLE: C2 SERIAL HARNESS	
	NO SCALE
TEES 2020	A3-8

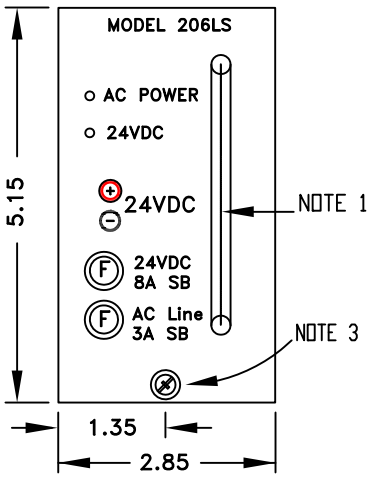


NOTE:

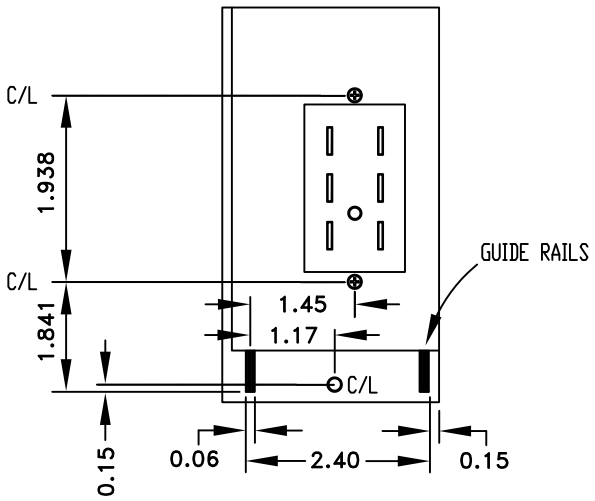
1. Input Panel #1, TB1 (+24VDC) to C5S, pin #24.

TITLE:	C1 HARNESS SIGNAL CABINET
	NO SCALE
TEES 2020	A3-9

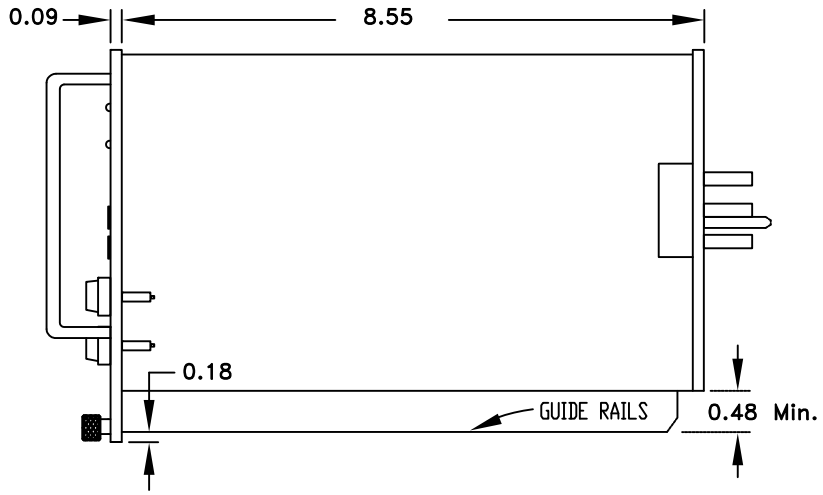
MODEL 206LS POWER SUPPLY MODULE



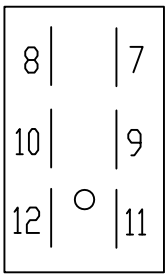
FRONT VIEW



REAR VIEW



SIDE VIEW



REAR VIEW

POWER SUPPLY MODULE WIRING DETAIL

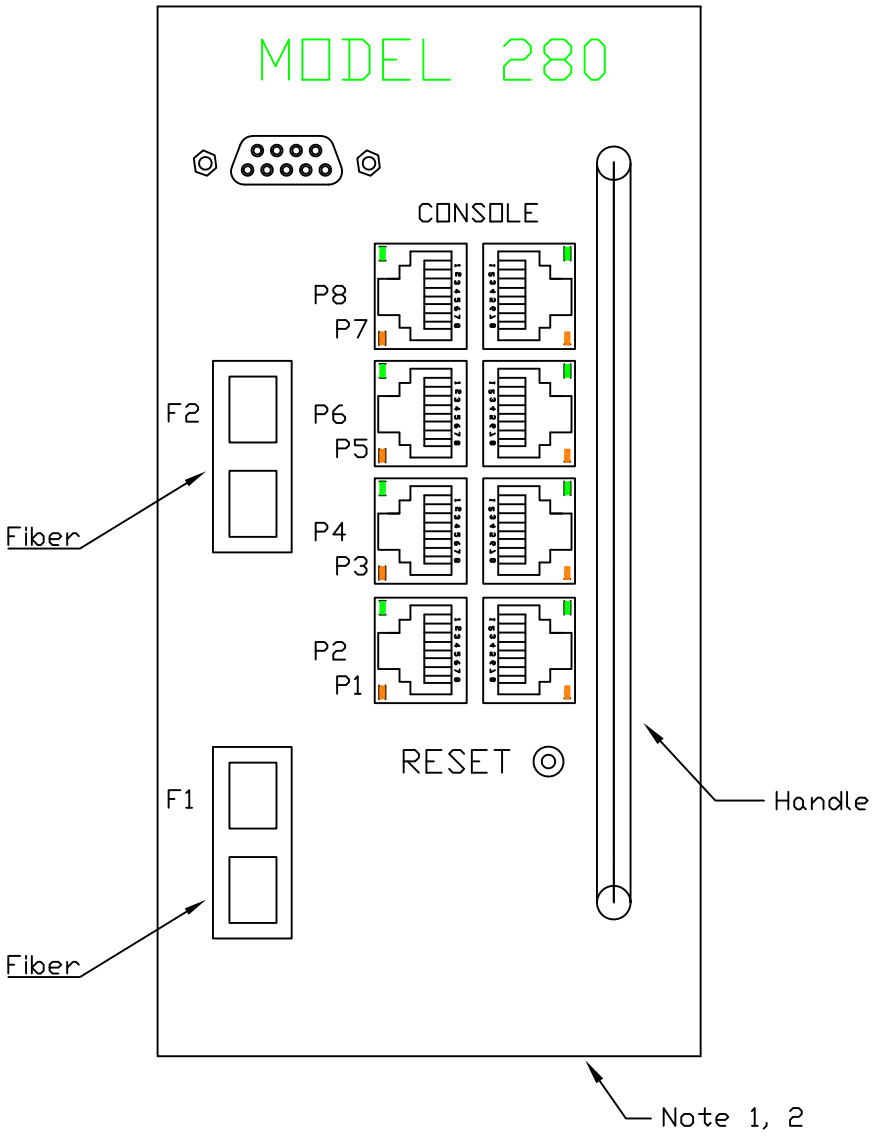
PIN NO.	FUNCTION
7	+24 VDC
8	DC GND
9	EG
10	NA
11	AC- CLEAN
12	AC+ CLEAN

NOTE:

1. "U" shaped rod handle fabricated of 0.25±0.05 diameter, Aluminum stock, with 4.00±0.125 length, & rod center to center shall be provided. The handle shall be vertically centered. The depth from the vertical centerline of the handle rod to the front panel shall be 1.25±0.125.
2. Power supply module dimension, from front panel to connector plug, shall be 8.64 +0.000, −0.125.
3. Thumb screw device, #10−32.
4. Connector BEAU P−5406 or equivalent.
5. Front panel shall be Aluminum stock or Stainless Steel.
6. All dimensions shown are in inches.

TITLE: MODEL 206LS POWER SUPPLY	
	NO SCALE
TEES 2020	A3-10

INPUT FILE ETHERNET SWITCH UNIT



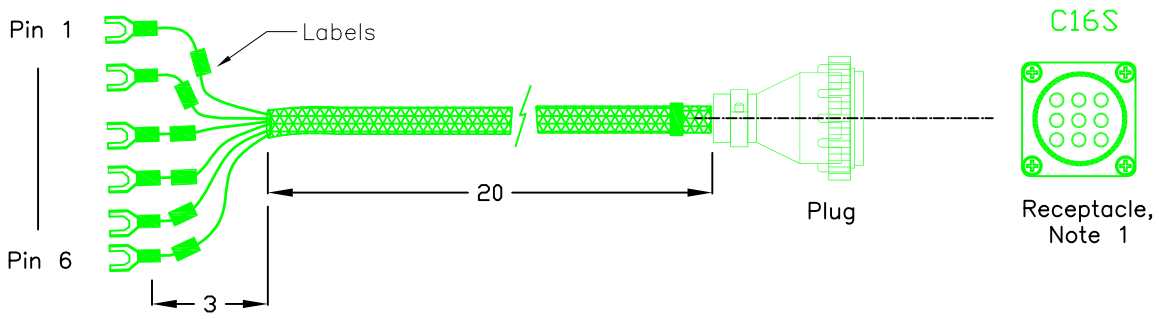
PORT 1-8 RJ45 PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

1. Four-channel card space, see A5-1 for dimensions.
2. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 280 INPUT FILE ETHERNET SWITCH UNIT	
	NO SCALE
TEES 2020	A3-11

C16 HARNESS



C16 Harness Pin Assignment		
PIN	FUNCTION	LABEL
1	APP IN	J-12D
2	GD IN	J-12J
3	SIM PRI	J-13D
4	SIM SEC	J-13J
5	ADV PRI	J-14D
6	ADV SEC	J-14J
7	NA	NA
8	NA	NA
9	NA	NA

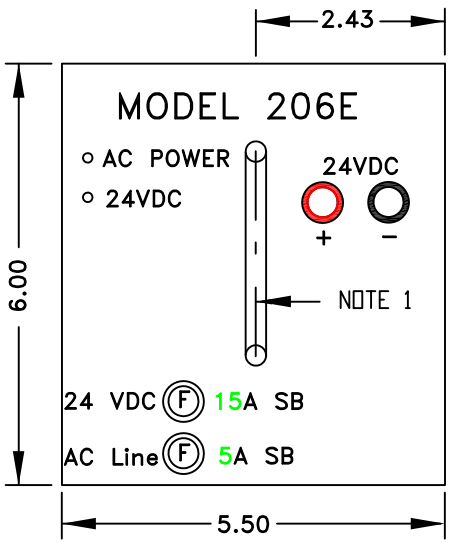
TYCO/AMP – Circular Plastic Connector (CPC)				
SHELL SIZE	NO. OF POSITION	KEY	RECEPTACLE	PLUG
13	9	-	206705-1	206708-1

NOTE:

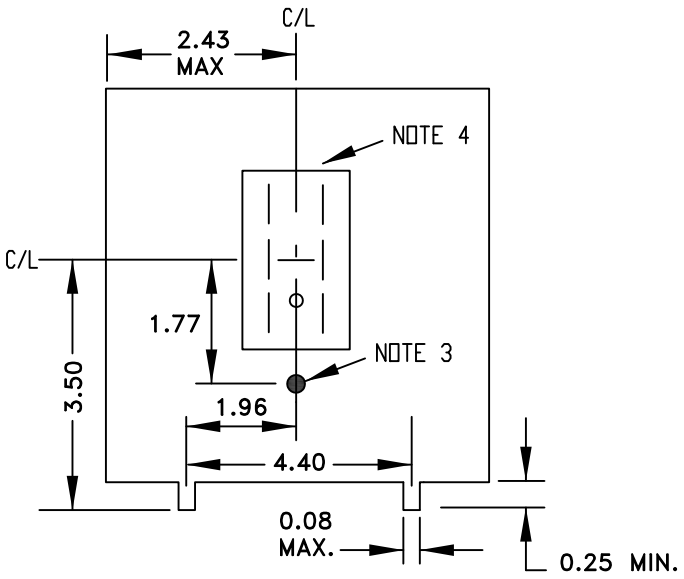
1. Panel Mount Receptacle, see A1-2 and A6-46 for details.
2. All dimensions shown are in inches

TITLE: C16 HARNESS DETAIL	
	NO SCALE
TEES 2020	A3-12

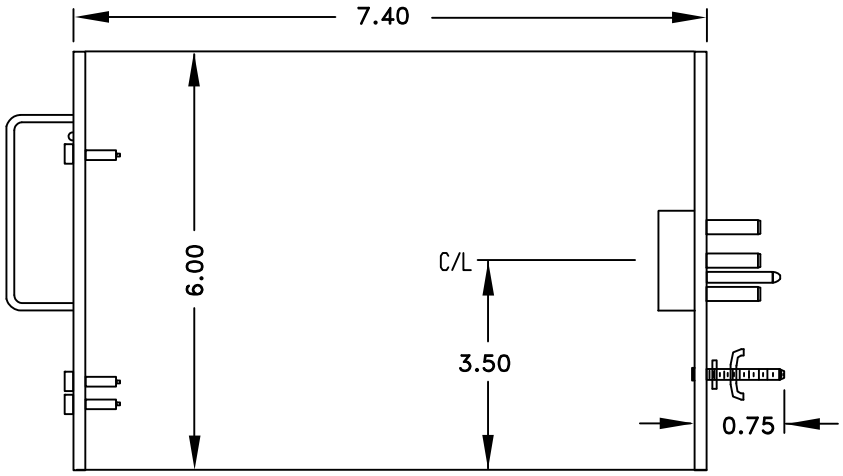
MODEL 206E POWER SUPPLY MODULE



FRONT VIEW

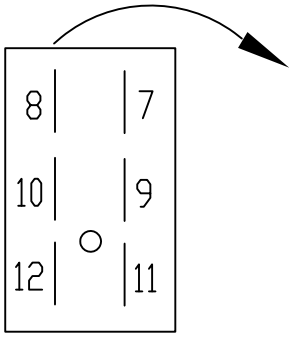


REAR VIEW



SIDE VIEW

POWER SUPPLY MODULE WIRING DETAIL



PIN NO.	CIRCUIT
7	+24 VDC
8	DC GND
9	EQUIPMENT GND
10	NA
11	AC− CLEAN
12	AC+ CLEAN

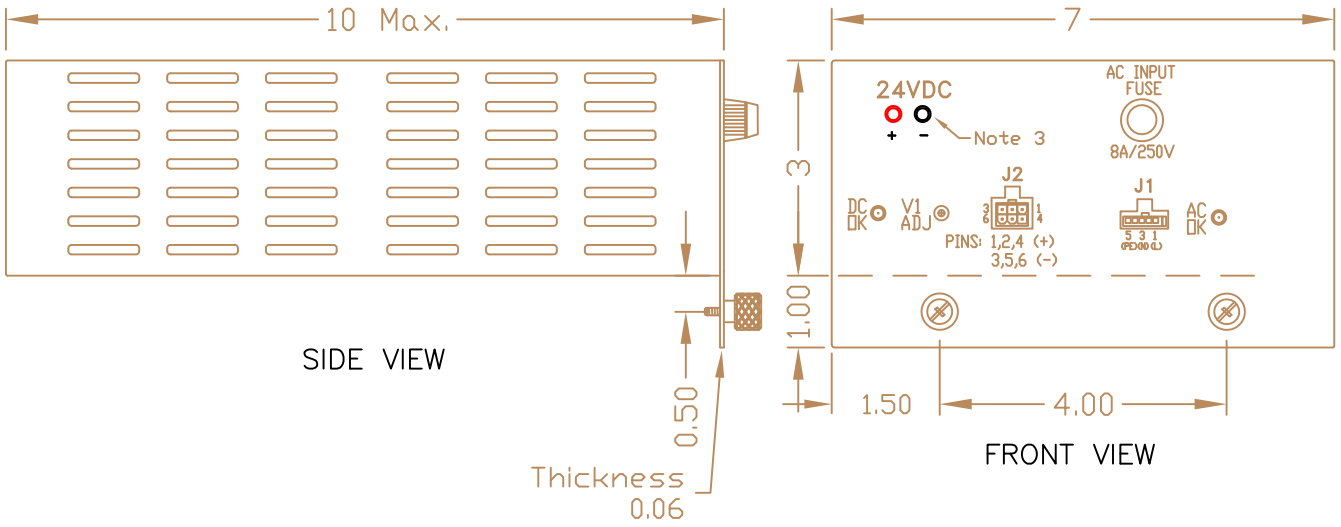
REAR VIEW

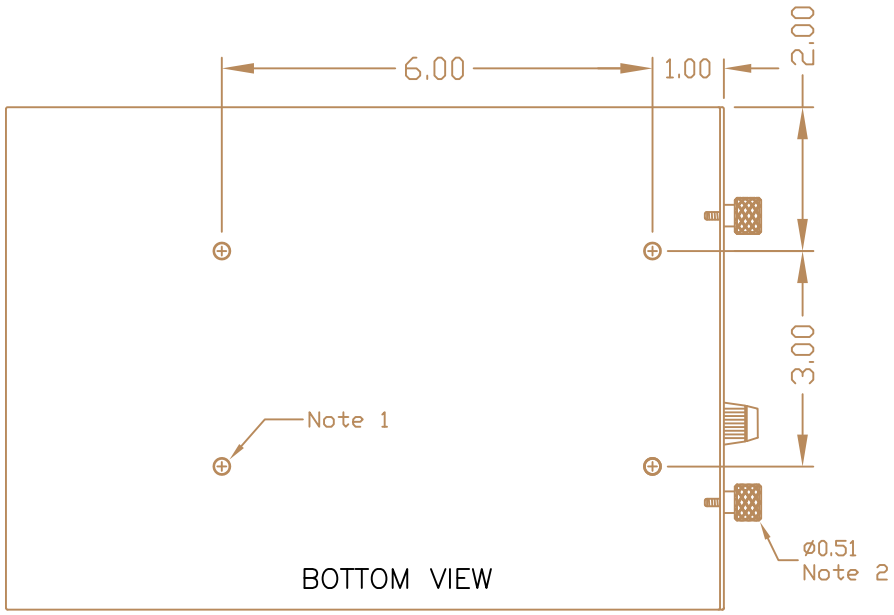
NOTE:

1. "U" shaped rod handle fabricated of 0.25±0.05 diameter, Aluminum stock, with 4.00±0.125 length, & rod center to center, shall be provided. The handle shall be vertically centered. The depth from the vertical centerline of the handle rod to the module from panel shall be 1.25±0.125.
2. The power supply module dimension, from front panel to connector plug, shall be 7.375 +0.000, −0.125.
3. A standard 8-32 metal stud retaining screw shall provide proper securing of the power supply when installed in the PDA using washers and a wingnut.
4. Connector BEAU P-5406 or equivalent.
5. Front panel shall be Aluminum stock or Stainless Steel.
6. All dimensions shown are in inches.

TITLE: MODEL 206E POWER SUPPLY	
	NO SCALE
TEES 2020	A3-13

MODEL 700 POWER SUPPLY MODULE

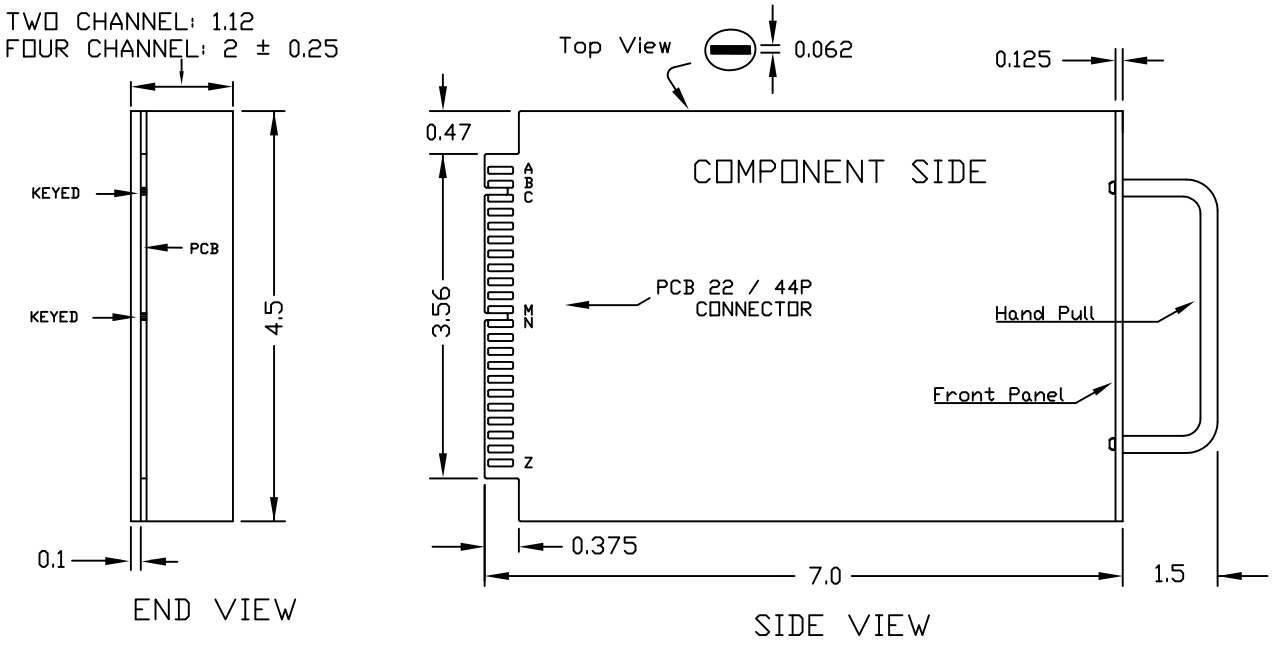


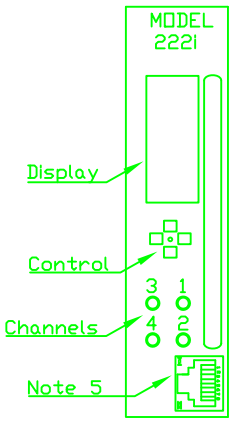


NOTE:
1. M4X0.7P Thread, 4X Mounting locations, bottom.
2. TSD: Southco #47-62-381-20.
3. 24VDC+ "RED", 24VDC- "BLACK".
4. All dimensions shown are in inches.

TITLE: MODEL 700 POWER SUPPLY	
	NO SCALE
TEES 2020	A3-14

APPENDIX A5
CHAPTER 5 DETAILS





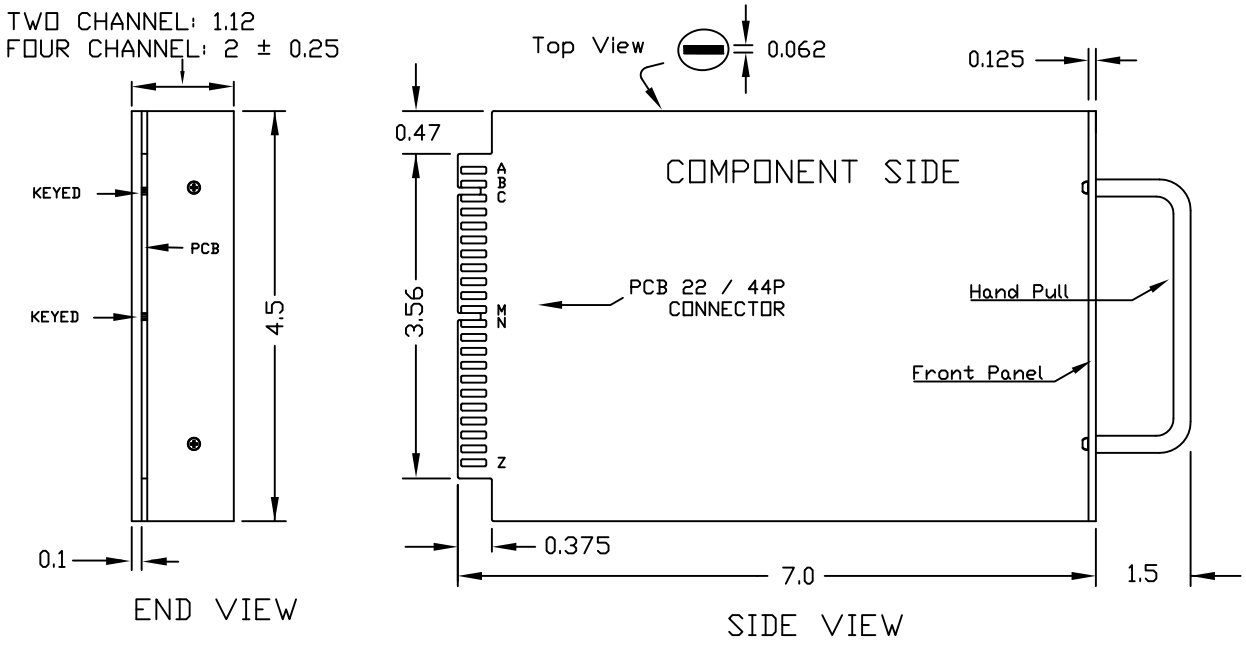
MODEL 222, 222i, 224, 224i & 232 CONNECTOR ASSIGNMENTS

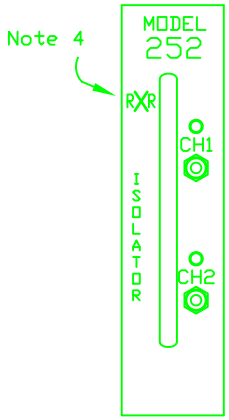
PIN	FUNCTION (SENSORS)
A	DC GROUND
B	+24 VDC
---	
*C	DETECTOR RESET
D	INPUT #1
E	INPUT #1
F	OUTPUT #1 (C)
H	OUTPUT #1 (E)
J	INPUT #2
K	INPUT #2
L	EQUIPMENT GROUND
M	NA

N	NA
P	INPUT #3
R	INPUT #3
S	OUTPUT #3 (C)
T	OUTPUT #3 (E)
U	INPUT #4
V	INPUT #4
W	OUTPUT #2 (C)
X	OUTPUT #2 (E)
Y	OUTPUT #4 (C)
Z	OUTPUT #4 (E)

NOTES:
1. Tolerance dimensions are ±0.02 in except as noted
2. Sheet definitions:
   ---= Slotted for keying
   (C) = Collector
   (E) = Emitter
   * = NA for Model 232.
3. i=Intelligent
4. "U" shape rod handle shall be fabricate of 0.18 in to 0.26 in diameter, Aluminum stock.
5. RJ45 Ethernet port
6. All detectors shall be of the scanning type.
7. Front panel shall be Aluminum stock or Stainless Steel.
8. All dimensions shown are in inches.

TITLE: DETECTOR SENSOR UNIT DETAILS	
	NO SCALE
TEES 2020	A5-1





MODEL 242L & 252 CONNECTOR ASSIGNMENTS

PIN	FUNCTION (ISOLATORS)
A	DC GROUND
B	+24 VDC

C	NA
D	INPUT #1
E	INPUT #1
F	OUTPUT #1 (C)
H	OUTPUT #1 (E)
J	INPUT #2
K	INPUT #2
L	EQUIPMENT GROUND
M	NA

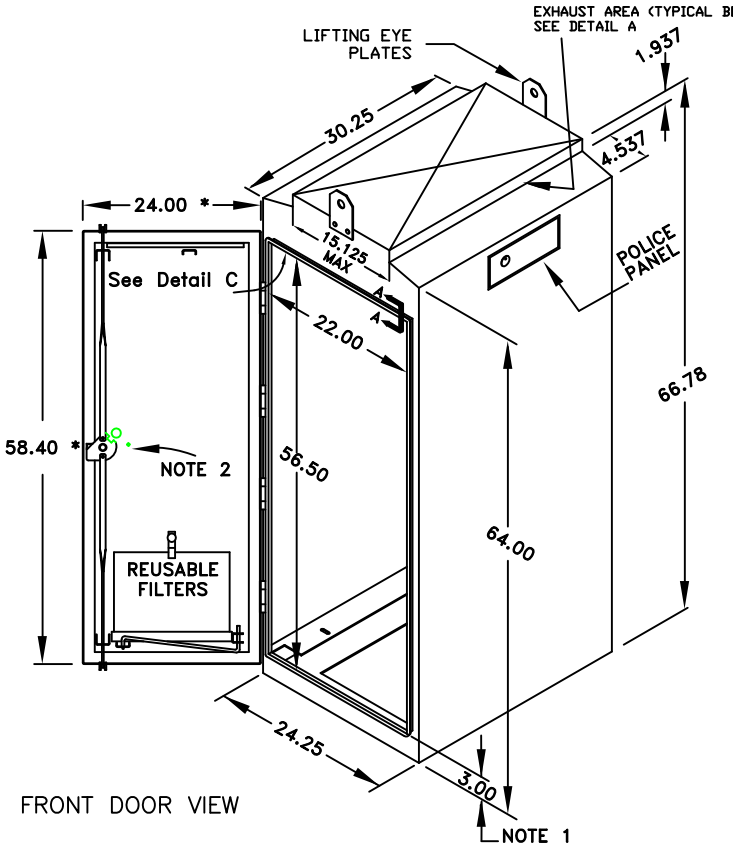
N	NA
P	NA
R	NA
S	NA
T	NA
U	NA
V	NA
W	OUTPUT #2 (C)
X	OUTPUT #2 (E)
Y	NA
Z	NA

NOTES:
1. Tolerance dimensions are ±0.02 in except as noted
2. Sheet definitions:
   ---= Slotted for keying
   (C) = Collector
   (E) = Emitter
3. "U" shape rod handle shall be fabricate of 0.18 in to 0.26 in diameter, Aluminum stock.
4. Label "RXR" on model 252.
5. Front panel shall be Aluminum stock or Stainless Steel.
6. All dimensions shown are in inches.

TITLE: DC AND AC ISOLATOR DETAILS	
	NO SCALE
TEES 2020	A5-2

APPENDIX A6
CHAPTER 6 DETAILS

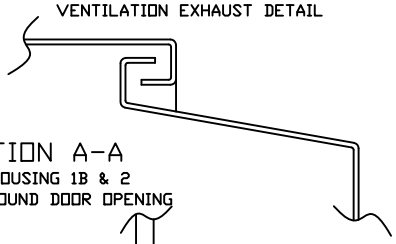
CABINET HOUSING 1B



FRONT DOOR VIEW

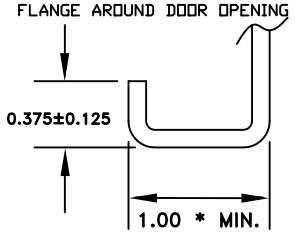
DETAIL A

CABINET HOUSING 1B & 2
VENTILATION EXHAUST DETAIL



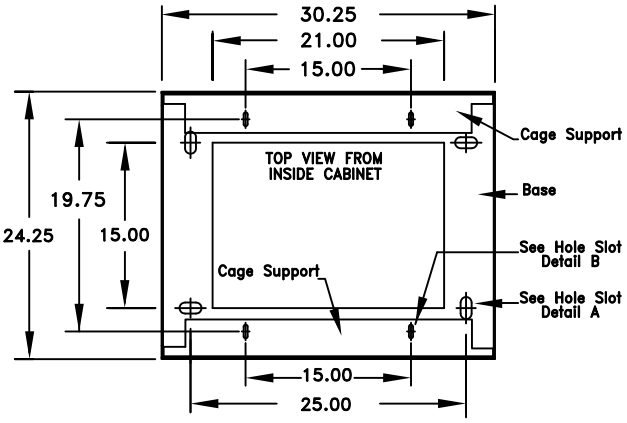
SECTION A-A

CABINET HOUSING 1B & 2
FLANGE AROUND DOOR OPENING

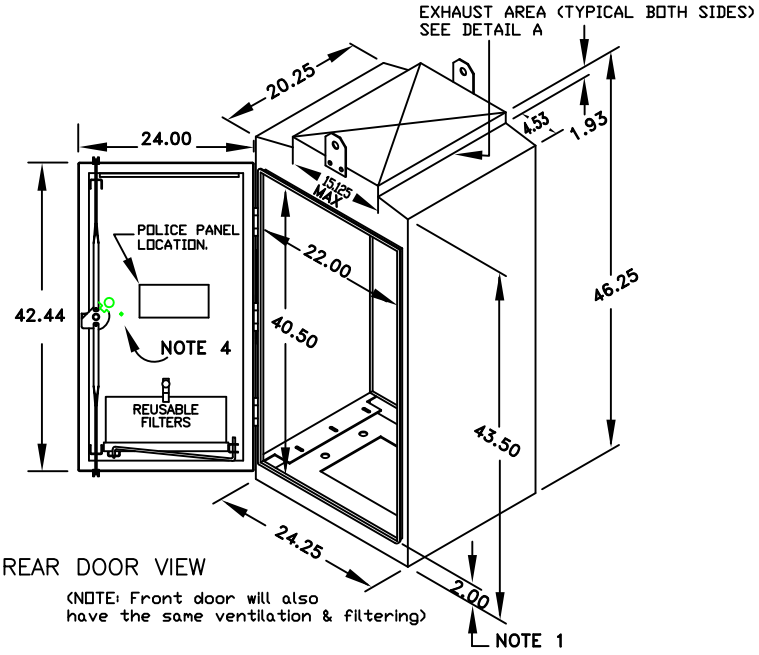


* TOLERANCE +0.0625, −0

CABINET HOUSING 1B BOTTOM DETAIL



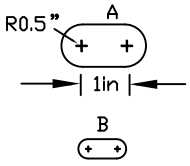
CABINET HOUSING 2



REAR DOOR VIEW

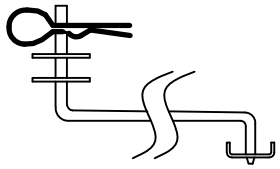
(NOTE: Front door will also have the same ventilation & filtering)

HOLE SLOT DETAIL

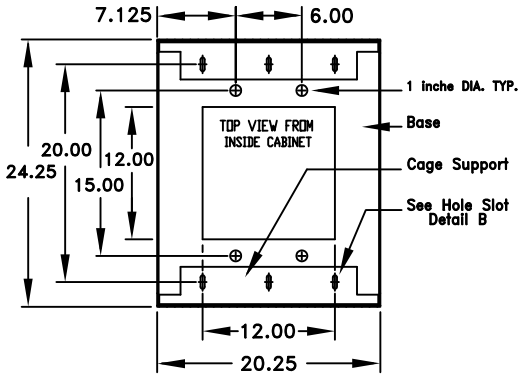


0.375"x1.25" OBROUND

DETAIL C



CABINET HOUSING 2 BOTTOM DETAIL



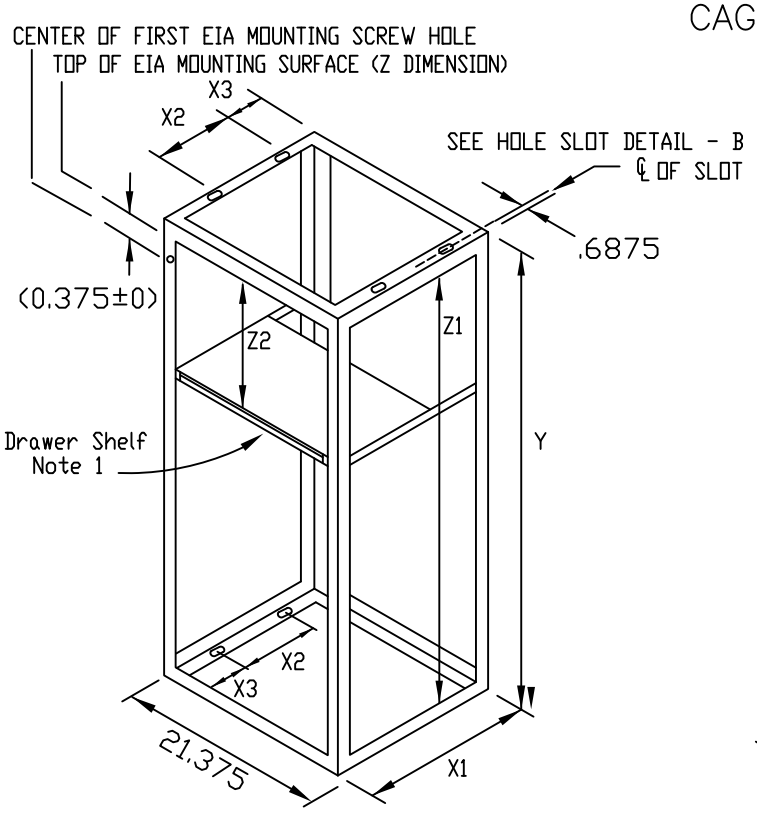
NOTE: ALL HOLE PATTERNS CENTERED ON CABINET BOTTOMS.

NOTE:

1. Cabinet base to door openning.
2. The locks & handles shall be on right side of the front door & the left side of the rear door (viewed externally)
3. All dimensions shown are in inches.
4. The locks & handles shall be on left side of the front door & the right side of the rear door (viewed externally)
5. The handles shall be placed centered vertically on the doors.
6. Upper and lower catches must hold the door open at multiple positions

TITLE: CABINET HOUSING #1 & #2 DETAILS SHEET 1 OF 4	
	NO SCALE
TEES 2020	A6-1

CAGE SUPPORT DETAIL

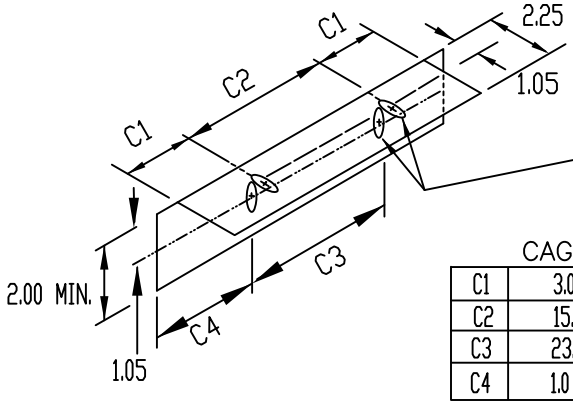


FRONT VIEW

CABINET
CAGE DIMENSIONS

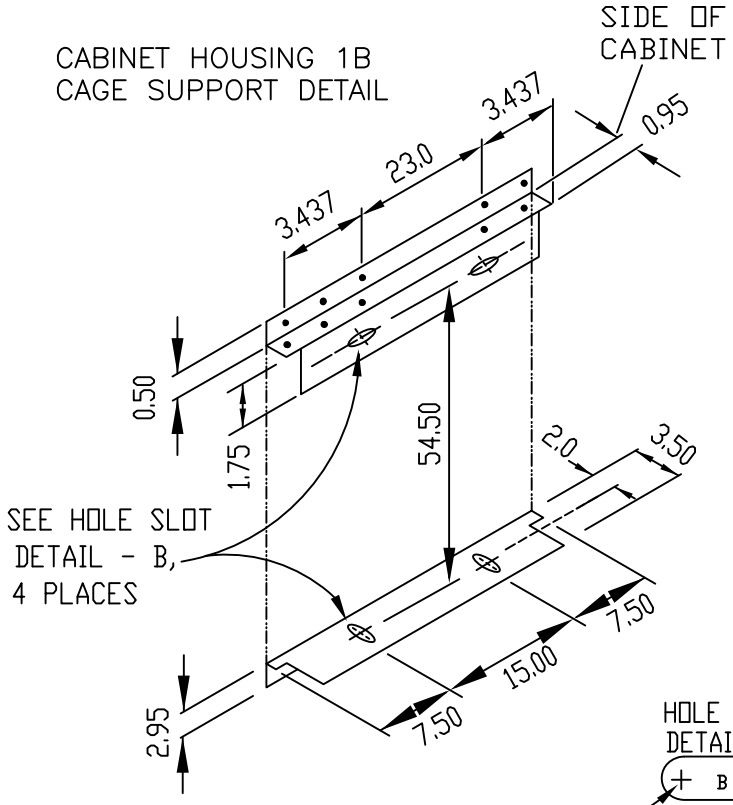
	CAGE #1	CAGE #2
X1	21.375	16.00
X2	15.00	12.00
X3	3.188	2.00
Y	55.50	40.00
Z1	53.00 MIN.	38.75 MIN.
Z2	15.75	7.25

SPACER BRACKET DETAIL

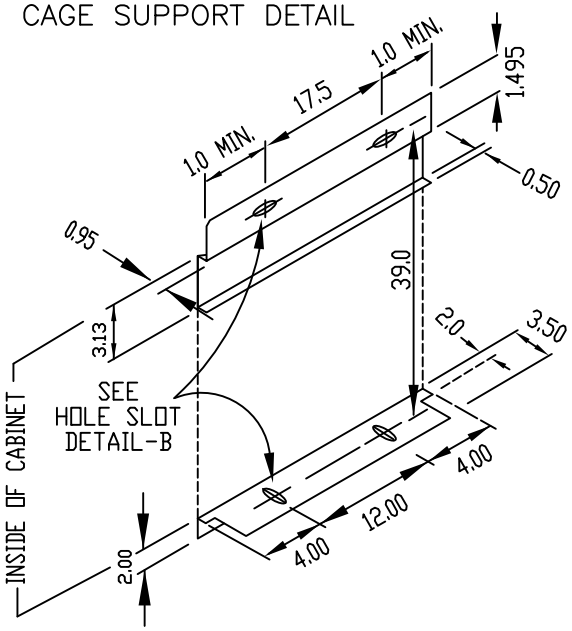


	CAGE #1	CAGE #2
C1	3.0 MIN.	3.0 MIN.
C2	15.0	12.0
C3	23.0	17.5
C4	1.0 MIN.	1.0 MIN.

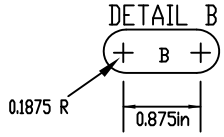
CABINET HOUSING 1B
CAGE SUPPORT DETAIL



CABINET HOUSING 2
CAGE SUPPORT DETAIL



HOLE SLOT
DETAIL B



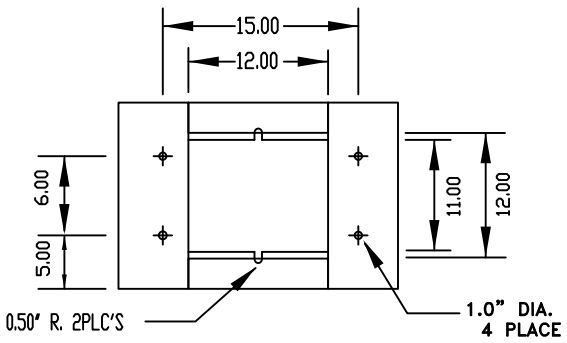
NOTE:

1. Drawer Shelf details, A6–6
2. All dimensions shown are in inches

TITLE: CABINET HOUSING #1 & #2 DETAILS
SHEET 2 OF 4

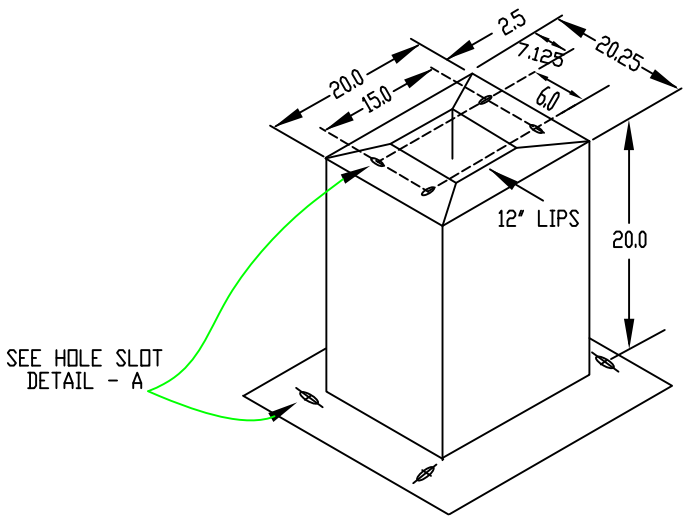
	NO SCALE
TEES 2020	A6-2

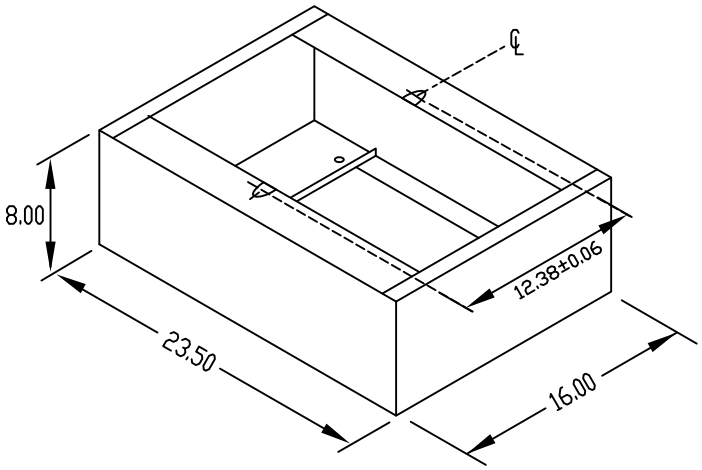
CABINET HOUSING 2
"M" BASE ADAPTOR DETAIL



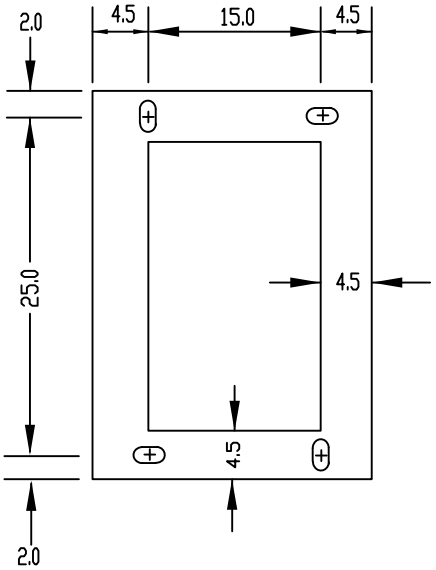
TOP VIEW

TYPE 332/336 ADAPTOR

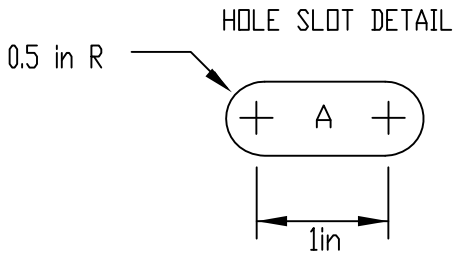




BOTTOM VIEW



332 BASE VIEW



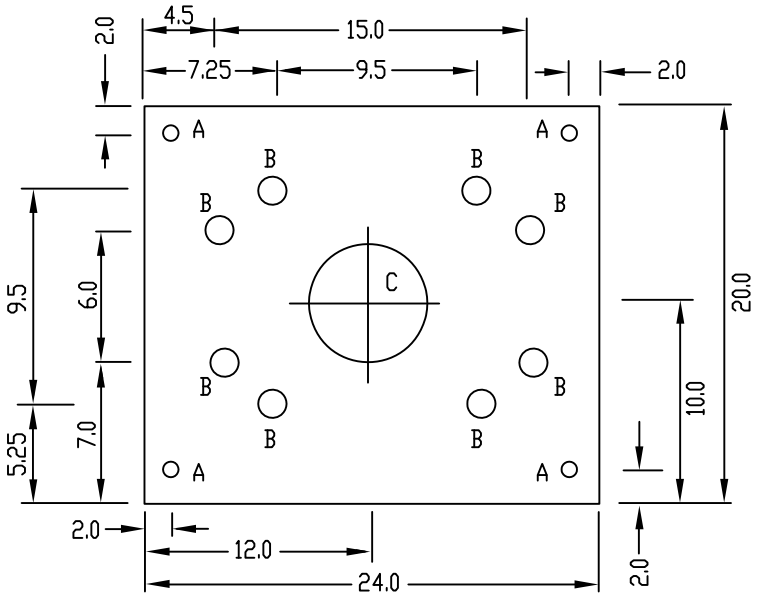
DETAIL A

NOTE:

All dimensions shown are in inches.

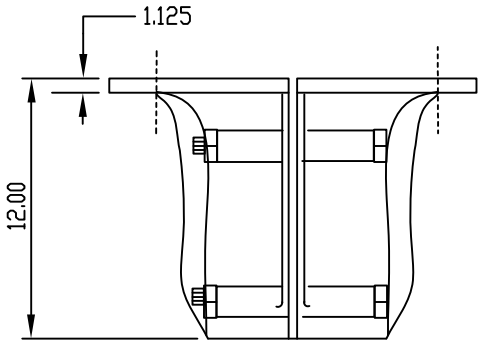
TITLE: CABINET HOUSING DETAILS SHEET 3 OF 4	
	NO SCALE
TEES 2020	A6-3

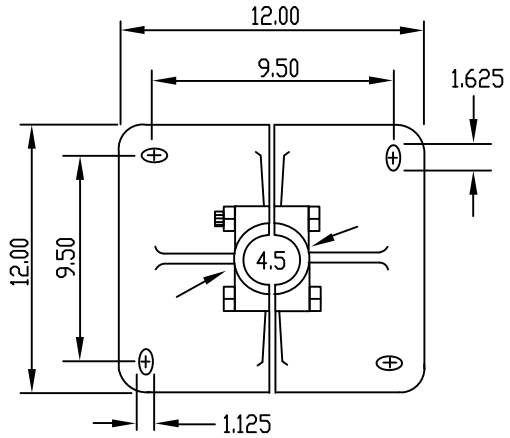
CABINET HOUSING 2 PEDESTAL ADAPTOR



SLIPFITTER BASE PLATE DETAIL
(0.375 inches ALUMINUM)

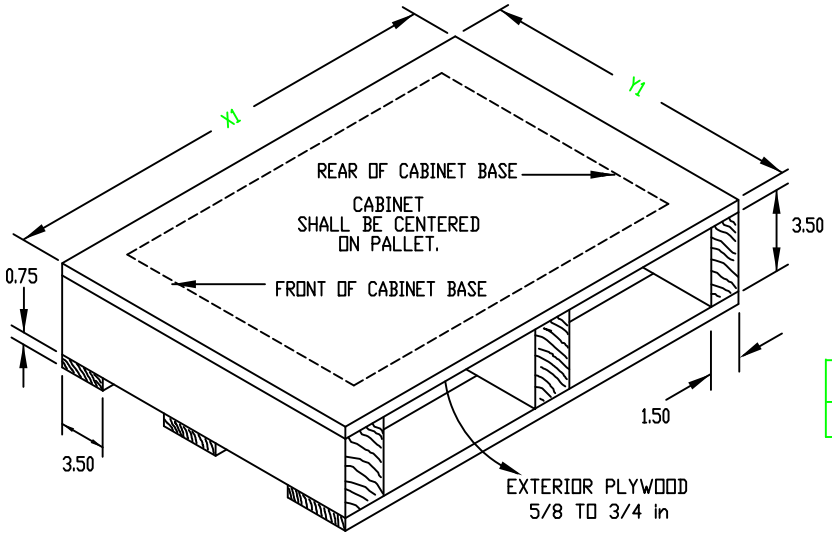
A = 0.50 in DIA.
B = 1 in DIA.
C = 5 in DIA.





SLIPFITTER (CAST ALUMINUM)
DETAIL

CABINET PALLET

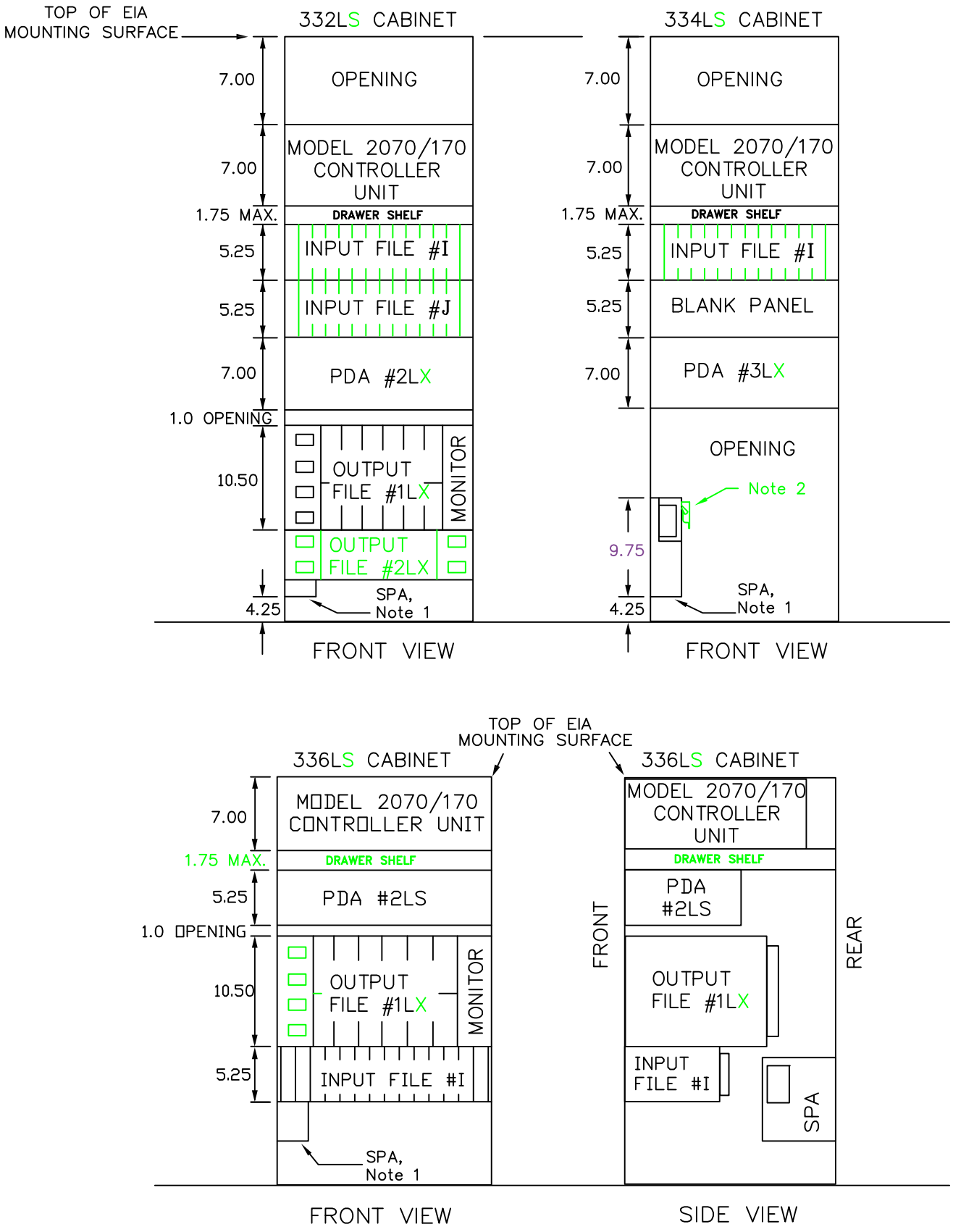


	HOUSING #1, #2	HOUSING #3, #4
X1	40	47
Y1	29	36

NOTE: (FOR DETAILS A6–1 to A6–4)

1. Housing 1B used in cabinets 332LS & 334LS and Housing 2 in cabinet 336LS.
   Housing 3 used in cabinets 342LX & 344LX and Housing 4 in cabinet 346LX.
2. Adaptors delivered separately shall be delivered centered and bolted on a plyboard shipping pallet.
3. Dashed lines on cabinet cage support detail delineates the cabinet side wall.
4. The bottom cabinet cage supports shall be continuously welded along the sides of the cabinet & extended to the inside corner of door openings.
   The top cabinet cage supports shall be continuously welded along the sides of the cabinet.
5. Cage support hole slots dimension shall be common for top & bottom.
6. All dimensions shown are in inches.

TITLE: CABINET HOUSING DETAILS SHEET 4 OF 4	
	NO SCALE
TEES 2020	A6–4



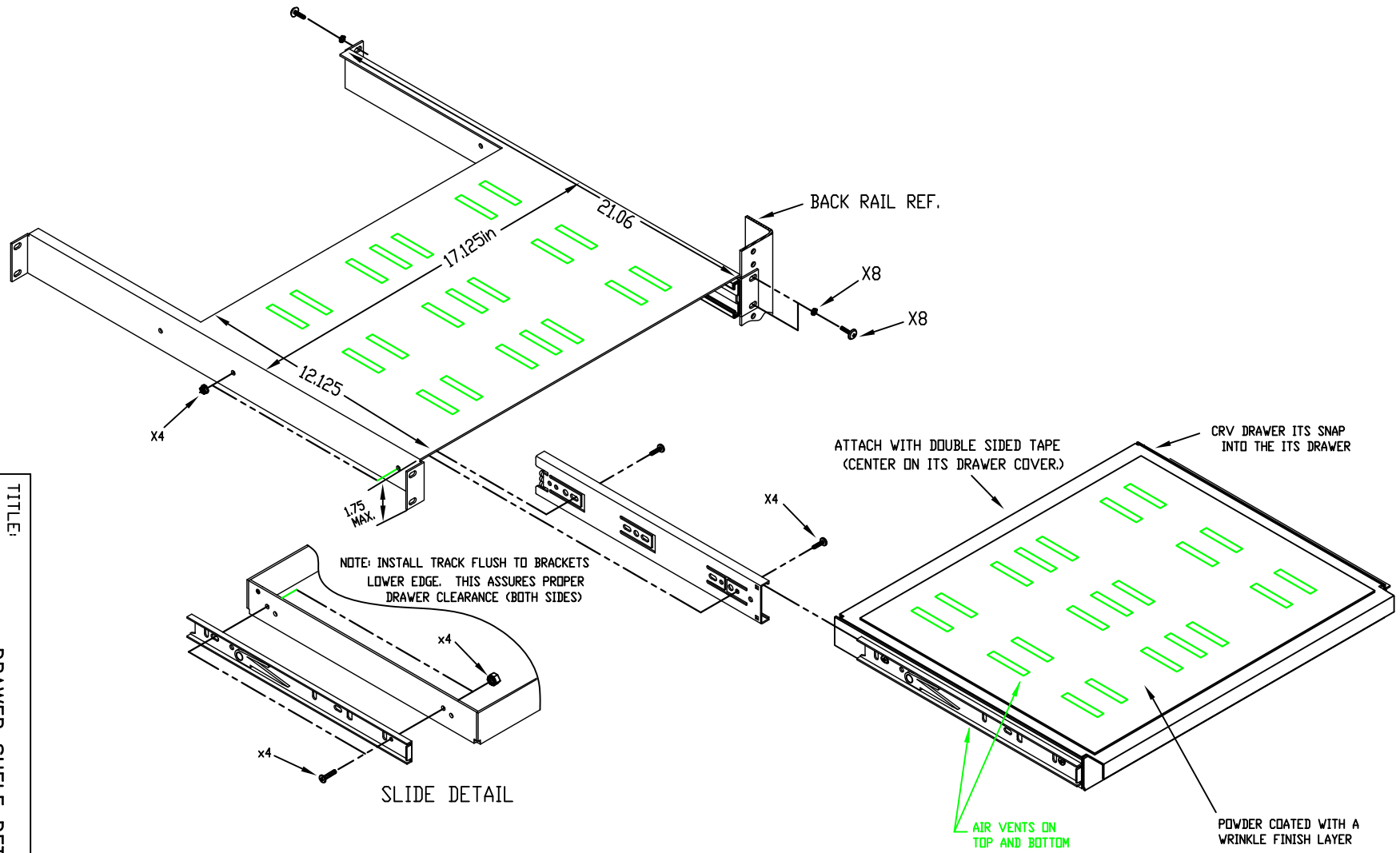
NOTE:

1. SPA shall be bolted on the rail and firmly attached to the Service Panel.
2. For Switch Guard details, see A6-60.
3. All dimensions shown are in inches.

TITLE: CABINET EQUIPMENT MOUNTING DETAILS SHEET 1 OF 3	
	NO SCALE
TEES 2020	A6-5

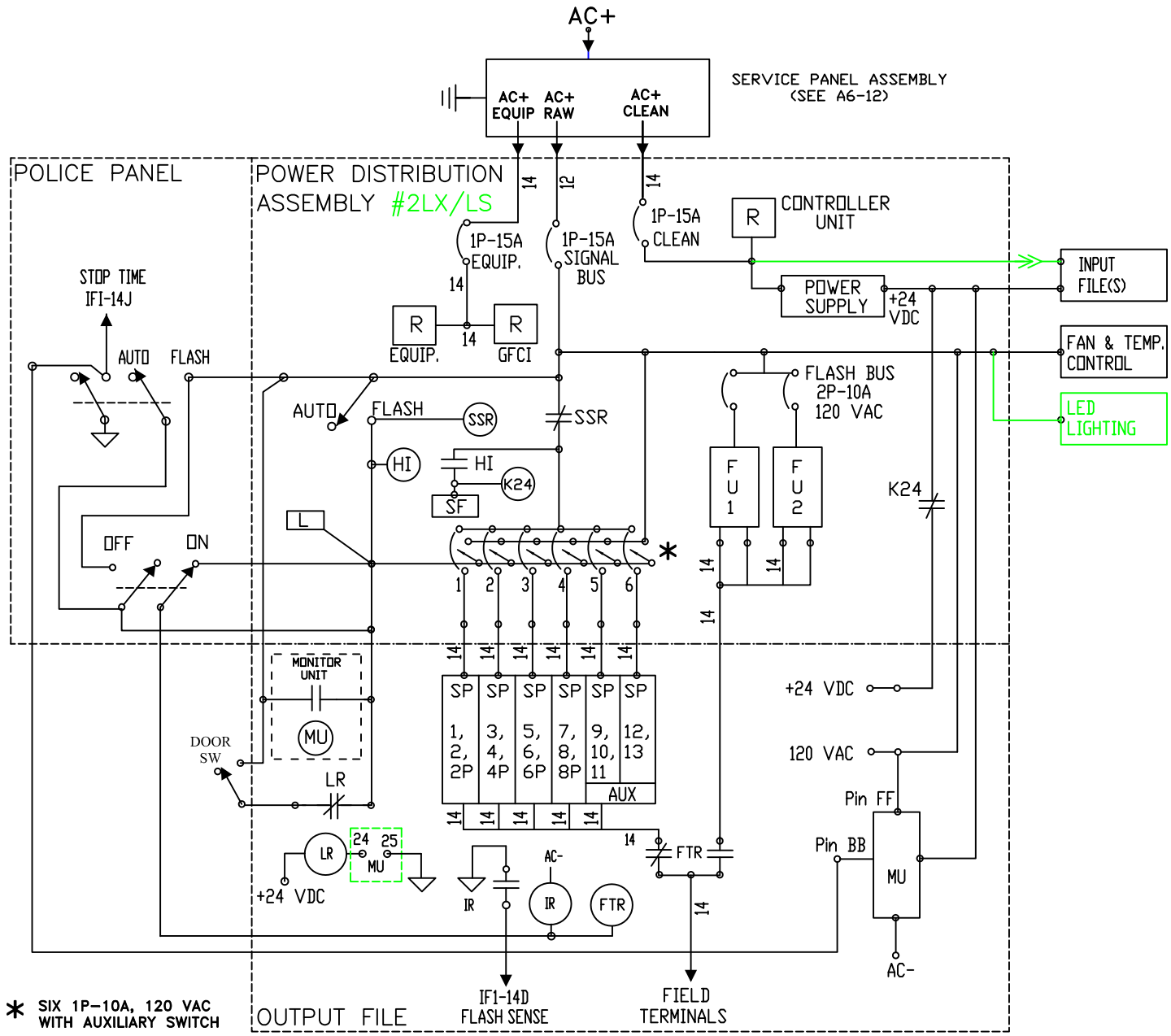
DRAWER SHELF UNIT

NOTE:
All dimensions shown are in inches



TITLE:		
DRAWER SHELF DETAILS	NO SCALE	TEES 2020
		A6-6

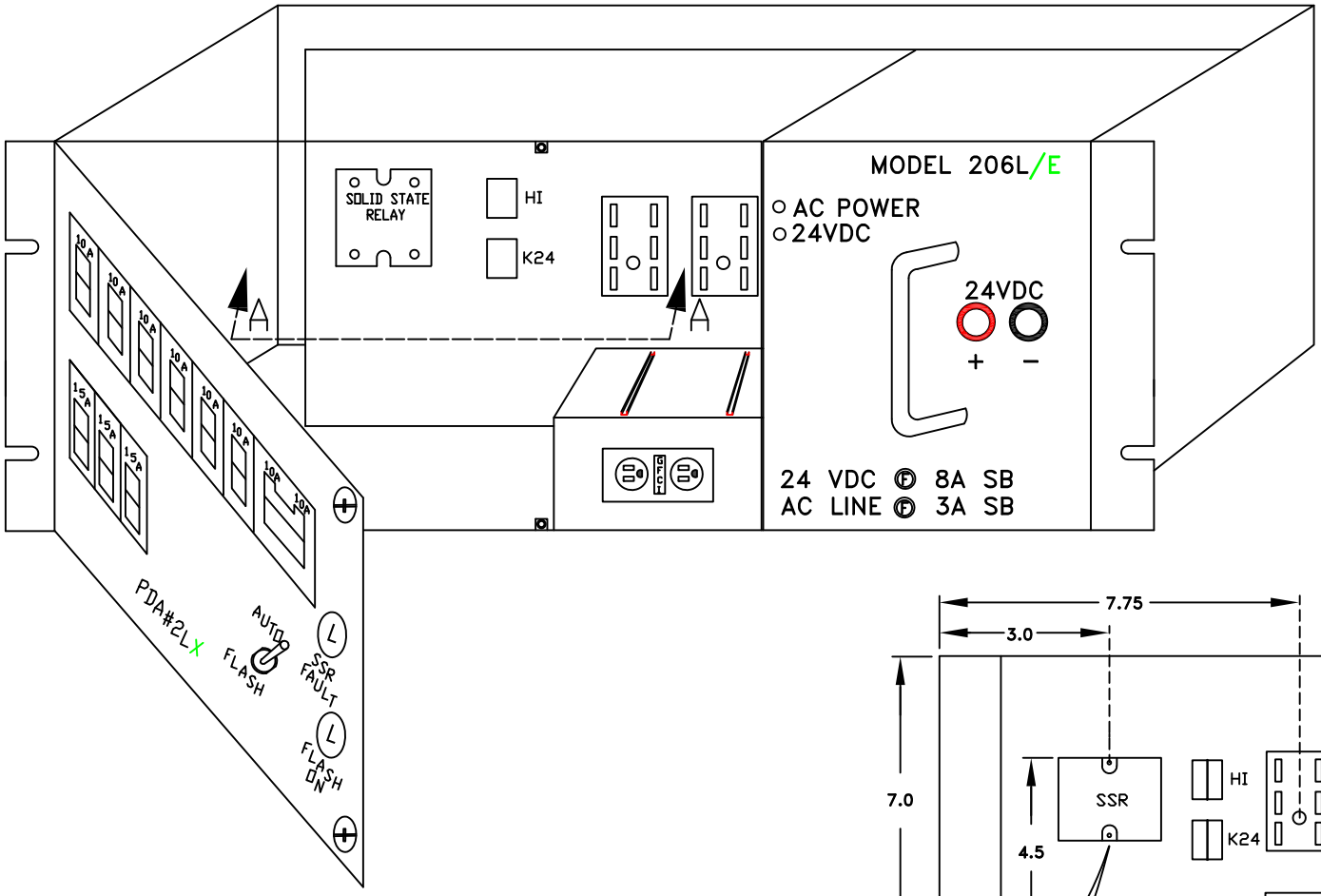
TRAFFIC SIGNAL CABINETS
ONE LINE DIAGRAM

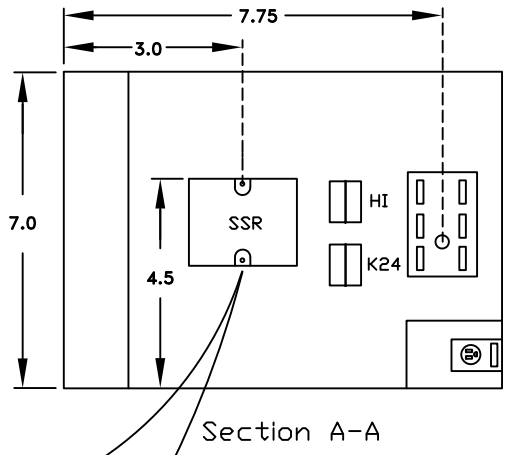


SHEET DEFINITIONS

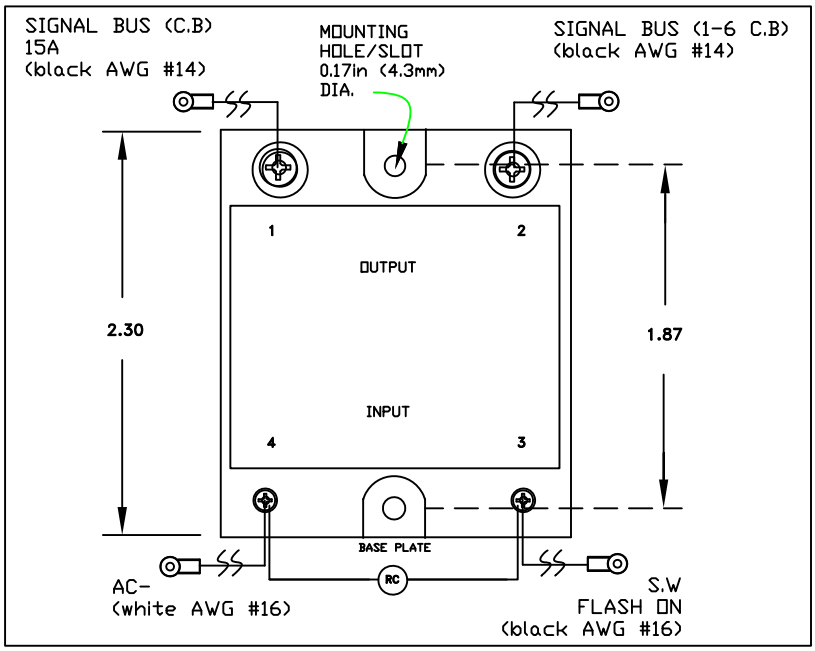
TBS	TERMINAL BLOCK - SERVICE	(*)	RELAY COIL - * RELAY NAME	TR	TRANSFER RELAY
	EQUIPMENT GROUND	FU1	FLASHER UNIT ONE	IR	ISOLATION RELAY
8	WIRE SIZE, IF NOT INDICATED SHALL BE #16 AWG OR LARGER		DC GROUND	GFCI	GROUND FAULT CIRCUIT INTERRUPTER
		WDT	WATCHDOG TIMER	LR	LOGIC RELAY
	CIRCUIT BREAKER	FTR	FLASH TRANSFER RELAY	CB-1	SIGNAL CIRCUIT BREAKER 1 (SECONDARY)
R	DUPLEX RECEPTACLE	L	PDA FLASH ON DISPLAY LAMP	IFI-14J	INPUT FILE I, TERMINAL BLOCK 14, POSITION J (CHANNEL 2 INPUT)
	SWITCH CONTACT	SPA	SERVICE PANEL ASSEMBLY	IF1-14D	INPUT FILE I, TERMINAL BLOCK 14, POSITION D
	RELAY CONTACT, NORMALLY CLOSED	MU	MONITOR UNIT	C1-65	C1 CONNECTOR, PIN 65
	RELAY CONTACT, NORMALLY OPEN	SF	SSR Fault Indicator	TRAFFIC SIGNAL CABINETS 332LS, 336LS, 342LX, 346LX	
SSR	SOLID STATE RELAY	T2-6	TERMINAL BLOCK 2, POSITION 6		
PDA	POWER DISTRIBUTION ASSEMBLY	HSR1	HEALTH STATUS RELAY 1		
AUX	AUXILIARY	HI	HEALTH INDICATOR RELAY		
SP	SWITCH PACK	K24	DISCONNECT 24VDC RELAY		
	PLUG SOCKET CONNECTION				

TITLE:	TRAFFIC SIGNAL CABINETS ONE LINE DIAGRAM
	NO SCALE
TEES 2020	A6-7





Section A-A

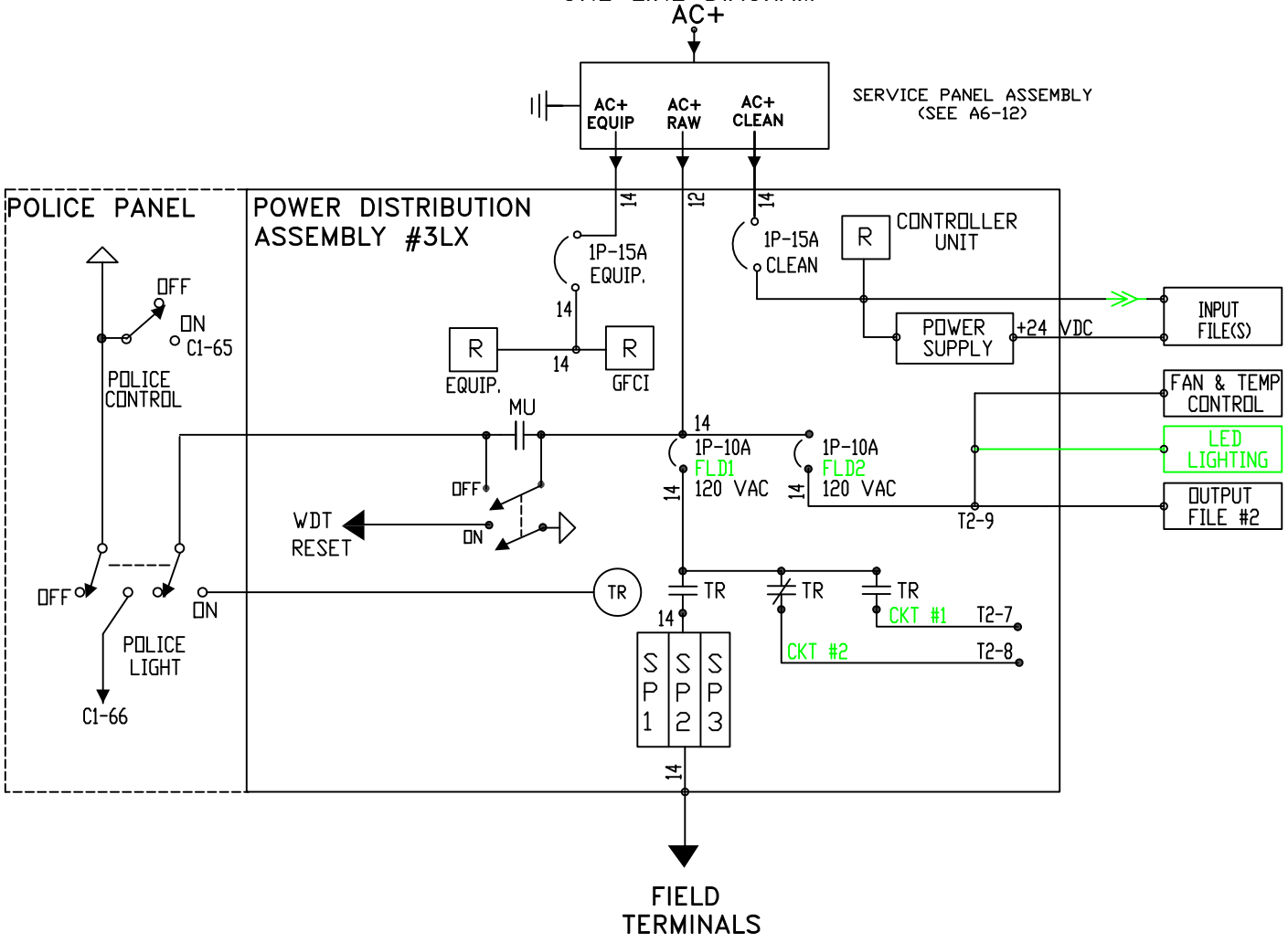


NOTE:

All dimensions shown are in inches.

TITLE: PDA #2LX SSR INSTALLATION DETAILS	
	NO SCALE
TEES 2020	A6-8

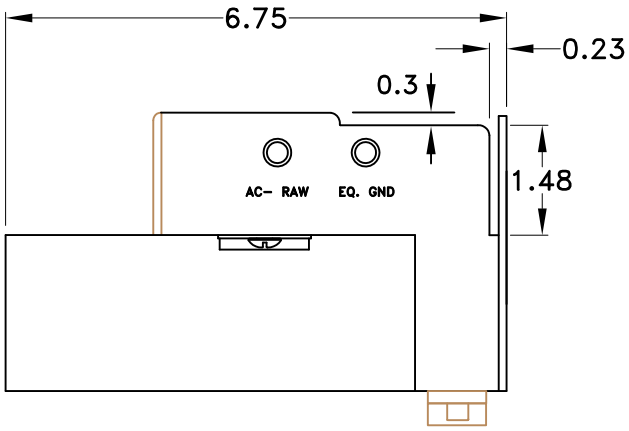
RAMP METER CABINETS
ONE LINE DIAGRAM



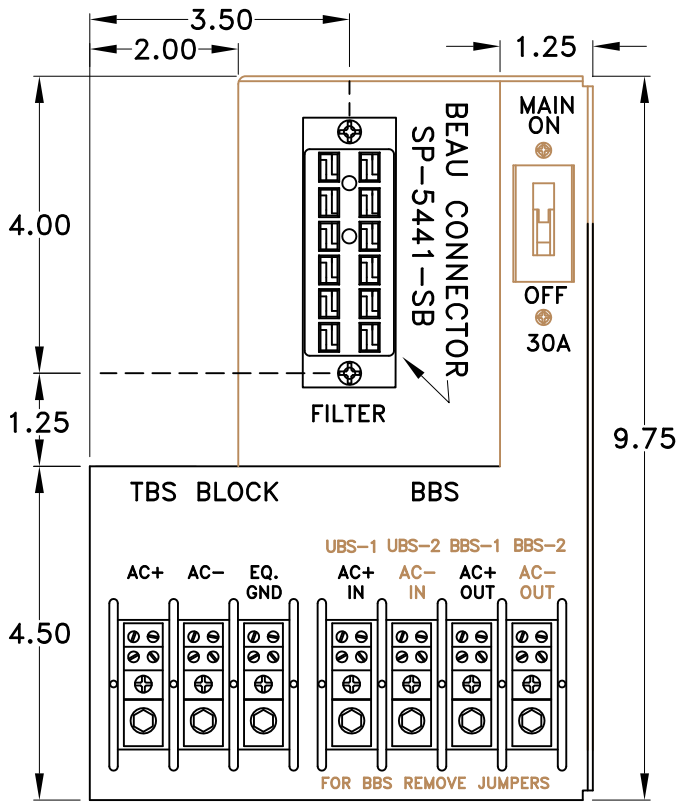
SHEET DEFINITIONS

TBS	TERMINAL BLOCK - SERVICE	WDT	WATCHDOG TIMER
⏚	EQUIPMENT GROUND	MU	MONITOR UNIT
⌒	CIRCUIT BREAKER	CB-1	SIGNAL CIRCUIT BREAKER 1 (SECONDARY)
R	DUPLEX RECEPTACLE	TR	TRANSFER RELAY
GFCI	GROUND FAULT CIRCUIT INTERRUPTER	T2-6	TERMINAL BLOCK 2, POSITION 6
⫽	RELAY CONTACT, NORMALLY CLOSED	C1-65	C1 CONNECTOR, PIN 65
⫠	RELAY CONTACT, NORMALLY OPEN	SPA	SERVICE PANEL ASSEMBLY
⊟	FLASHER UNIT ONE	SP	SWITCH PACK
PDA	POWER DISTRIBUTION ASSEMBLY	▽	DC GROUND
FLD2	FIELD CIRCUIT BREAKER	8	WIRE SIZE, IF NOT INDICATED SHALL BE #16 AWG OR LARGER
≫	PLUG SOCKET CONNECTION	IFI-14J	INPUT FILE I, TERM. BLOCK 14, POSITION J (CHANNEL 2 INPUT)
⌒	SWITCH CONTACT	RAMP METER CABINETS 334LS, 344LX	

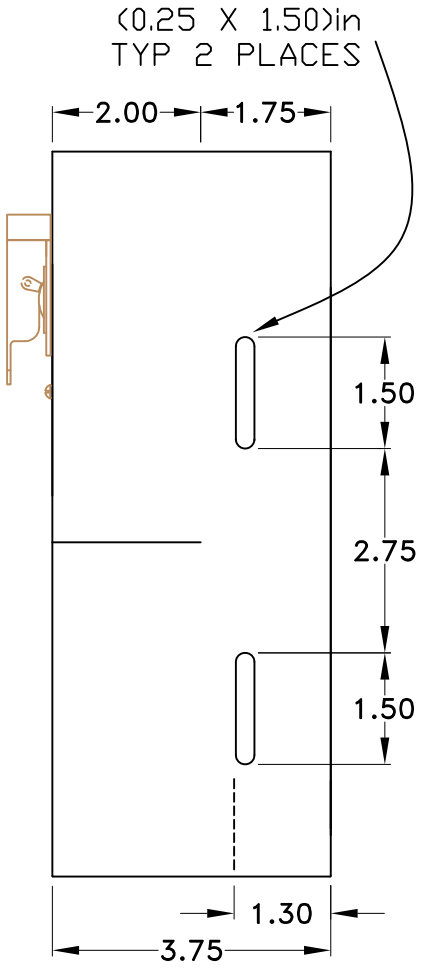
TITLE: RAMP METER CABINETS ONE LINE DIAGRAM	
	NO SCALE
TEES 2020	A6-09



TOP VIEW



FRONT VIEW

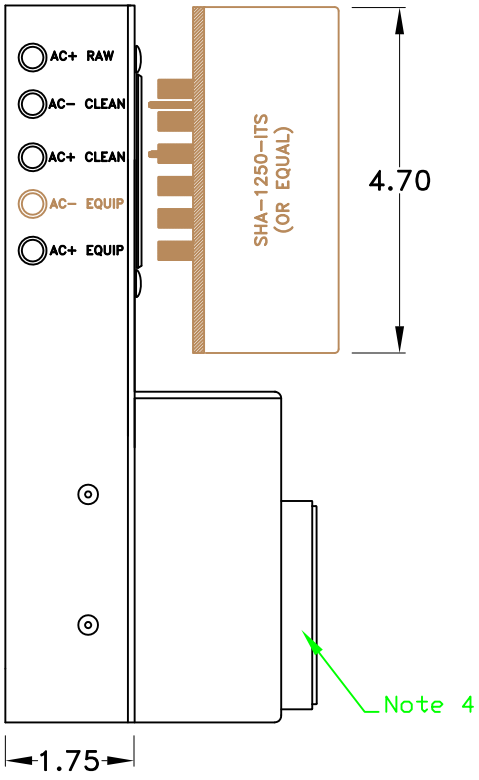


SIDE VIEW

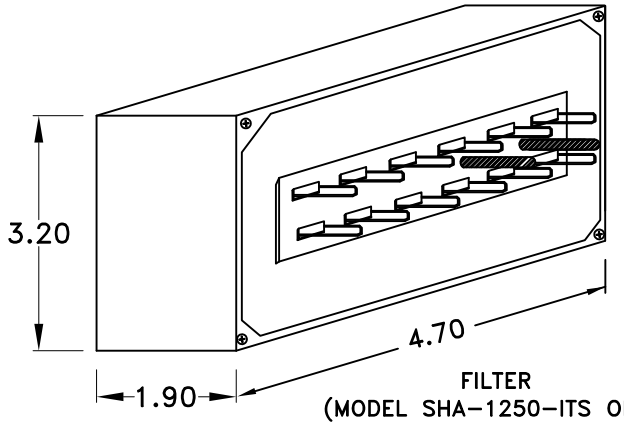
NOTE:

All dimensions shown are in inches.

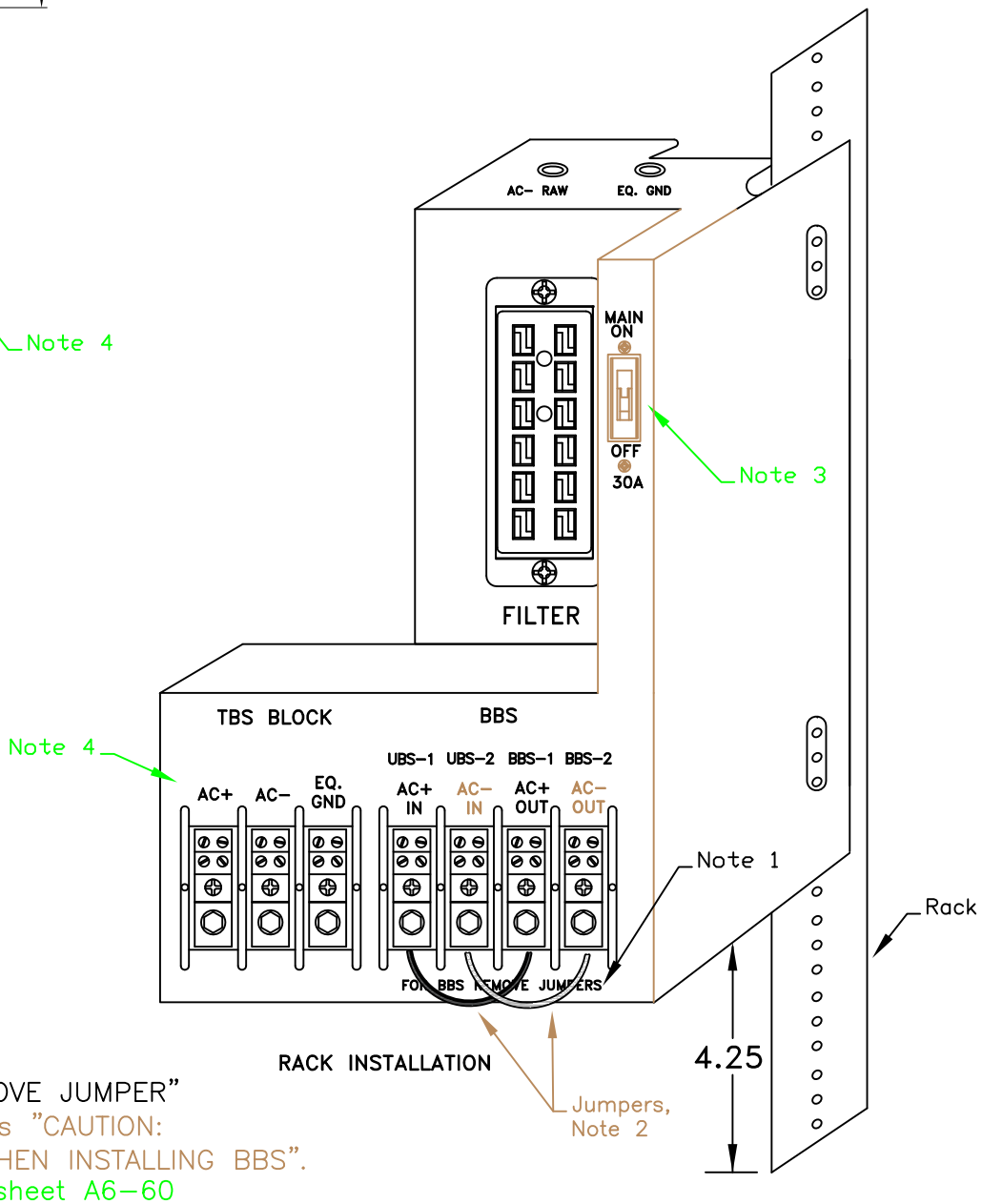
TITLE: SERVICE PANEL ASSEMBLY (SPA) DETAILS SHEET 1 OF 3	
	NO SCALE
TEES 2020	A6-10



SIDE VIEW



FILTER
(MODEL SHA-1250-ITS OR EQUAL)

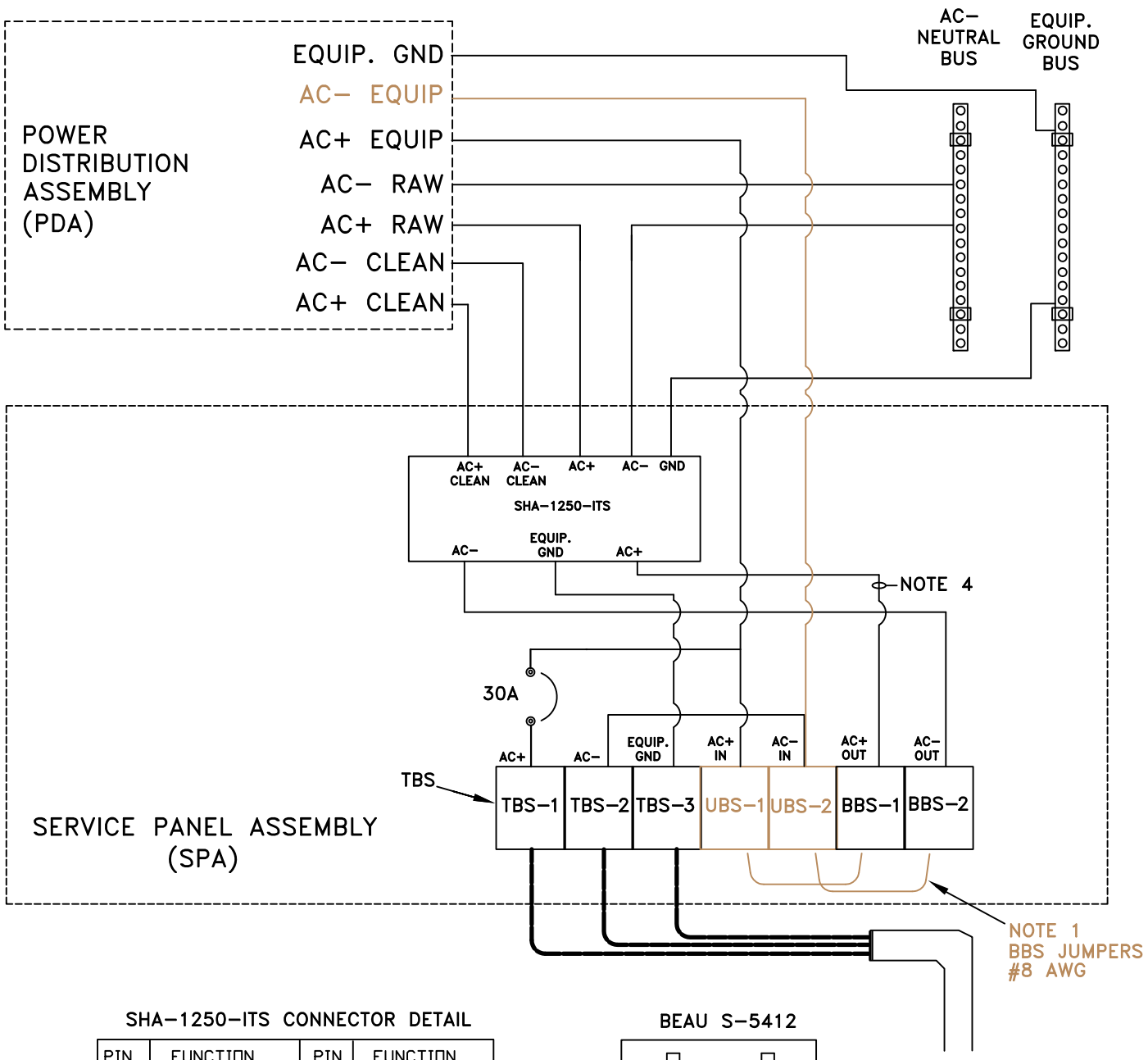


RACK INSTALLATION

NOTES: (FOR THIS DETAIL)

1. Place label "FOR BBS REMOVE JUMPER"
2. Attach red tags on jumpers "CAUTION: REMOVE THESE JUMPERS WHEN INSTALLING BBS".
3. See Switch Guard details, sheet A6-60
4. Clear plastic cover shall protect the terminal blocks.
5. The SPA shall be mounted at least 4.25in above the bottom of the cabinet shelf, except the 336LS.
6. All dimensions shown are in inches.

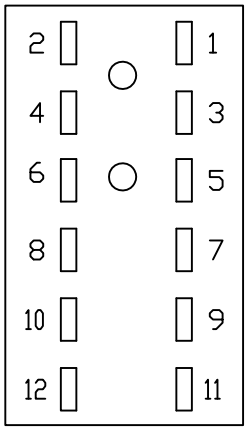
TITLE: SERVICE PANEL ASSEMBLY (SPA) DETAILS SHEET 2 OF 3	
	NO SCALE
TEES 2020	A6-11



SHA–1250–ITS CONNECTOR DETAIL

PIN	FUNCTION	PIN	FUNCTION
1	AC+ RAW	2	AC+ RAW
3	EQ. GND	4	EQ. GND
5	AC+ CLEAN	6	AC+ RAW
7	AC– CLEAN	8	NA
9	EQ. GND	10	EQ. GND
11	AC– RAW	12	AC– RAW

BEAU S–5412



REAR VIEW

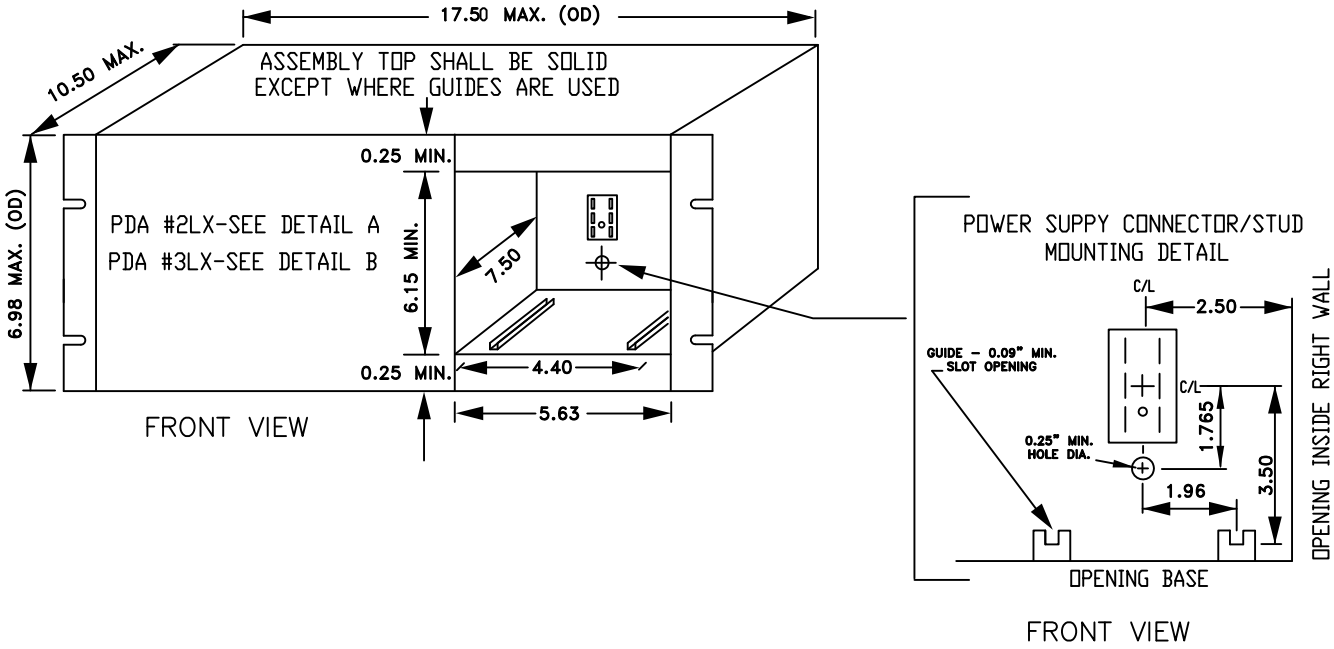
NOTE:

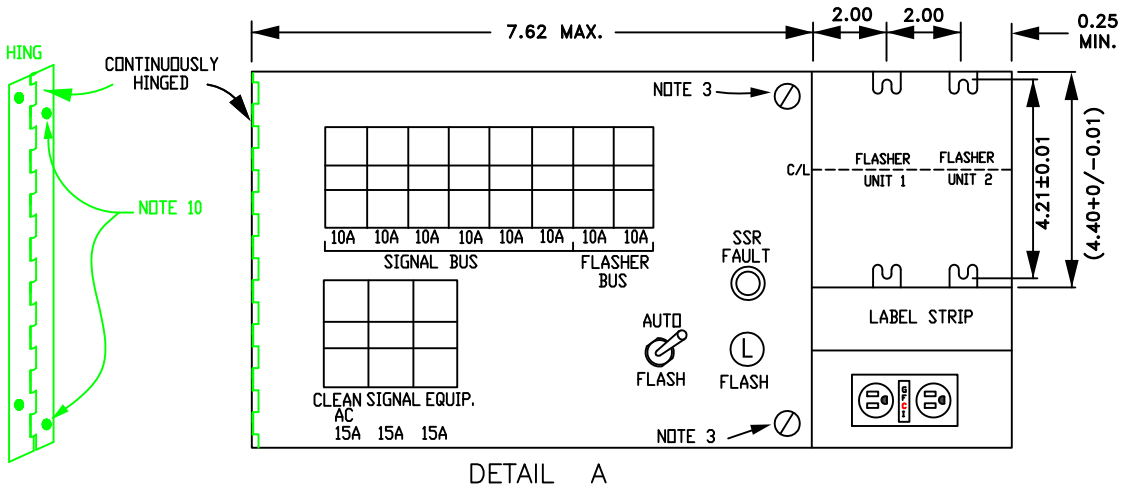
BBS = Battery Back–up System
TBS = Terminal Block Service
UBS = Utility to BBS

1. Remove jumper when connecting BBS.
2. SHA–1250–ITS connector BEAU S–5412 or equivalent.
3. Surge protection shall be provided of indicators
   GREEN LED Indicator ON= ok, OFF= error.
   YELLOW LED ON= error, Off= ok.
4. Red insulation conductor

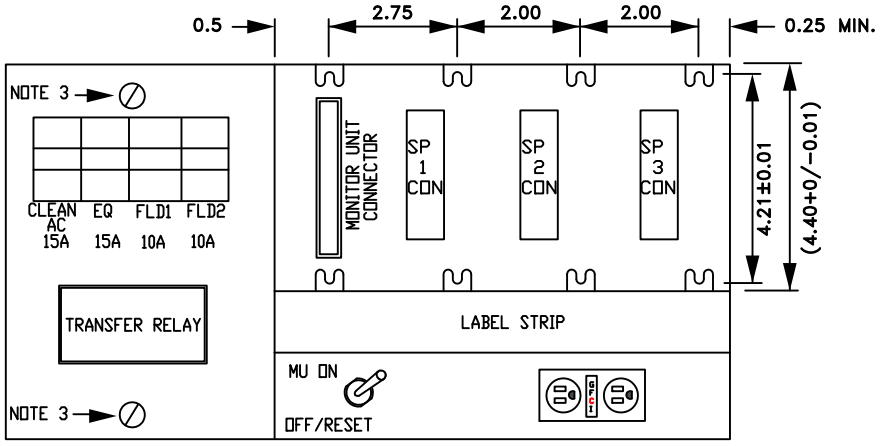
TITLE:
SERVICE PANEL ASSEMBLY (SPA) DETAILS
SHEET 3 OF 3

	NO SCALE
TEES 2020	A6–12





DETAIL A

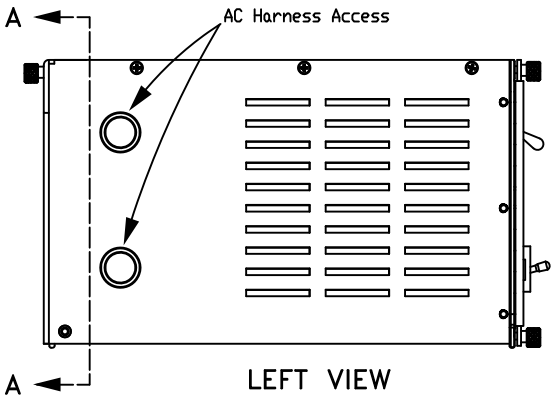


DETAIL B

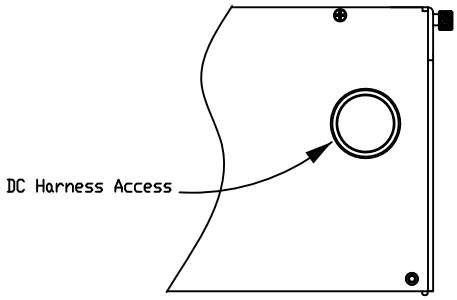
NOTE:

1. See A6-17 for notes.
2. All dimensions shown are in inches.

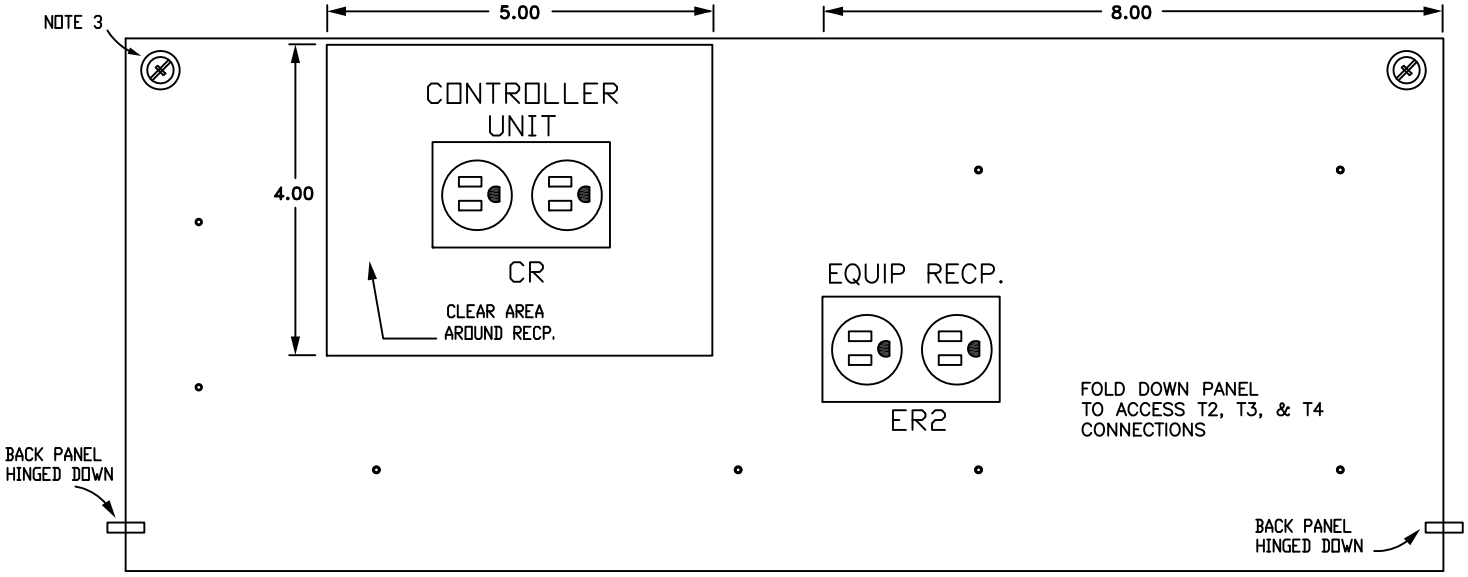
TITLE: PDA #2LX & #3LX DETAILS SHEET 1 OF 8	
	NO SCALE
TEES 2020	A6-13



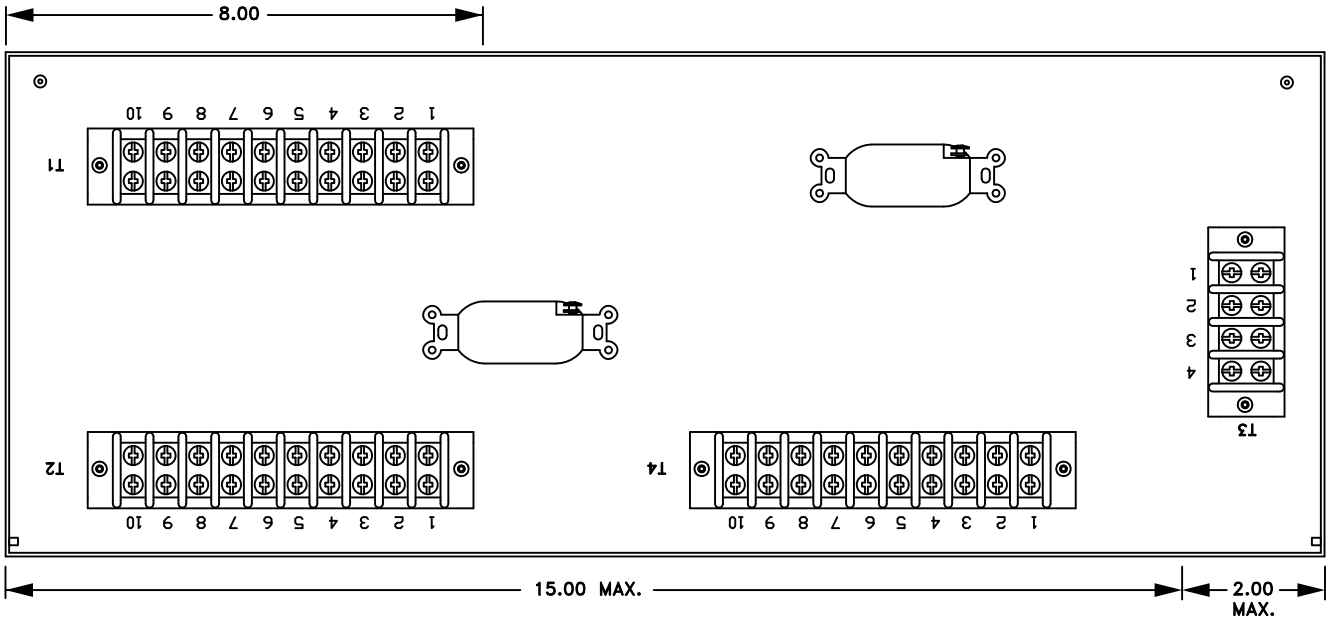
LEFT VIEW



RIGHT VIEW



PDA #2LX REAR VIEW

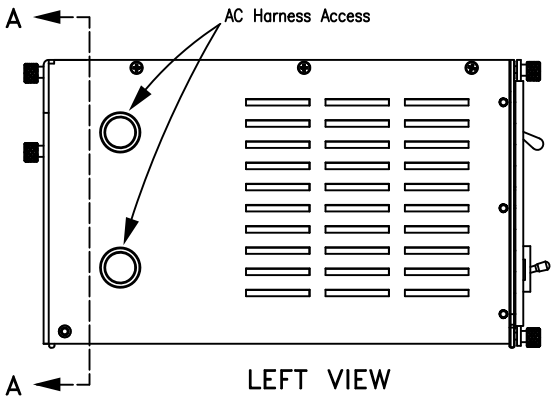


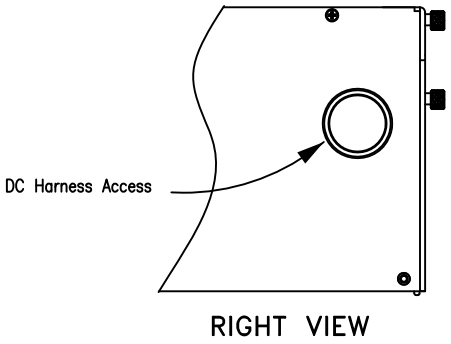
VIEW A–A
(INSIDE REAR PANEL)

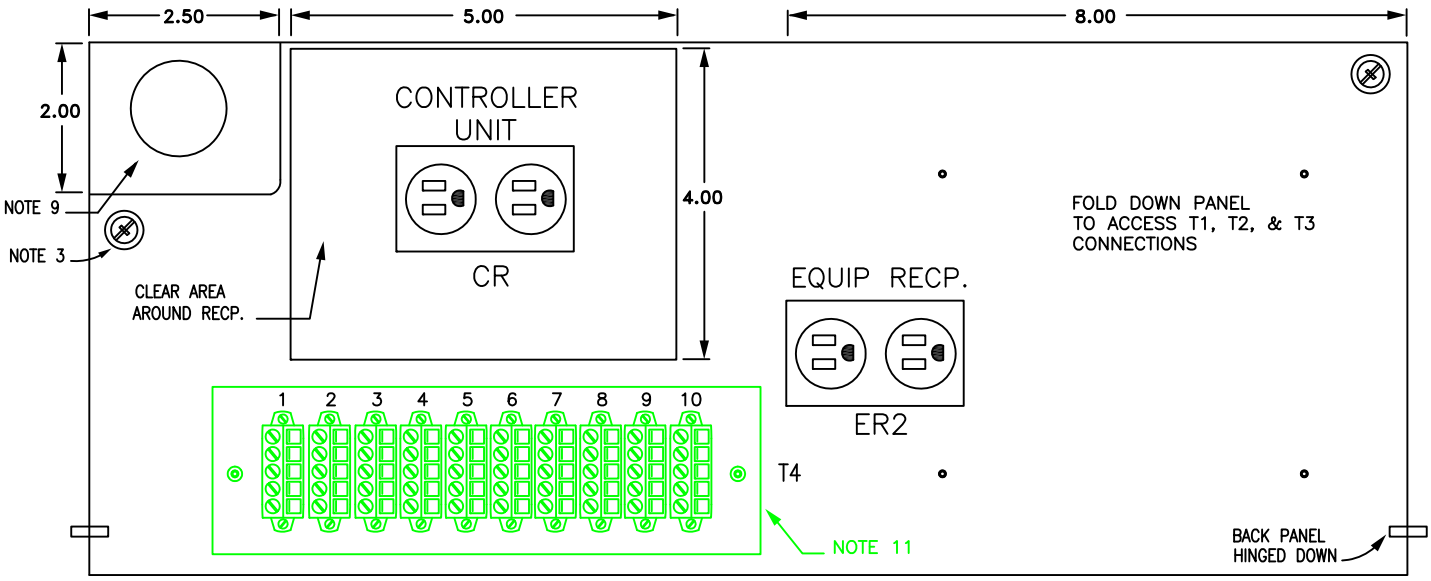
NOTE:

1. See A6-17 for notes.
2. All dimensions shown are in inches.

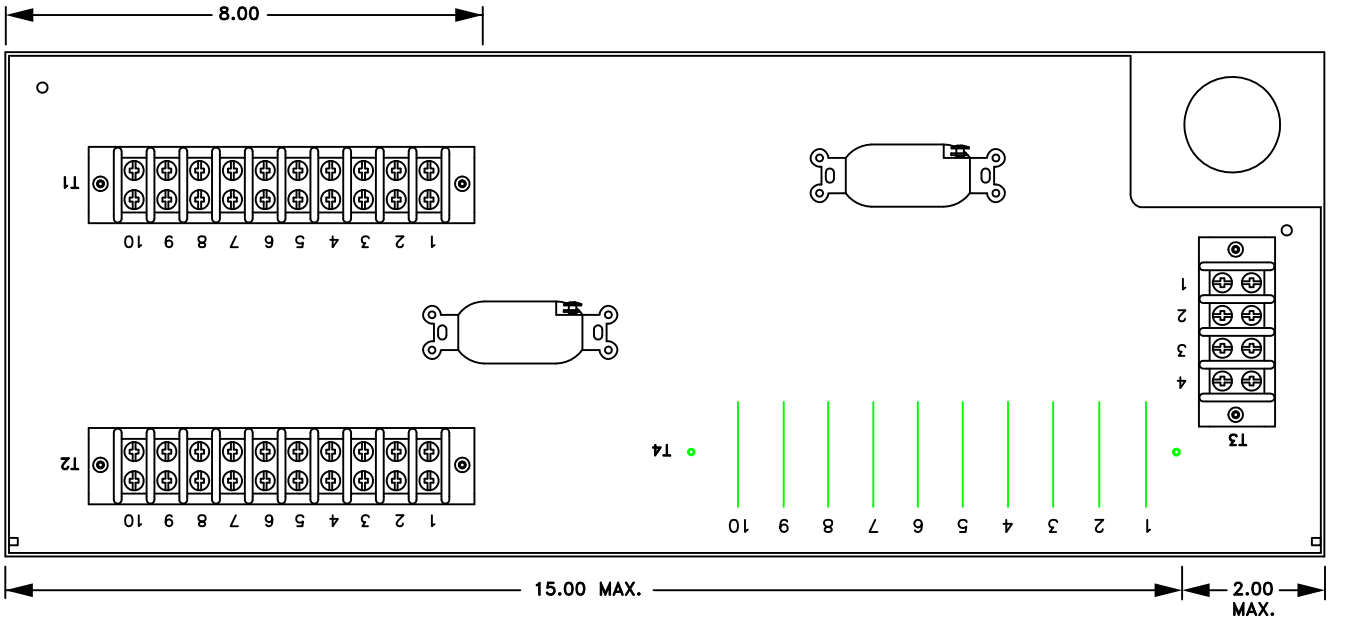
TITLE: PDA #2LX DETAILS SHEET 2 OF 8	
	NO SCALE
TEES 2020	A6-14







PDA #3LX REAR VIEW



VIEW A–A
(INSIDE REAR PANEL)

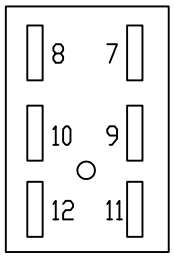
NOTE:

1. See A6–16 and A6–17 for more details.
2. All dimensions shown are in inches.

TITLE: PDA #3LX DETAILS SHEET 3 OF 8	
	NO SCALE
TEES 2020	A6–15

MODEL 204 FLASHER UNIT
CONNECTOR SOCKET WIRING DETAIL

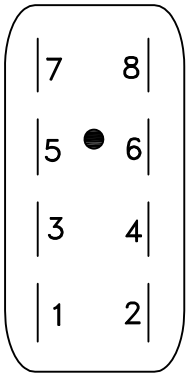
PIN NO.	FUNCTION
7	LD Ckt #1
8	LD Ckt #2
9	EG
10	AC- RAW
11	AC+ RAW
12	NA



REAR VIEW

MODEL 205 FLASH TRANSFER (HEAVY DUTY) RELAY SOCKET DETAIL

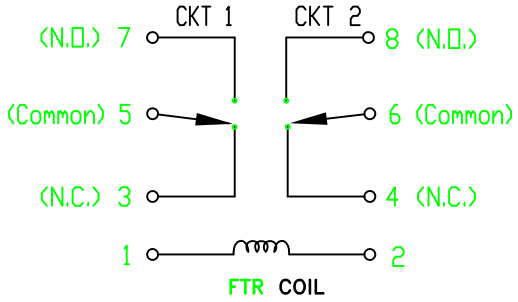
PIN	FUNCTION
1	COIL
2	COIL
3	N.C. CIRCUIT #1
4	N.C. CIRCUIT #2
5	COMMON CIRCUIT #1
6	COMMON CIRCUIT #2
7	N.O. CIRCUIT #1
8	N.O. CIRCUIT #2



REAR VIEW

MODEL 205 -
BEAU P-5408-LAB (Or Equal)

FLASH TRANSFER (HEAVY DUTY) RELAY CONNECTOR WIRING DETAIL



K24 RELAY PIN DETAIL

PIN	FUNCTION	
1	COIL AC+ (HI)	
2	-	
3	-	
4	COIL AC-	
5	N.C.	+24Vdc (Controlled)
6	COMMON	+24Vdc (PS)
7	N.O.	
8	N.C.	
9	COMMON	
10	N.O.	

HEALTH INDICATOR RELAY PIN DETAIL

PIN	FUNCTION	
1	COIL AC+ (flash)	
2	-	
3	-	
4	COIL AC-	
5	N.C.	
6	COMMON	(SSR, 2)
7	N.O.	(K24 COIL)
8	N.C.	
9	COMMON	
10	N.O.	

NOTE:

1. MODEL 205 - BEAU P-5408-LAB, Or Equal.
2. All dimensions shown are in inches

TITLE: PDA #2LX & #3LX DETAILS SHEET 4 OF 8	
	NO SCALE
TEES 2020	A6-16

POWER DISTRIBUTION ASSEMBLY TERMINAL BLOCK ASSIGNMENT DETAIL

PDA's	2LX, 2LS	2LX, 2LS	3LX	2LX, 2LS & 3LX	2LX,2LS	3LX
TERMINAL BLOCK	T1	T2		T3	T4	
SIDE / POS	A B	A B	A B	A B	A B	A B
1.	EG BUS / EG	EQ AC– / ER AC– UBS–2	EG BUS / EQ GND	24VDC BUS / PS–7	NA / NA	FL1 / SP 3–3
2.	AC– BUS / AC–	01–5 / FU1–7	AC– BUS / AC–	24VDC (CONTROLLED) / PS–7	NA / NA	FL2 / SP 3–5
3.	CR AC– / AC– CLEAN	01–6 / FU1–8	* / AC+ RAW	DC GND BUS / PS 8	NA / NA	FL3 / SP 3–7
4.	* / SCB CKT 5	01–7 / FU2–7	* / AC+ CLEAN	DC GND BUS / PS–8	NA / NA	FL4 / SP 2–3
5.	* / AC+ RAW	01–8 / FU2–8	* / MU		NA / NA	FL5 / SP 2–5
6.	CR AC+ / AC+ CLEAN	* / FTR DRIVE	* / TR COIL		NA / NA	FL6 / SP 2–7
7.	* / SSR	01–1 / SCB CKT 1	NA / TRC1NO		NA / NA	FL7 / SP 1–3
8.	* / SCB CKT 6	01–2 / SCB CKT 2	NA / TRC2NC		NA / NA	FL8 / SP 1–5
9.	* / FCB1 (SEC)	01–3 / SCB CKT 3	03–5 / FLD2		NA / NA	FL9 / SP 1–7
10.	* / ER AC+	01–4 / SCB CKT 4	SPA AC– CLEAN / AC– CLEAN		NA / NA	EQ / ER AC– AC– UBS–2

A = EXTERNAL SIDE B = INTERNAL SIDE * = WIRE PER ONE LINE DIAGRAM

NOTES: (FOR DETAILS A6–13 TO A6–17)

1. All dimensions shown are in inches.
2. Sheet Definitions:

CKT = CIRCUIT	EG = EQUIPMENT GROUND
FLD1 = FIELD 1 CIRCUIT BREAKER	FL1 = FIELD LOAD 1
FU1–7 = FLASHER UINT #1, PIN 7	ER = EQUIPMENT RECEPTACLE
L = LAMP	LD CKT#1 = LOAD CIRCUIT 1
SSR = SOLID STATE RELAY	CR = CONTROLLER RECEPTACLE
MN = MAIN	MU–22 = MONITOR UNIT – PIN 22
OD = OUTSIDE DIMENSION	POS = POSITION
PS–7 = POWER SUPPLY PIN 7	SCB = SIGNAL CIRCUIT BREAKER
SP 3–3 = SWITCH PACK 3, PIN 3	TR = TRANSFER RELAY
01–8 = OUTPUT FILE TB 01, POSITION 8	TRC1NO = TRANSFER RELAY CIRCUIT 1, NORMALLY OPEN
FCB1 = FIELD CIRCUIT BREAKER 1	
EQ = EQUIPMENT	

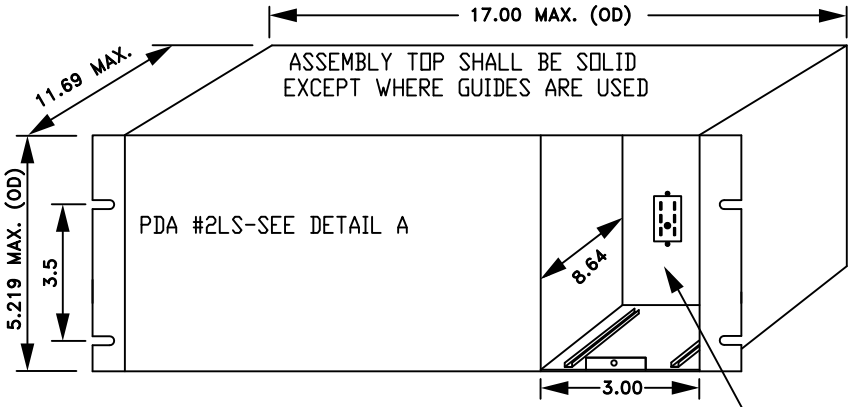
3. Thumb screw device.
4. Transfer relay in PDA #2LX, #2LS & #3LX shall extend no more than 1.0 inch out from the assembly front face.
5. Slack shall be provided in the wiring for the circuit breakers and GFCI receptacle to allow for the removal and repair. Excess bends and stress on the wiring shall be minimized.
6. See Output File plan sheet for heavy duty relay and switch pack wiring assignments and connector mounting location.
7. Wiring shall be routed (with extra length) to minize movement when front panel door is opened. The wiring going to the front panel shall be routed such that it does not cause undue twisting or bending of the wires.
8. No ventilation hole shall be large enough to place a 0.375 inch diameter object through.
9. If PDA #2LX or #2LS is installed, park the C1 harness #1 – C5S connector at the Input Panel's C5P. If PDA #3LX is intalled, the C1 harness #2 – C5S connector shall be connected to the PDA's C6P connector, support bracket and wiring shall be installed.
10. Hing shall fasten to PDA chassis with two acorn Stainles Steel nuts.
11. Terminal shall be 5–pin screw type, Weidmuller BLT–C10 or equivalent.

TITLE: PDA #2LX, #2LS & #3LX DETAILS
SHEET 5 OF 8

NO SCALE

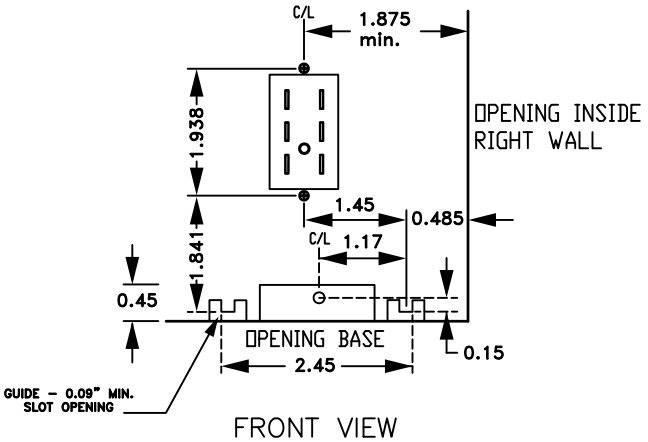
TEES 2020

A6–17

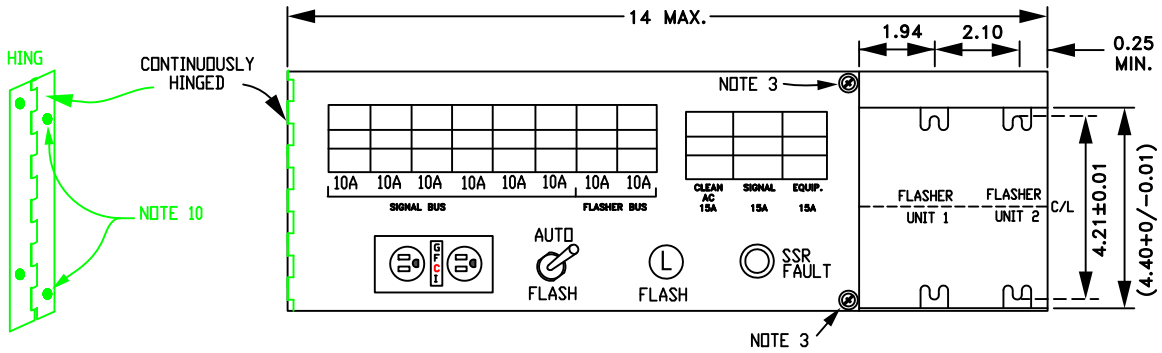


FRONT VIEW

POWER SUPPLY CONNECTOR/STUD MOUNTING DETAIL



FRONT VIEW

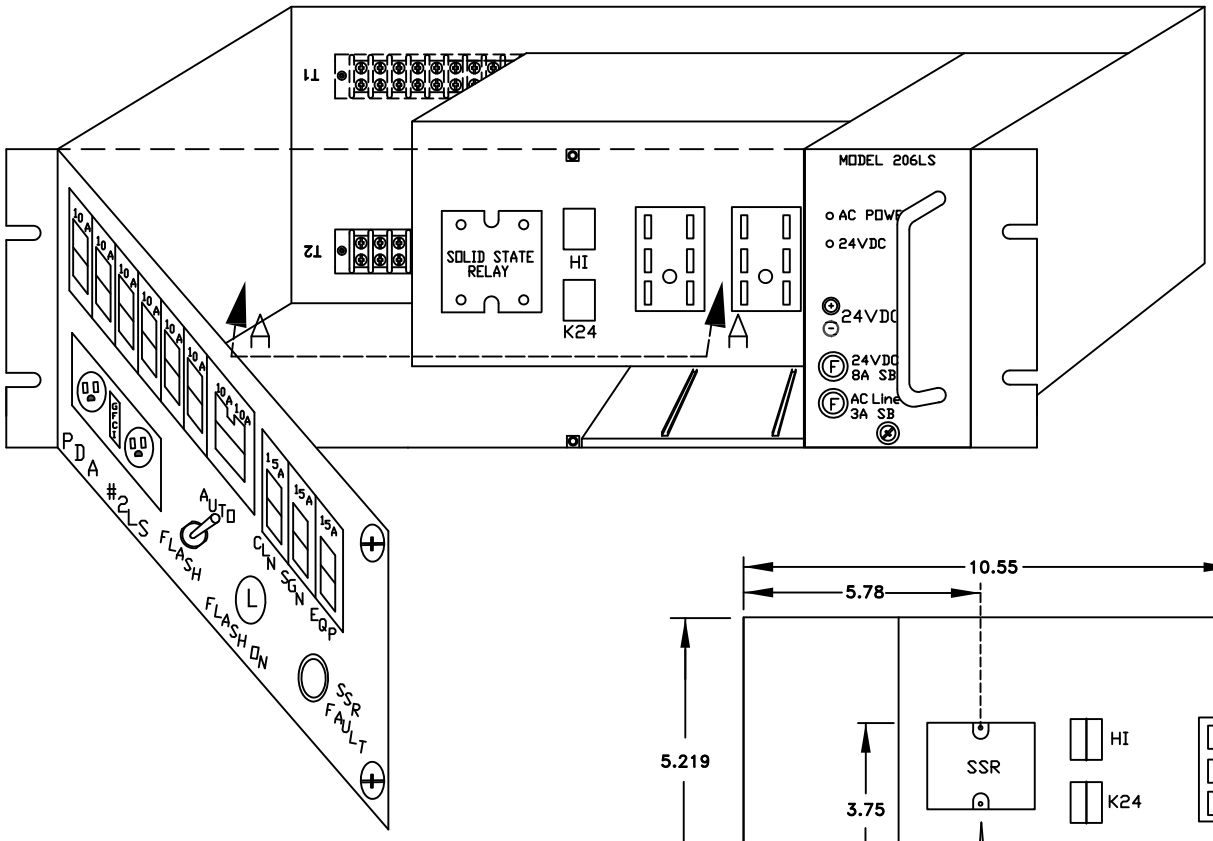


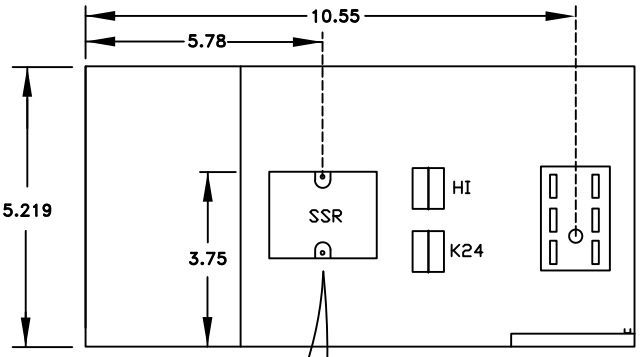
DETAIL A

NOTE:

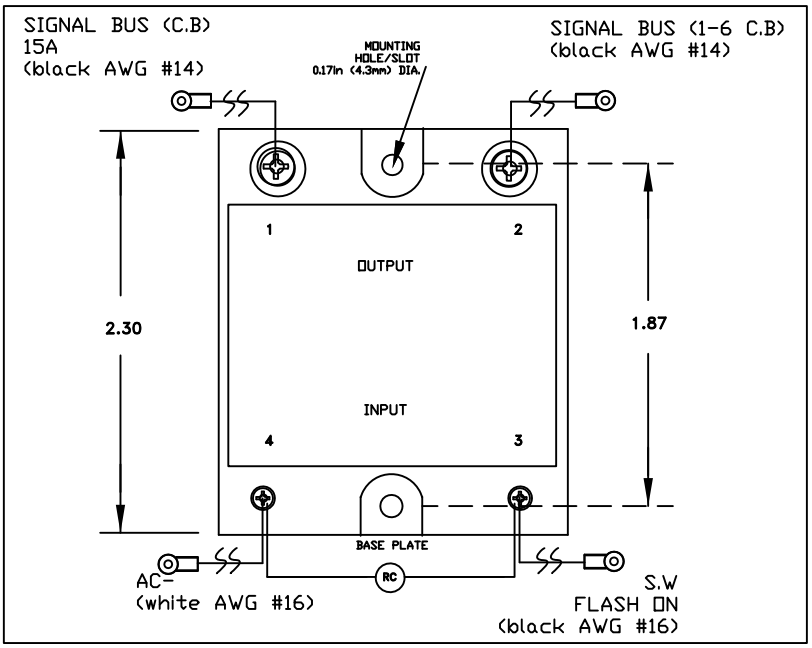
1. See A6-16 and A6-17 for more details.
2. All dimensions shown are in inches.

TITLE: PDA #2LS DETAILS SHEET 6 OF 8	
	NO SCALE
TEES 2020	A6-18





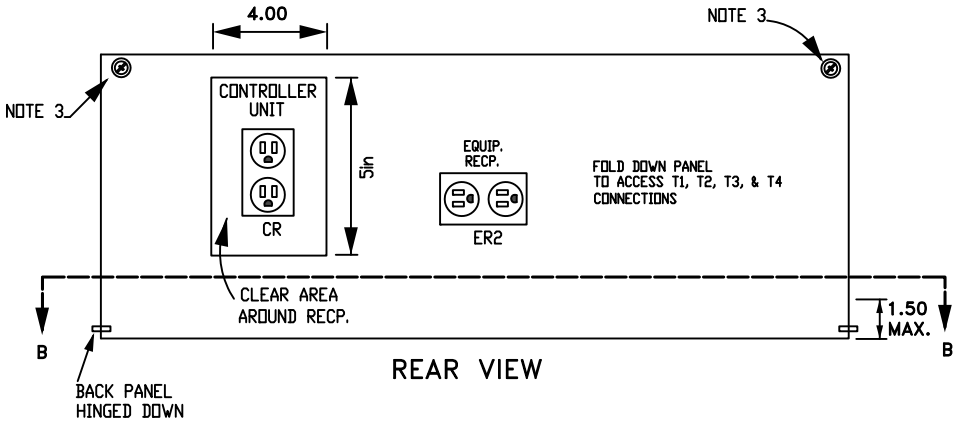
Section A-A



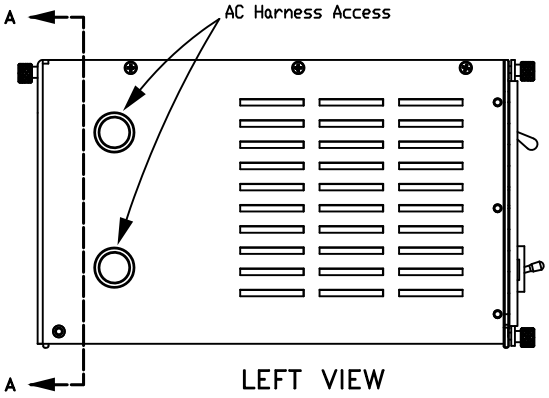
NOTE:

1. PDA top and bottom vented.
2. All dimensions shown are in inches.

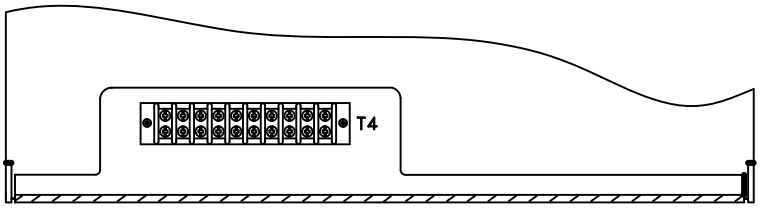
TITLE: PDA #2LS SSR INSTALLATION DETAILS SHEET 7 OF 8	
	NO SCALE
TEES 2020	A6-19



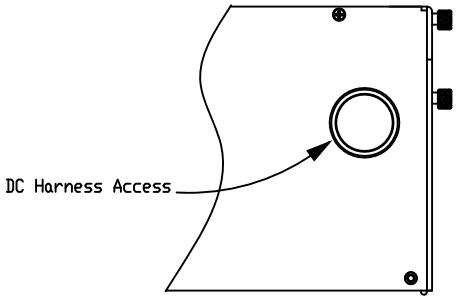
REAR VIEW



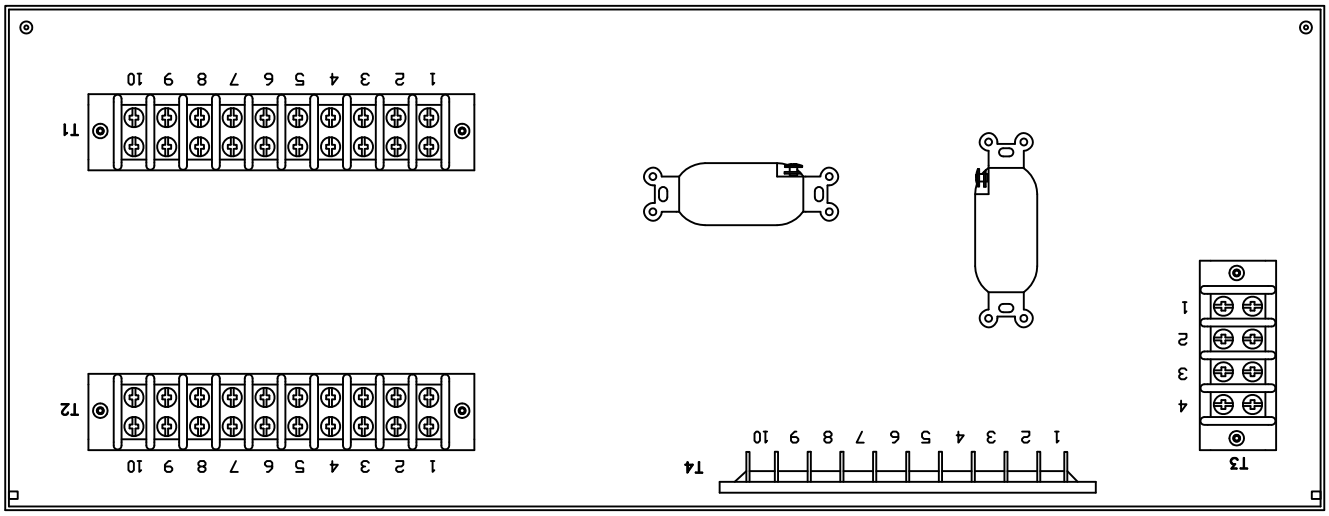
LEFT VIEW



VIEW B–B



RIGHT VIEW

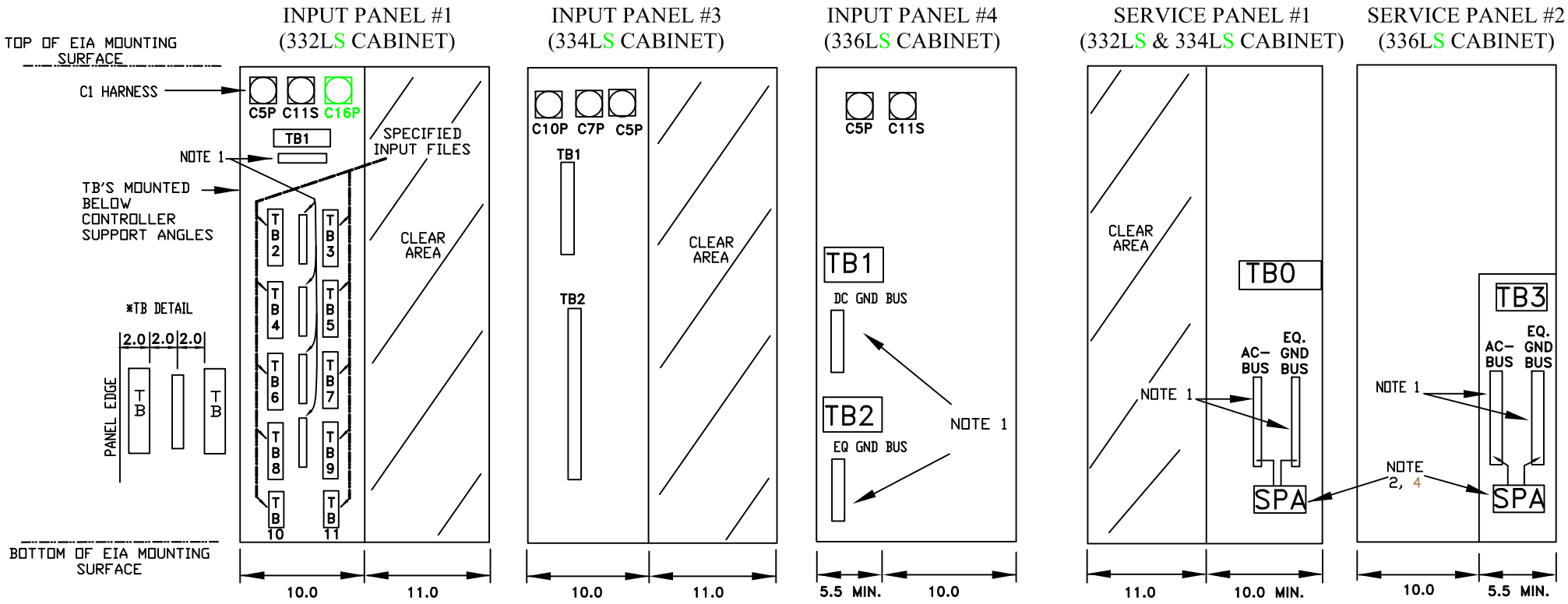


VIEW A–A
(INSIDE REAR PANEL)

NOTE:

See A6-16 and A6-17 for more details.

TITLE: PDA #2LS DETAILS SHEET 8 OF 8	
	NO SCALE
TEES 2020	A6-20



NOTES:

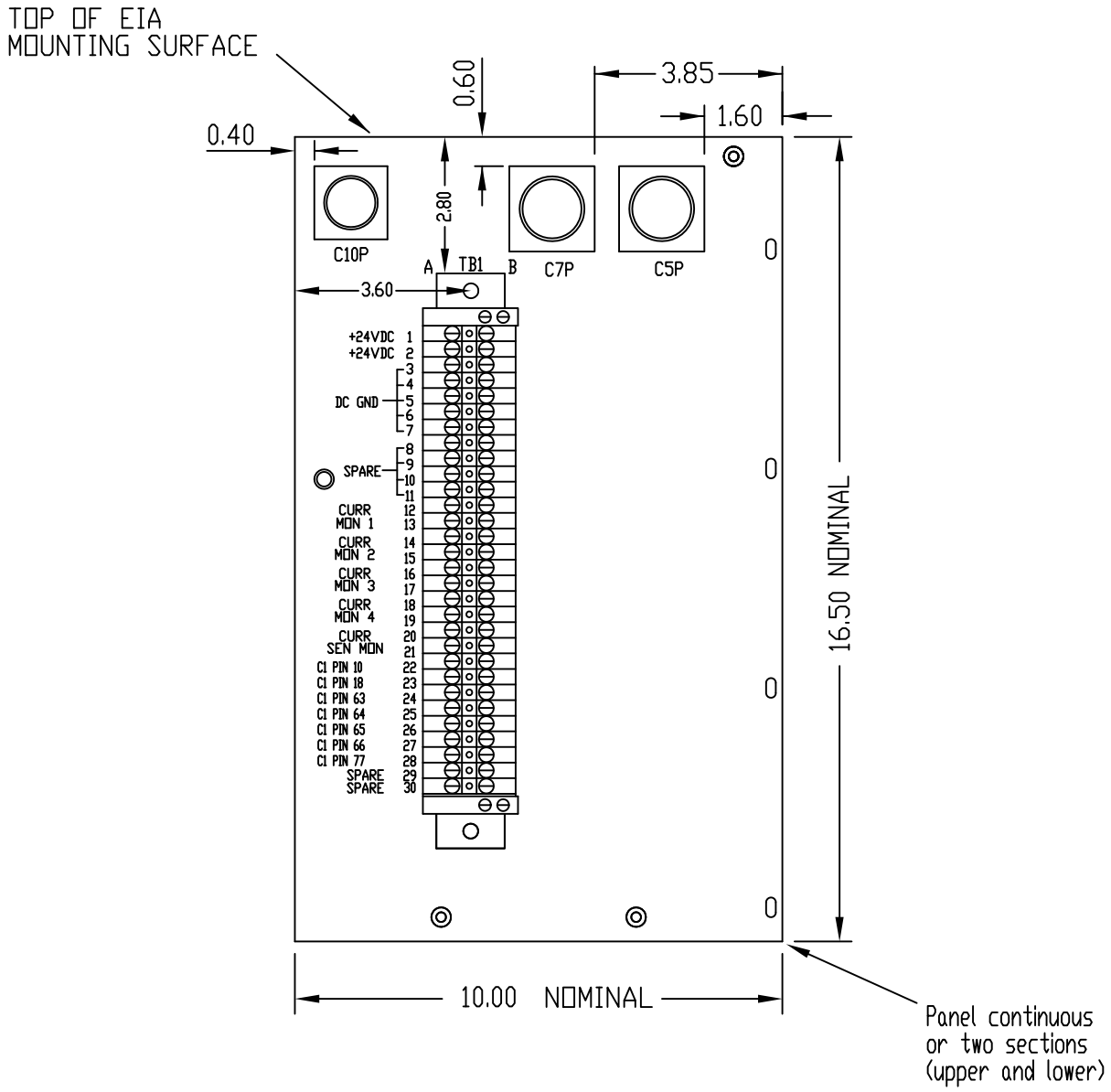
1. 10 terminal (#8 wire) minimum copper bus.
2. See service panel assembly details A6–10, A6–11 & A6–12.
3. The terminal block shall have terminal positions necessary to match position assignments. Terminal position screws shall be 8–32 except for TBS, TB0, TB0, TB3, which shall be 10–32
4. SPA shall be bolted on the Rail and firmly attached to the Service Panel.
5. All dimensions shown are in inches.

TITLE:
SIDE PANEL DETAILS
SHEET 1 OF 4

NO SCALE

TEES 2020

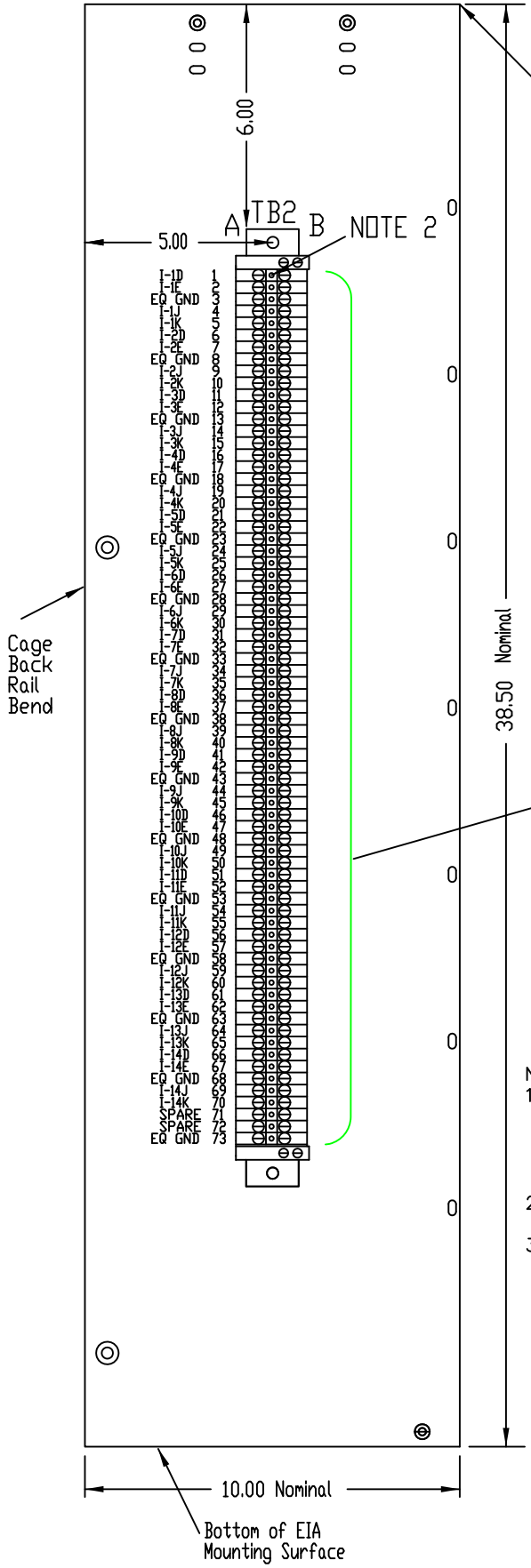
A6–21

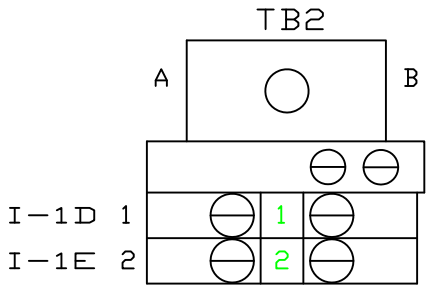


NOTES:

1. Provide and install a 30 position TB1 Terminal Block & three circular connectors, C5P, C7P & C10P (no contacts), TB1 shall be Open Construct Phoenix Contact Terminal Block UT 6, Weidmuller Terminal Block WDU 10 or equal, mounted on DIN Ralling (supported every 6 inches with position function label tabs and positions commoned and end locks.
2. A 4 foot length "CMS" Harness of 14 #20 (or larger) Conductors shall be furnished and installed in the cabinet. One end of the harness shall be the C10S Connector resting in C10P (mounted on the Input Panel #3) when not in used. The other end shall be stripped (according to manufacturers requirements) and connected to the "B Side" of TB1. The conductor bundle shall have external protection.
3. All dimensions shown are in inches.

TITLE: SIDE PANEL DETAILS SHEET 2 OF 4	
	No Scale
TEES 2020	A6-22





LABELING ON PANEL
AND TERMINAL BLOCK.

NOTES:
1. Provide and install a 73 position TB2 Terminal Block. TB2 shall be Open Construction Phoenix Contact Terminal Block UT 6, Weidmuller Terminal Block WDU 10 or equal, mounted on DIN Railing (supported every 6 inches) with position function label tabs and positions commoned and end locks.
2. All terminals to be labeled using manufacturer recommended plastic labels as shown above.
3. All dimensions shown are in inches.

TITLE: SIDE PANEL DETAIL SHEET 3 OF 4	
	No Scale
TEES 2020	A6-23

TERMINAL BLOCK ASSIGNMENT

332LS, 342LX INPUT PANEL #1

POS	A	B	POS	A	B
TB2-1 TB2-2	DET 1	I-1D I-1E	TB3-1 TB3-2	DET 21	J-1D J-1E
TB2-3 TB2-4	DET 2	I-1J I-1K	TB3-3 TB3-4	DET 22	J-1J J-1K
TB2-5 TB2-6	DET 3	I-2D I-2E	TB3-5 TB3-6	DET 23	J-2D J-2E
TB2-7 TB2-8	DET 4	I-2J I-2K	TB3-7 TB3-8	DET 24	J-2J J-2K
TB2-9 TB2-10	DET 5	I-3D I-3E	TB3-9 TB3-10	DET 25	J-3D J-3E
TB2-11 TB2-12	DET 6	I-3J I-3K	TB3-11 TB3-12	DET 26	J-3J J-3K
TB4-1 TB4-2	DET 7	I-4D I-4E	TB5-1 TB5-2	DET 27	J-4D J-4E
TB4-3 TB4-4	DET 8	I-4J I-4K	TB5-3 TB5-4	DET 28	J-4J J-4K
TB4-5 TB4-6	DET 9	I-5D I-5E	TB5-5 TB5-6	DET 29	J-5D J-5E
TB4-7 TB4-8	DET 10	I-5J I-5K	TB5-7 TB5-8	DET 30	J-5J J-5K
TB4-9 TB4-10	DET 11	I-6D I-6E	TB5-9 TB5-10	DET 31	J-6D J-6E
TB4-11 TB4-12	DET 12	I-6J I-6K	TB5-11 TB5-12	DET 32	J-6J J-6K
TB6-1 TB6-2	DET 13	I-7D I-7E	TB7-1 TB7-2	DET 33	J-7D J-7E
TB6-3 TB6-4	DET 14	I-7J I-7K	TB7-3 TB7-4	DET 34	J-7J J-7K
TB6-5 TB6-6	DET 15	I-8D I-8E	TB7-5 TB7-6	DET 35	J-8D J-8E
TB6-7 TB6-8	DET 16	I-8J I-8K	TB7-7 TB7-8	DET 36	J-8J J-8K
TB6-9 TB6-10	DET 17	I-9D I-9E	TB7-9 TB7-10	DET 37	J-9D J-9E
TB6-11 TB6-12	DET 18	I-9J I-9K	TB7-11 TB7-12	DET 38	J-9J J-9K
TB8-1 TB8-2	MANUAL SPARE	I-11D I-11J	TB9-1 TB9-2	Spare 2/ EVB Spare 3/ EVD	J-11D J-11J
TB8-3 TB8-4	11 COM PED Ø2	I-11K I-12D	TB9-3 TB9-4	11 COM EVA/ APP	J-11K J-12D
TB8-5 TB8-6	PED Ø4 12 COM	I-12J I-12K	TB9-5 TB9-6	EVC/ GD/ISL 12 COM/ GD/ISL DC-	J-12J J-12K
TB8-7 TB8-8	PED Ø6 PED Ø8	I-13D I-13J	TB9-7 TB9-8	EVB/ SIM PRI EVD/ SIM SEC	J-13D J-13J
TB8-9 TB8-10	13 COM FLH SENSE	I-13K I-14D	TB9-9 TB9-10	13 COM/ SIM DC- ADV PRI	J-13K J-14D
TB8-11 TB8-12	STOP TIME 14 COM	I-14J I-14K	TB9-11 TB9-12	ADV SEC 14 COM/ ADV DC-	J-14J J-14K
TB10-1 TB10-2	DET 19	I-10D I-10E	TB11-1 TB11-2	DET 39	J-10D J-10E
TB10-3 TB10-4	DET 20	I-10J I-10K	TB11-3 TB11-4	DET 40	J-10J J-10K

TB1- SEE INPUT PANEL #4 TB1 ASSIGNMENTS

334LS, 344LX INPUT PANEL #3, TB #1

POS	A	B
TB1-1	+24 VDC	I/O FILES
TB1-2	+24 VDC	CAB. HARNESS #5
TB1-3	DC GND	C1 PINS 1 & 104
TB1-4	DC GND	I/O FILES &
TB1-5	DC GND	CAB. HARNESS #5
TB1-6	DC GND	
TB1-7	DC GND	
TB1-8	SPARE	NA
TB1-9	SPARE	NA
TB1-10	SPARE	NA
TB1-11	SPARE	NA
TB1-12	CURR. MONITOR 1	CAB. HARNESS #5
TB1-13	CURR. MONITOR 1	CAB. HARNESS #5
TB1-14	CURR. MONITOR 2	CAB. HARNESS #5
TB1-15	CURR. MONITOR 2	CAB. HARNESS #5
TB1-16	CURR. MONITOR 3	CAB. HARNESS #5
TB1-17	CURR. MONITOR 3	CAB. HARNESS #5
TB1-18	CURR. MONITOR 4	CAB. HARNESS #5
TB1-19	CURR. MONITOR 4	CAB. HARNESS #5
TB1-20	CURR. SEN. MON.	CAB. HARNESS #5
TB1-21	CURR. SEN. MON.	CAB. HARNESS #5
TB1-22	C1 PIN 10	CIA CONTROL 4
TB1-23	C1 PIN 18	NA
TB1-24	C1 PIN 63	NA
TB1-25	C1 PIN 64	NA
TB1-26	C1 PIN 65	POL. CONTROL SW.
TB1-27	C1 PIN 66	POL. LIGHTS SW.
TB1-28	C1 PIN 77	NA
TB1-29	SPARE	CAB. HARNESS #5
TB1-30	SPARE	CAB. HARNESS #5

336LS, 346LX INPUT PANEL #4

TERM	A	B
TB1-1	(+24 VDC) O2-1/T3-1	I15-1, J15-1
TB1-2	M RESET	O2-5
TB1-3	O2-7/T3-2	C5-24
TB1-4	RESERVED	RESERVED (COMM IN)
TB1-5	RESERVED	RESERVED (COMM IN)
TB1-6	RESERVED	RESERVED (COMM OUT)
TB1-7	RESERVED	RESERVED (COMM OUT)
TB1-8	RESERVED	RESERVED
TB2-1 TO 6	NA	NA

334LS, 344LX INPUT PANEL #3, TB #2

POS	A	B	POS	A	B
TB2-1	1-1D		TB2-38	EQ. GND	
TB2-2	1-1E		TB2-39	1-8J	
TB2-3	EQ. GND		TB2-40	1-8K	
TB2-4	1-1J		TB2-41	1-9D	
TB2-5	1-1K		TB2-42	1-9E	
TB2-6	1-2D		TB2-43	EQ. GND	
TB2-7	1-2E		TB2-44	1-9J	
TB2-8	EQ. GND		TB2-45	1-9K	
TB2-9	1-2J		TB2-46	1-10D	
TB2-10	1-2K		TB2-47	1-10E	
TB2-11	1-3D		TB2-48	EQ. GND	
TB2-12	1-3E		TB2-49	1-10J	
TB2-13	EQ. GND		TB2-50	1-10K	
TB2-14	1-3J		TB2-51	1-11D	
TB2-15	1-3K		TB2-52	1-11E	
TB2-16	1-4D		TB2-53	EQ. GND	
TB2-17	1-4E		TB2-54	1-11J	
TB2-18	EQ. GND		TB2-55	1-11K	
TB2-19	1-4J		TB2-56	1-12D	
TB2-20	1-4K		TB2-57	1-12E	
TB2-21	1-5D		TB2-58	EQ. GND	
TB2-22	1-5E		TB2-59	1-12J	
TB2-23	EQ. GND		TB2-60	1-12K	
TB2-24	1-5J		TB2-61	1-13D	
TB2-25	1-5K		TB2-62	1-13E	
TB2-26	1-6D		TB2-63	EQ. GND	
TB2-27	1-6E		TB2-64	1-13J	
TB2-28	EQ. GND		TB2-65	1-13K	
TB2-29	1-6J		TB2-66	1-14D	
TB2-30	1-6K		TB2-67	1-14E	
TB2-31	1-7D		TB2-68	EQ. GND	
TB2-32	1-7E		TB2-69	1-14J	
TB2-33	EQ. GND		TB2-70	1-14K	
TB2-34	1-7J		TB2-71	SPARE	
TB1-35	1-7K		TB1-72	SPARE	
TB1-36	1-8D		TB1-73	EQ. GND	
TB2-37	1-8E				

33xLS, 34xLX SERVICE PANEL 1, 336LS, 346LX SERVICE PANEL 2

TERM	A	B
TBS-1	AC+	TO PDA (without BBS) TO BBS-1 (with BBS)
TBS-2	AC-	AC- BUS
TBS-3	GND	TO EQ.GND BUS
BBS-1	AC+ IN	MBPS AC+ IN
BBS-2	MBPS AC+ OUT	TO PDA
TB0-1 TO 12	NA	NA
TB3-1 TO 6	NA	NA

See Service Panel Assembly (SPA) details A6-10, A6-11 & A6-40

NOTES:

1. Sheet Definitions:
   - 11 COM = DC COMMON
   - COMM = COMMUNICATION
   - DET1 = DETECTOR #1
   - EVA = EMERGENCY VEHICLE PREEMPTION A
   - IFI-1D = INPUT FILE 1, SLOT 1, CONNECTOR PIN D
   - OF = OUTPUT FILE
   - M = MONITOR MODULE
   - NA = NOT ASSIGNED
   - RR1 = RAILROAD PREEMPTION 1
   - MBPS = MANUAL BYPASS SWITCH
   - BBS = BATTERY BACK-UP SYSTEM
   - PDA = POWER DISTRIBUTION ASSEMBLY
   - x = 2, 4
   - ADV = Advance
   - APP = Advance Pedestrian Preemption
   - GD = Gate Down, ISL = Island
   - SIM = Simultanous, PRI = Primary, SEC = Secondary
2. All dimensions shown are in inches.

TITLE:

SIDE PANEL DETAILS
SHEET 4 OF 4

NO SCALE

TEES 2020

A6-24

C1 HARNESS WIRING LIST #1

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC GND	DC GND BUS	–	53	I2-7	IFI-11W	SPARE #1
2	O1-1	C4-1	SWPK 4P-RED	54	I2-8	IFJ-11F	EVB
3	O1-2	C4-2	SWPK 4P-GRN	55	I3-1	IFJ-1F	5 CE
4	O1-3	C4-3	SWPK 4-RED	56	I3-2	IFI-1F	1 CE
5	O1-4	C4-4	SWPK 4-YEL	57	I3-3	IFJ-5F	7 CE
6	O1-5	C4-5	SWPK 4-GRN	58	I3-4	IFI-5F	3 CE
7	O1-6	C4-6	SWPK 3-RED	59	I3-5	IFJ-9F	5 CE
8	O1-7	C4-7	SWPK 3-YEL	60	I3-6	IFI-9F	1 CE
9	O1-8	C4-8	SWPK 3-GRN	61	I3-7	IFJ-9W	7 CE
10	O2-1	C4-9	SWPK 2P-RED	62	I3-8	IFI-9W	3 CE
11	O2-2	C4-10	SWPK 2P-GRN	63	I4-5	IFI-3F	2 CE
12	O2-3	C4-11	SWPK 2-RED	64	I4-6	IFJ-3F	6 CE
13	O2-4	C4-12	SWPK 2-YEL	65	I4-7	IFI-7F	4 CE
14	DC GND	IFI-15-4	INPUT DC GND	66	I4-8	IFJ-7F	8 CE
15	O2-5	C4-13	SWPK 2-GRN	67	I5-1	IFI-12F	2 PED
16	O2-6	C4-14	SWPK 1-RED	68	I5-2	IFI-13F	6 PED
17	O2-7	C4-15	SWPK 1-YEL	69	I5-3	IFI-12W	4 PED
18	O2-8	C4-16	SWPK 1-GRN	70	I5-4	IFI-13W	8 PED
19	O3-1	C4-17	SWPK 8P-RED	71	I5-5	IFJ-12F	EVA / APP
20	O3-2	C4-18	SWPK 8P-GRN	72	I5-6	IFJ-13F	EVB / SIM PRI
21	O3-3	C4-19	SWPK 8-RED	73	I5-7	IFJ-12W	EVC / GD,ISL
22	O3-4	C4-20	SWPK 8-YEL	74	I5-8	IFJ-13W	EVD / SIM SEC
23	O3-5	C4-21	SWPK 8-GRN	75	I6-1	IFJ-11W	SPARE #3
24	O3-6	C4-22	SWPK 7-RED	76	I6-2	IFI-3W	2 CE
25	O3-7	C4-23	SWPK 7-YEL	77	I6-3	IFJ-3W	6 CE
26	O3-8	C4-24	SWPK 7-GRN	78	I6-4	IFI-7W	4 CE
27	O4-1	C4-25	SWPK 6P-RED	79	I6-5	IFJ-7W	8 CE
28	O4-2	C4-26	SWPK 6P-GRN	80	I6-6	IFI-11F	ADVANCE
29	O4-3	C4-27	SWPK 6-RED	81	I6-7	IFI-14F	FLASH SENSE
30	O4-4	C4-28	SWPK 6-YEL	82	I6-8	IFI-14W	STOP TIME
31	O4-5	C4-29	SWPK 6-GRN	83	O6-1	C5-1	SWPK 14-RED N/A
32	O4-6	C4-30	SWPK 5-RED	84	O6-2	C5-2	SWPK 14-GRN N/A
33	O4-7	C4-31	SWPK 5-YEL	85	O6-3	C5-3	SWPK 13-RED
34	O4-8	C4-32	SWPK 5-GRN	86	O6-4	C5-4	SWPK 13-YEL
35	O5-1	C4-33	SWPK 2P-YEL	87	O6-5	C5-5	SWPK 13-GRN
36	O5-2	C4-34	SWPK 6P-YEL	88	O6-6	C5-6	SWPK 12-RED
37	O5-3	C4-35	SWPK 4P-YEL	89	O6-7	C5-7	SWPK 12-YEL
38	O5-4	C4-36	SWPK 8P-YEL	90	O6-8	C5-8	SWPK 12-GRN
39	I1-1	IFI-2F	2 CE	91	O7-1	C5-9	SWPK 11-RED HS
40	I1-2	IFJ-2F	6 CE	92	DC GND	DC GND BUS	–
41	I1-3	IFI-6F	4 CE	93	O7-2	C5-10	SWPK 11-GRN GPO2
42	I1-4	IFJ-6F	8 CE	94	O7-3	C5-11	SWPK 10-RED
43	I1-5	IFI-2W	2 CE	95	O7-4	C5-12	SWPK 10-YEL
44	I1-6	IFJ-2W	6 CE	96	O7-5	C5-13	SWPK 10-GRN
45	I1-7	IFI-6W	4 CE	97	O7-6	C5-14	SWPK 9-RED
46	I1-8	IFJ-6W	8 CE	98	O7-7	C5-15	SWPK 9-YEL
47	I2-1	IFI-4F	2 CALL	99	O7-8	C5-16	SWPK 9-GRN
48	I2-2	IFJ-4F	6 CALL	100	O5-5	C5-17	SWPK 14-YEL N/A
49	I2-3	IFI-8F	4 CALL	101	O5-6	C5-18	SWPK 11-YEL GPO1
50	I2-4	IFJ-8F	8 CALL	102	O5-7	IFI&J-15-3	DETECTOR RESET
51	I2-5	IFJ-14F	RR1 PRE / ADV. PRI	103	O5-8	C4-37	WDT-MU
52	I2-6	IFJ-14W	RR2 PRE / ADV. SEC	104	DC GND	IFJ-15-4	INPUT DC GND

TITLE:

HARNESS WIRING DETAILS
SHEET 1 OF 5

NO SCALE

TEES 2020

A6-25

C1 HARNESS WIRING LIST #2

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC GND	TB1/3-7	DC GND BUS	53	I2-7	IFI-11F	RATE CODE 2
2	O1-1	C6-1	SWPK 1-RED	54	I2-8	IFI-11W	RATE CODE 1
3	O1-2	C6-2	SWPK 1-GRN	55	I3-1	IFI-4F	MAIN 9
4	O1-3	C6-3	SWPK 2-RED	56	I3-2	IFI-4W	MAIN 10
5	O1-4	C6-4	SWPK 2-YEL	57	I3-3	IFI-6F	MAIN 3
6	O1-5	C6-5	SWPK 2-GRN	58	I3-4	IFI-6W	MAIN 4
7	O1-6	C6-6	SWPK 3-RED	59	I3-5	IFI-7F	MAIN 5
8	O1-7	C6-7	SWPK 3-YEL	60	I3-6	IFI-7W	MAIN 6
9	O1-8	C6-8	SWPK 3-GRN	61	I3-7	IFI-8F	MAIN 11
10	O2-1	TB1/22	CIA CONTROL 4	62	I3-8	IFI-8W	MAIN 12
11	O2-2	C7-25	CMS CLOCK	63	I4-5	TB1/24	MAIN 17
12	O2-3	C7-26	CMS ENABLE	64	I4-6	TB1/25	MAIN 18
13	O2-4	C7-27	CMS CLEAR	65	I4-7	TB1/26	POL. CONTR'L SW.
14	DC GND	IFI-15-4	INPUT DC GND	66	I4-8	TB1/27	POL. LIGHTS SW.
15	O2-5	C7-28	CMS DIM LEVEL 1	67	I5-1	C7-16	CIA SENSE 1
16	O2-6	C7-29	CMS DIM LEVEL 2	68	I5-2	C7-31	CIA SENSE 2
17	O2-7	C7-30	CMS DIM LEVEL 3	69	I5-3	C7-32	CIA SENSE 3
18	O2-8	TB1/23	-	70	I5-4	C7-33	CIA SENSE 4
19	O3-1	C7-9	CMS ADDRESS 1	71	I5-5	C7-34	CIA SENSE 5
20	O3-2	C7-10	CMS ADDRESS 2	72	I5-6	C7-35	CIA SENSE 6
21	O3-3	C7-11	CMS ADDRESS 3	73	I5-7	C7-36	CIA SENSE 7
22	O3-4	C7-12	CMS ADDRESS 4	74	I5-8	C7-37	CIA SENSE 8
23	O3-5	C7-13	CMS ADDRESS 5	75	I6-1	C7-5	CMS LATCH
24	O3-6	C7-14	CMS ADDRESS 6	76	I6-2	C7-6	PHASE FIRE
25	O3-7	C7-15	CMS ADDRESS 7	77	I6-3	TB1/29	MAIN 19
26	O3-8	C7-4	CIA CONTROL 5	78	I6-4	C7-8	CMS TEST REQ.
27	O4-1	C7-17	CMS DATA 1	79	I6-5	IFI-10F	MAIN 15
28	O4-2	C7-18	CMS DATA 2	80	I6-6	IFI-9W	MAIN 14
29	O4-3	C7-19	CMS DATA 3	81	I6-7	IFI-9F	MAIN 13
30	O4-4	C7-20	CMS DATA 4	82	I6-8	IFI-10W	MAIN 16
31	O4-5	C7-21	CMS DATA 5	83	O6-1	C5-1	SWPK 14-RED
32	O4-6	C7-22	CMS DATA 6	84	O6-2	C5-2	SWPK 14-GRN
33	O4-7	C7-23	CMS DATA 7	85	O6-3	C5-3	SWPK 13-RED
34	O4-8	C7-24	CMS DATA 8	86	O6-4	C5-4	SWPK 13-YEL
35	O5-1	C7-1	CIA CONTROL 1	87	O6-5	C5-5	SWPK 13-GRN
36	O5-2	C7-2	CIA CONTROL 2	88	O6-6	C5-6	SWPK 12-RED
37	O5-3	C6-9	SWPK 1-YEL	89	O6-7	C5-7	SWPK 12-YEL
38	O5-4	C7-3	CIA CONTROL 3	90	O6-8	C5-8	SWPK 12-GRN
39	I1-1	IFI-1W	PASSAGE 1	91	O7-1	C5-9	SWPK 11-RED
40	I1-2	IFI-12W	PASSAGE 2	92	DC GND	TB1/3-7	-
41	I1-3	IFI-12F	DEMAND 2	93	O7-2	C5-10	SWPK 11-GRN
42	I1-4	IFI-13W	OFF RAMP 2	94	O7-3	C5-11	SWPK 10-RED
43	I1-5	IFI-13F	QUE 2	95	O7-4	C5-12	SWPK 10-YEL
44	I1-6	IFI-14W	PASSAGE 3	96	O7-5	C5-13	SWPK 10-GRN
45	I1-7	IFI-14F	DEMAND 3	97	O7-6	C5-14	SWPK 9-RED
46	I1-8	IFI-1F	DEMAND 1	98	O7-7	C5-15	SWPK 9-YEL
47	I2-1	IFI-2W	OFF RAMP 1	99	O7-8	C5-16	SWPK 9-GRN
48	I2-2	IFI-3W	MAIN 7	100	O5-5	C5-17	SWPK 14-YEL
49	I2-3	IFI-3F	MAIN 8	101	O5-6	C5-18	SWPK 11-YEL
50	I2-4	IFI-2F	QUE 1	102	O5-7	IFI-15-3	DETECTOR RESET
51	I2-5	IFI-5F	MAIN 1	103	O5-8	C6-10	WDT
52	I2-6	IFI-5W	MAIN 2	104	DC GND	TB1/3-7	DC GND BUS

TITLE: HARNESS WIRING DETAILS SHEET 2 OF 5	
	NO SCALE
TEES 2020	A6-26

C1 HARNESS WIRING LIST #3

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC GND	DC GND BUS		53	I2-7	TB2-5	SPARE #1
2	O1-1	C4-1	SWPK 4P-RED	54	I2-8	TB2-6	SPARE #2
3	O1-2	C4-2	SWPK 4P-GRN	55	I3-1	IFI-5F	5 CE
4	O1-3	C4-3	SWPK 4-RED	56	I3-2	IFI-1F	1 CE
5	O1-4	C4-4	SWPK 4-YEL	57	I3-3	IFI-7F	7 CE
6	O1-5	C4-5	SWPK 4-GRN	58	I3-4	IFI-3F	3 CE
7	O1-6	C4-6	SWPK 3-RED	59	I3-5	IFI-1SP	–
8	O1-7	C4-7	SWPK 3-YEL	60	I3-6	IFI-2SP	–
9	O1-8	C4-8	SWPK 3-GRN	61	I3-7	IFI-3SP	–
10	O2-1	C4-9	SWPK 2P-RED	62	I3-8	IFI-4SP	–
11	O2-2	C4-10	SWPK 2P-GRN	63	I4-5	IFI-5SP	–
12	O2-3	C4-11	SWPK 2-RED	64	I4-6	IFI-6SP	–
13	O2-4	C4-12	SWPK 2-YEL	65	I4-7	IFI-7SP	–
14	DC GND	IFI-15-4	INPUT DC GND	66	I4-8	IFI-8SP	–
15	O2-5	C4-13	SWPK 2-GRN	67	I5-1	IFI-12F	2 PED
16	O2-6	C4-14	SWPK 1-RED	68	I5-2	IFI-13F	6 PED
17	O2-7	C4-15	SWPK 1-YEL	69	I5-3	IFI-12W	4 PED
18	O2-8	C4-16	SWPK 1-GRN	70	I5-4	IFI-13W	8 PED
19	O3-1	C4-17	SWPK 8P-RED	71	I5-5	IFI-10F	EVA PREEMPT
20	O3-2	C4-18	SWPK 8P-GRN	72	I5-6	IFI-11F	EVB PREEMPT
21	O3-3	C4-19	SWPK 8-RED	73	I5-7	IFI-10W	EVC PREEMPT
22	O3-4	C4-20	SWPK 8-YEL	74	I5-8	IFI-11W	EVD PREEMPT
23	O3-5	C4-21	SWPK 8-GRN	75	I6-1	IFI-9SP	SPARE #3
24	O3-6	C4-22	SWPK 7-RED	76	I6-2	IFI-10SP	2 CE
25	O3-7	C4-23	SWPK 7-YEL	77	I6-3	IFI-11SP	6 CE
26	O3-8	C4-24	SWPK 7-GRN	78	I6-4	IFI-12SP	4 CE
27	O4-1	C4-25	SWPK 6P-RED	79	I6-5	IFI-13SP	8 CE
28	O4-2	C4-26	SWPK 6P-GRN	80	I6-6	IFI-14SP	ADVANCE
29	O4-3	C4-27	SWPK 6-RED	81	I6-7	IFI-14F	FLASH SENSE
30	O4-4	C4-28	SWPK 6-YEL	82	I6-8	IFI-14W	STOP TIME
31	O4-5	C4-29	SWPK 6-GRN	83	O6-1	NA	–
32	O4-6	C4-30	SWPK 5-RED	84	O6-2	NA	–
33	O4-7	C4-31	SWPK 5-YEL	85	O6-3	NA	–
34	O4-8	C4-32	SWPK 5-GRN	86	O6-4	NA	–
35	O5-1	C4-33	SWPK 2P-YEL	87	O6-5	NA	–
36	O5-2	C4-34	SWPK 6P-YEL	88	O6-6	NA	–
37	O5-3	C4-35	SWPK 4P-YEL	89	O6-7	NA	–
38	O5-4	C4-36	SWPK 8P-YEL	90	O6-8	NA	–
39	I1-1	IFI-2F	2 CE	91	O7-1	NA	–
40	I1-2	IFI-6F	6 CE	92	DC GND	DC GND BUS	–
41	I1-3	IFI-4F	4 CE	93	O7-2	NA	–
42	I1-4	IFI-8F	8 CE	94	O7-3	NA	–
43	I1-5	IFI-2W	2 CE	95	O7-4	NA	–
44	I1-6	IFI-6W	6 CE	96	O7-5	NA	–
45	I1-7	IFI-4W	4 CE	97	O7-6	NA	–
46	I1-8	IFI-8W	8 CE	98	O7-7	NA	–
47	I2-1	IFI-1W	2 CALL	99	O7-8	NA	–
48	I2-2	IFI-5W	6 CALL	100	O5-5	NA	–
49	I2-3	IFI-3W	4 CALL	101	O5-6	NA	–
50	I2-4	IFI-7W	8 CALL	102	O5-7	IFI-15-3	DETECTOR RESET
51	I2-5	IFI-9F	RR1 PREEMPT	103	O5-8	C4-37	WDT-MU
52	I2-6	IFI-9W	RR2 PREEMPT	104	DC GND	IFJ-15-4	–

TITLE: HARNESS WIRING DETAILS SHEET 3 OF 5	
	NO SCALE
TEES 2020	A6-27

C4 HARNESS WIRING LIST #1 AND #3

PIN	SOURCE	DESTINATION
1	C1-2	SWPK 4P-RED
2	C1-3	SWPK 4P-GRN
3	C1-4	SWPK 4-RED
4	C1-5	SWPK 4-YEL
5	C1-6	SWPK 4-GRN
6	C1-7	SWPK 3-RED
7	C1-8	SWPK 3-YEL
8	C1-9	SWPK 3-GRN
9	C1-10	SWPK 2P-RED
10	C1-11	SWPK 2P-GRN
11	C1-12	SWPK 2-RED
12	C1-13	SWPK 2-YEL
13	C1-15	SWPK 2-GRN
14	C1-16	SWPK 1-RED
15	C1-17	SWPK 1-YEL
16	C1-18	SWPK 1-GRN
17	C1-19	SWPK 8P-RED
18	C1-20	SWPK 8P-GRN
19	C1-21	SWPK 8-RED
20	C1-22	SWPK 8-YEL
21	C1-23	SWPK 8-GRN
22	C1-24	SWPK 7-RED
23	C1-25	SWPK 7-YEL
24	C1-26	SWPK 7-GRN
25	C1-27	SWPK 6P-RED
26	C1-28	SWPK 6P-GRN
27	C1-29	SWPK 6-RED
28	C1-30	SWPK 6-YEL
29	C1-31	SWPK 6-GRN
30	C1-32	SWPK 5-RED
31	C1-33	SWPK 5-YEL
32	C1-34	SWPK 5-GRN
33	C1-35	SWPK 2P-YEL
34	C1-36	SWPK 6P-YEL
35	C1-37	SWPK 4P-YEL
36	C1-38	SWPK 8P-YEL
37	C1-103	SWPK WDT-MU

C5 HARNESS WIRING LIST #1 AND #2

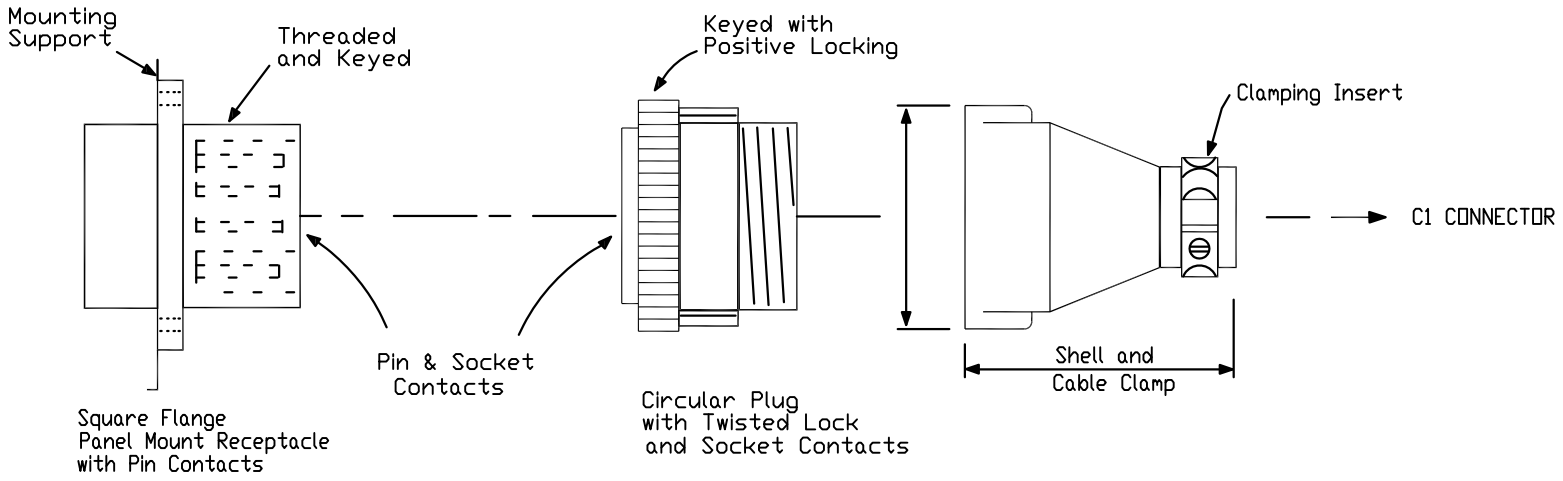
PIN	SOURCE	DESTINATION
1	C1-83	SWPK 14-RED N/A
2	C1-84	SWPK 14-GRN N/A
3	C1-85	SWPK 13-RED
4	C1-86	SWPK 13-YEL
5	C1-87	SWPK 13-GRN
6	C1-88	SWPK 12-RED
7	C1-89	SWPK 12-YEL
8	C1-90	SWPK 12-GRN
9	C1-91	SWPK 11-RED HS
10	C1-93	SWPK 11-GRN GPO2
11	C1-94	SWPK 10-RED
12	C1-95	SWPK 10-YEL
13	C1-96	SWPK 10-GRN
14	C1-97	SWPK 9-RED
15	C1-98	SWPK 9-YEL
16	C1-99	SWPK 9-GRN
17	C1-100	SWPK 14-YEL N/A
18	C1-101	SWPK 11-YEL GPO1
19	NA	NA
20	NA	NA
21	NA	NA
22	NA	NA
23	NA	NA
24	+24 VDC	PIN 9, ALL SOCKETS

C6 HARNESS WIRING LIST #2

PIN	SOURCE	DESTINATION
1	C1-2	SWPK 1-RED
2	C1-3	SWPK 1-GRN
3	C1-4	SWPK 2-RED
4	C1-5	SWPK 2-YEL
5	C1-6	SWPK 2-GRN
6	C1-7	SWPK 3-RED
7	C1-8	SWPK 3-YEL
8	C1-9	SWPK 3-GRN
9	C1-37	SWPK 1-YEL
10	C1-103	WDT
11	NA	NA
12	NA	NA
13	NA	NA
14	NA	NA
15	NA	NA
16	NA	NA
17	NA	NA
18	NA	NA
19	NA	NA
20	NA	NA
21	NA	NA
22	NA	NA
23	NA	NA
24	+24 VDC	PIN 9, ALL SOCKETS

TITLE: HARNESS WIRING DETAILS SHEET 4 OF 5	
	NO SCALE
TEES 2020	A6-28

CONNECTORS C4, C5 AND C6



NOTE: (FOR DETAILS A6–25 to A6–29)

1. Sheet definitions:

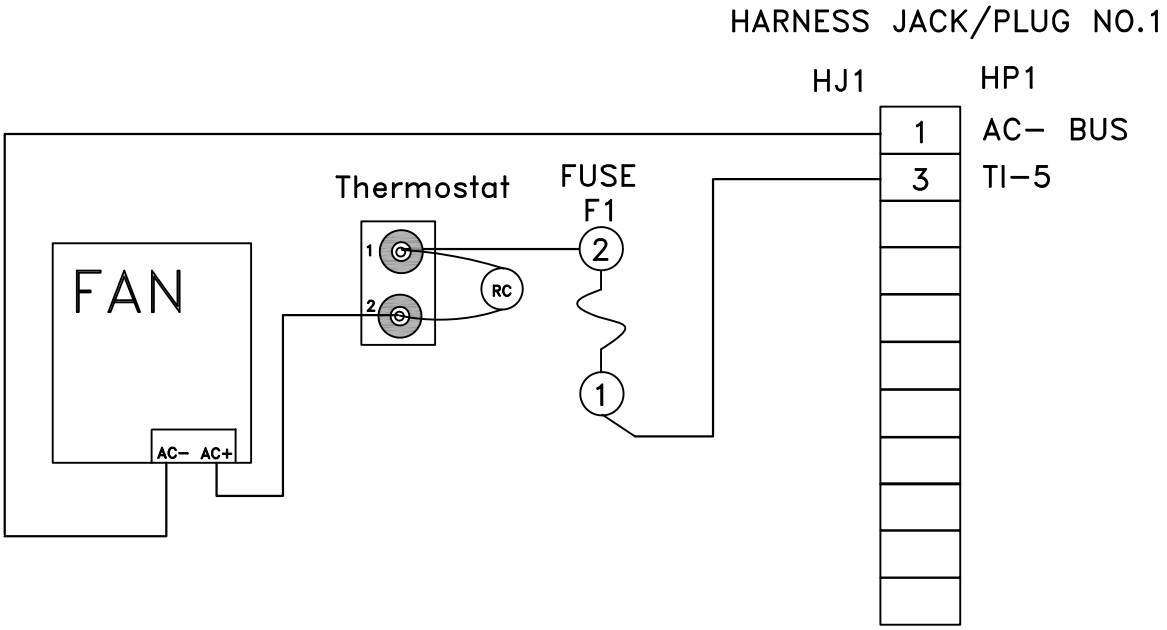
C1–2	= CONNECTOR C1, PIN 2
EVA	= EMERGENCY VEHICLE A
I1–1	= INPUT PORT 5001, BIT 1
IFI–2F, SP	= INPUT FILE 1, TERMINAL BLOCK 2, TERMINAL DESIGNATION F (CHANNEL 1 OUTPUT), SPARE
IFJ–6W	= INPUT FILE J, TERMINAL BLOCK 6, TERMINAL DESIGNATION W (CHANNEL 2 OUTPUT)
O1–1	= OUTPUT PORT 5001, BIT 1
TB1/26	= TERMINAL BLOCK 1 POSITION 26
RR1	= RAILROAD 1
SWPK 2P–GRN	= SWITCHPACK 2 PEDESTRIAN, GREEN
WDT–MU	= WATCHDOG TIMER, MONITOR UNIT
2 CE	= PHASE 2 COUNT & EXTENSION

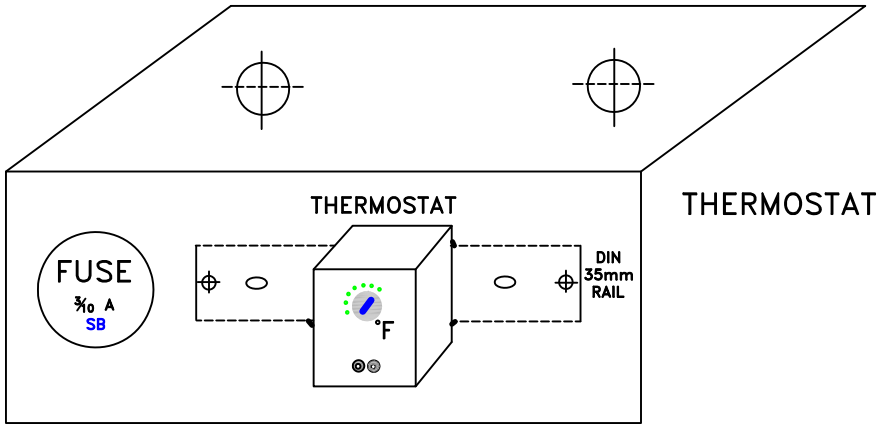
TITLE:
HARNESS WIRING DETAILS
SHEET 5 OF 5

TEES 2020

NO SCALE

A6–29





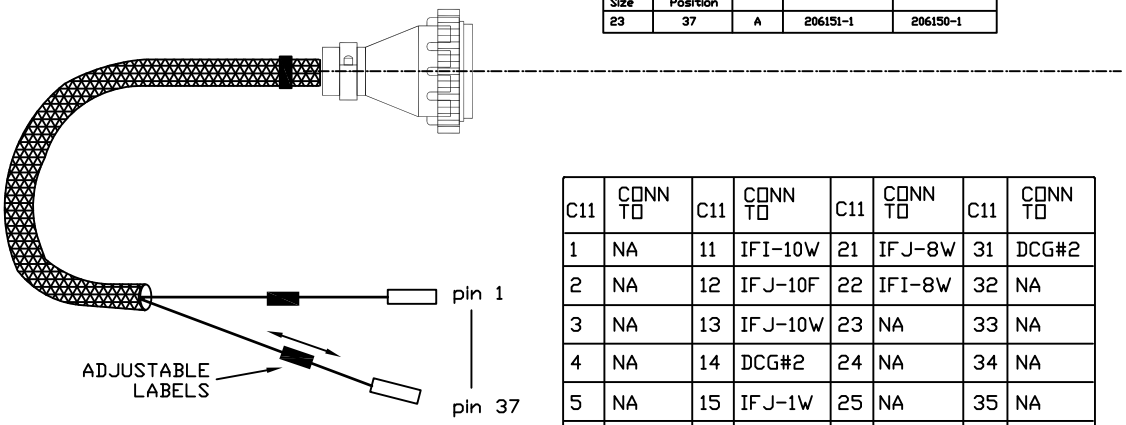
THERMOSTAT MOUNTING DETAILS

NOTE:
1. All dimensions are in inches

TITLE: FAN AND THERMOSTAT DETAILS	
	NO SCALE
TEES 2020	A6-30

C11P HARNESS

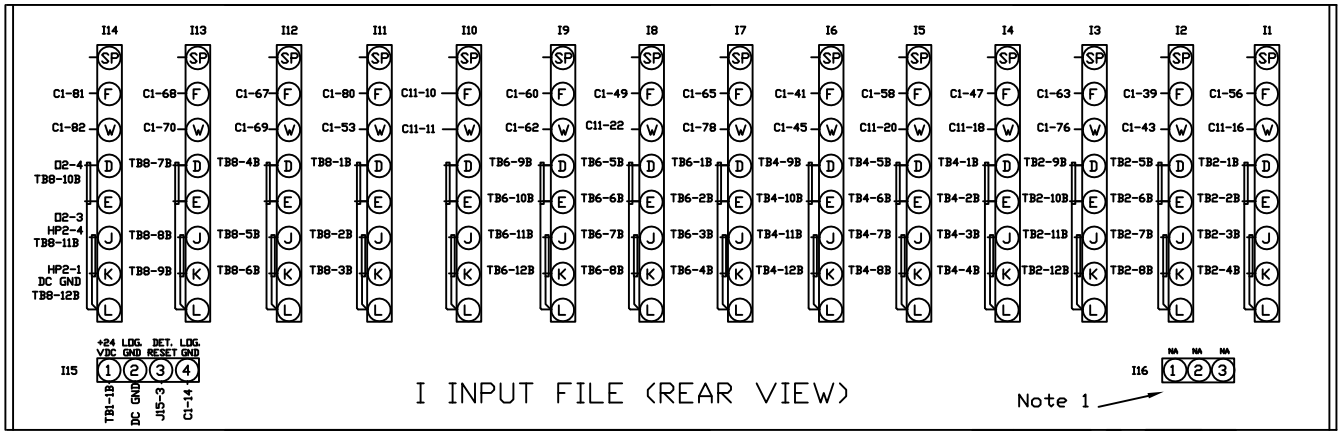
TYCO/AMP - Circular Plastic Connector (CPC)				
Shell Size	No. of Position	Key	Receptacle	Plug
23	37	A	206151-1	206150-1



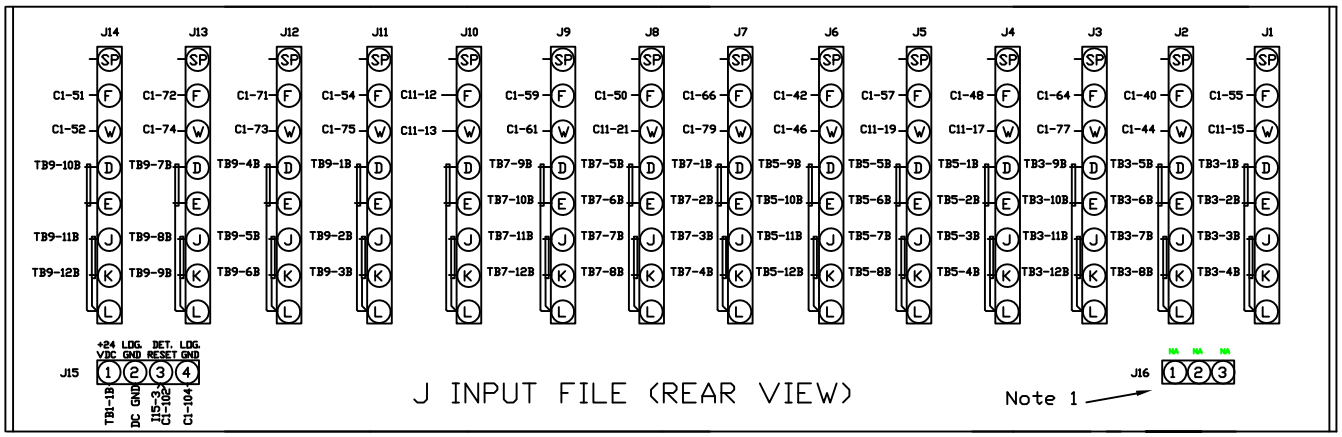
C11	CONN TO	C11	CONN TO	C11	CONN TO	C11	CONN TO
1	NA	11	IFI-10W	21	IFJ-8W	31	DCG#2
2	NA	12	IFJ-10F	22	IFI-8W	32	NA
3	NA	13	IFJ-10W	23	NA	33	NA
4	NA	14	DCG#2	24	NA	34	NA
5	NA	15	IFJ-1W	25	NA	35	NA
6	NA	16	IFI-1W	26	NA	36	NA
7	NA	17	IFJ-4W	27	NA	37	DCG#2
8	NA	18	IFI-4W	28	NA		
9	DCG#2	19	IFJ-5W	29	NA		
10	IFI-10F	20	IFI-5W	30	NA		

IFI-10F = INPUT FILE I, TERMINAL BLOCK 10, TERMINAL DESIGNATION F (CHANNEL 1 OUTPUT)
IFJ-10W = INPUT FILE J, TERMINAL BLOCK 10, TERMINAL DESIGNATION W (CHANNEL 2 OUTPUT)

2070-2E+
FI/O MODULE
REAR VIEW



I INPUT FILE (REAR VIEW)



J INPUT FILE (REAR VIEW)

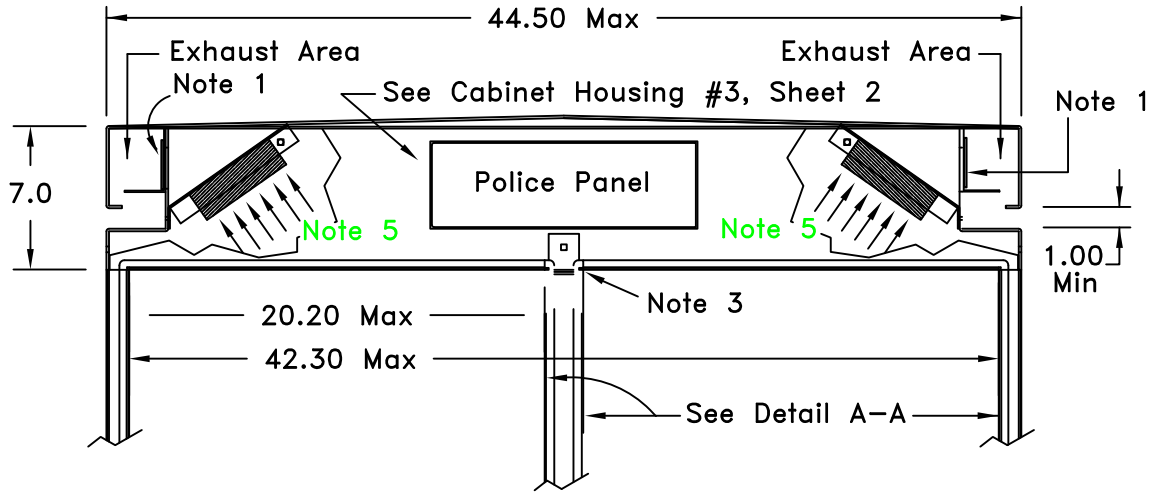
CALTRANS MODEL 33xLS, 34xLX CABINETS
I & J INPUT FILE

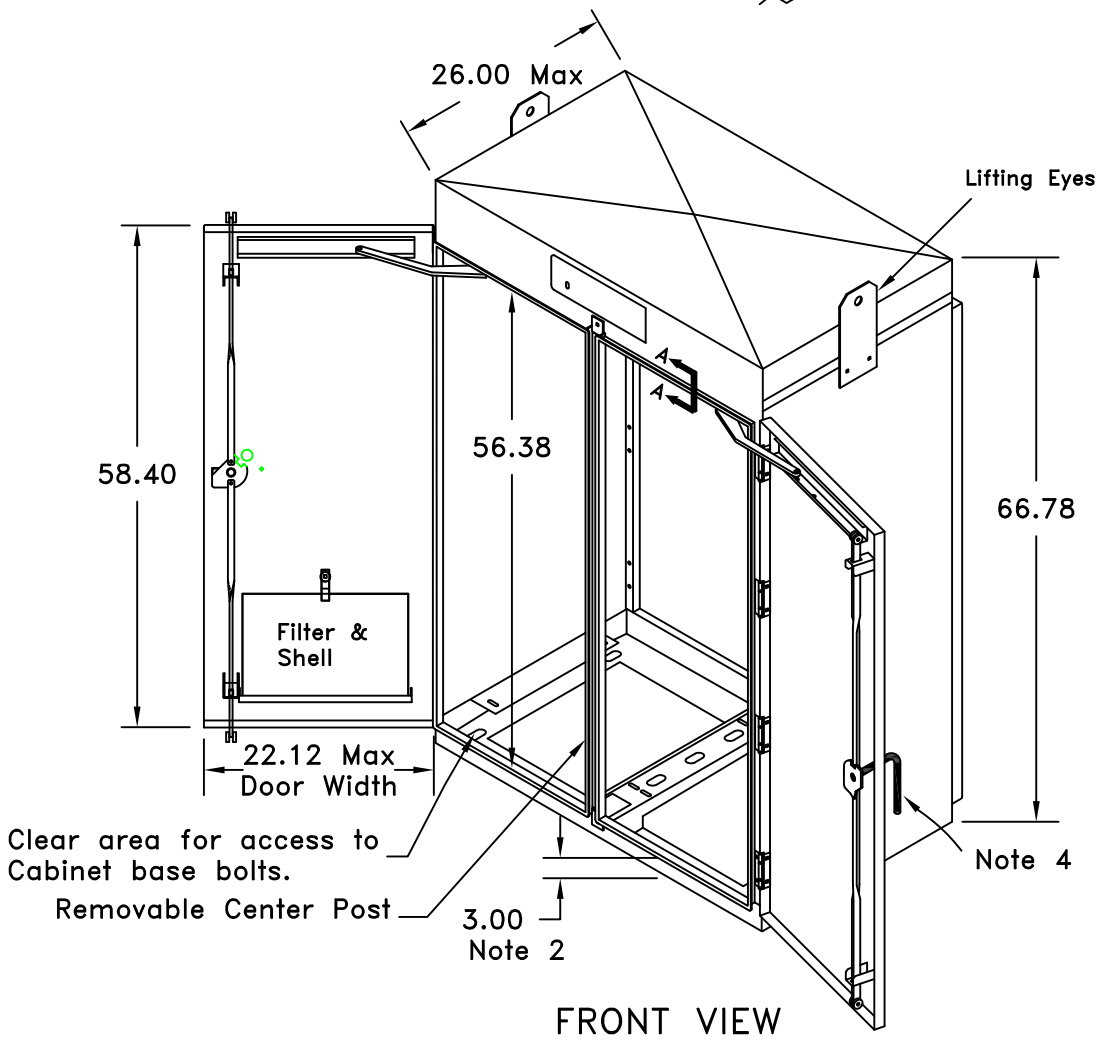
NOTE:

1. See A6-43 for details.
2. For C1S and C11S Pin Assignment, see A9-9.

TITLE: C11 HARNESS TERMINATION DETAIL	
	NO SCALE
TEES 2020	A6-31

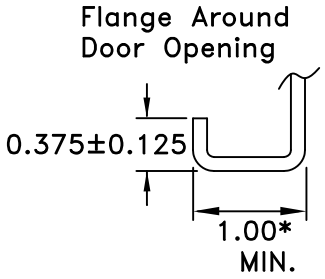
EXHAUST DETAIL





FRONT VIEW

SECTION A–A DETAIL



* TOLERANCE +0.0625 −0

NOTES:

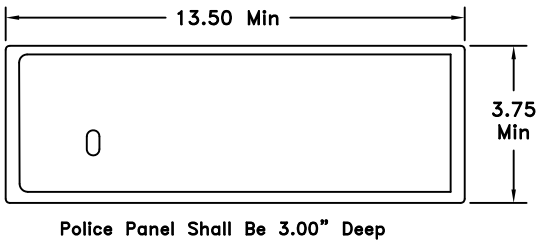
1. Perforated Screen
2. From Cabinet base to door lip
3. After center post is installed a sealant shall be applied to prevent leakage.
4. The handles shall be placed centered vertically on the doors opposite from the hinges on both, the rear & front.
5. Two fans each side.
6. All dimensions shown are in inches.

TITLE:

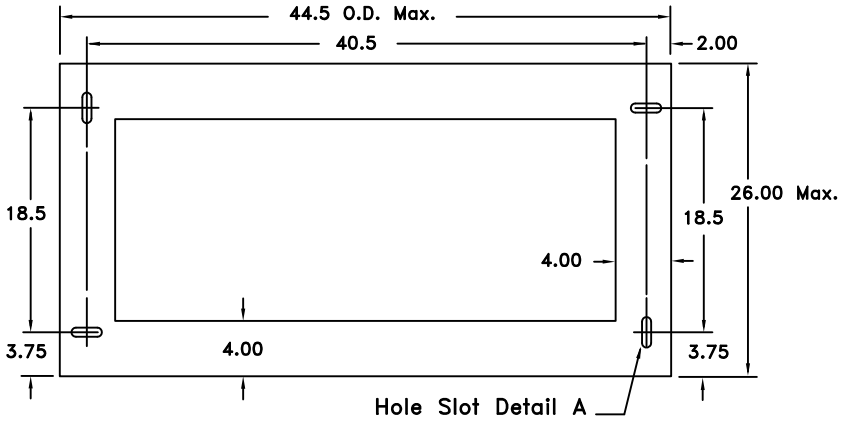
CABINET HOUSING #3 DETAILS
SHEET 1 OF 7

	NO SCALE
TEES 2020	A6–32

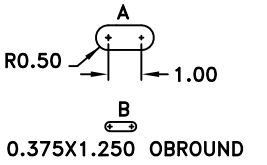
CABINET HOUSING #3 & #4 POLICE PANEL DETAIL



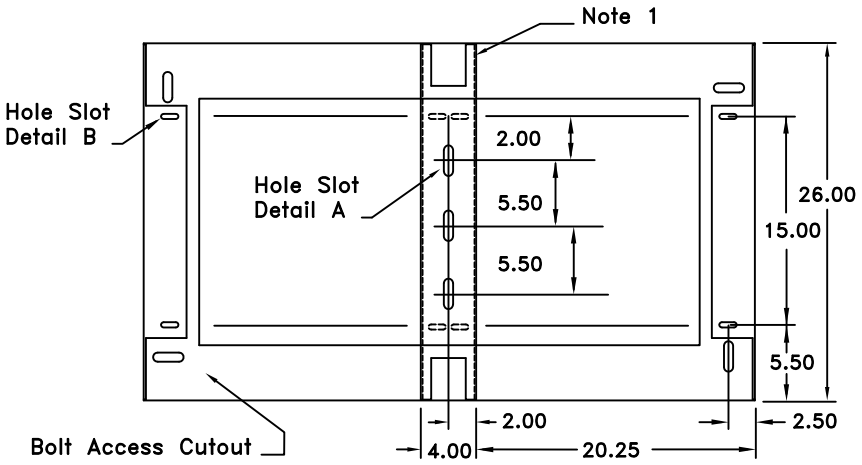
CABINET HOUSING #3 & #4 BOTTOM DETAIL



HOLE SLOT DETAIL



CAGE SUPPORT DETAIL

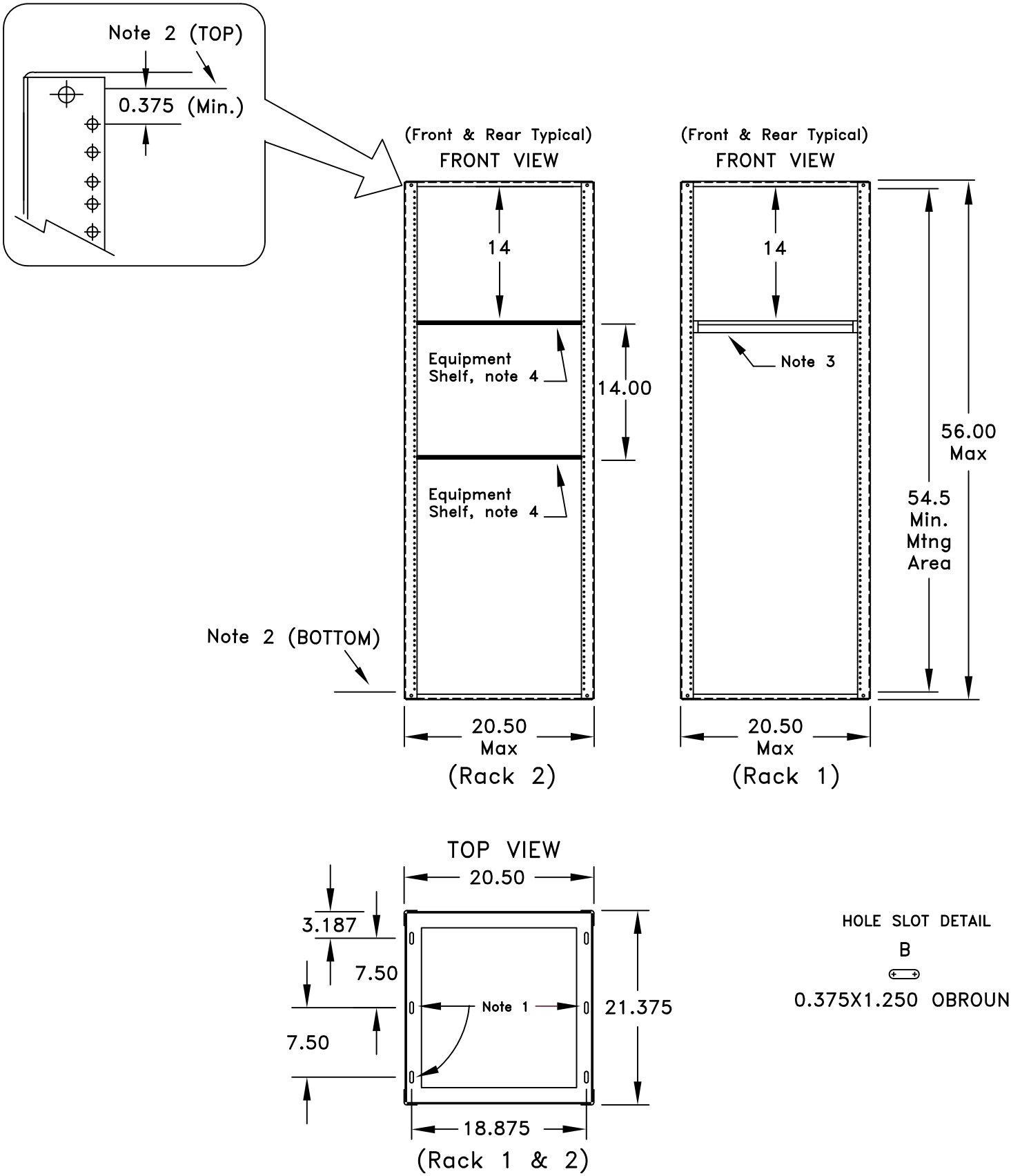


TOP VIEW

NOTES:

1. Tac Weld Cage Support to bottom assembly front and rear. See Cage Support Assembly Detail.
2. Uses Type LX Foundation.

TITLE: CABINET HOUSING #3 & #4 DETAILS SHEET 2 OF 7	
	NO SCALE
TEES 2020	A6-33



NOTES

1. Hole Slot Detail B, Cage #1 details A6–2.
2. TOP, Refers to the bottom lip of the top hat.
   BOTTOM, Refers to the top lip of the bottom hat.
3. Controller unit support drawer shelf assembly, A6–6.
4. Equipment shelf, A6–41.
5. All dimensions shown are in inches.

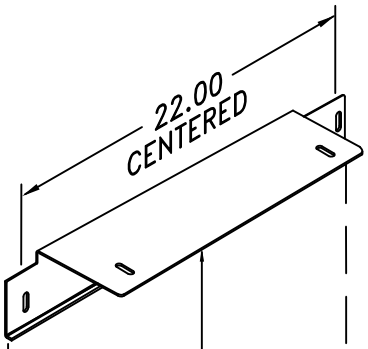
TITLE:

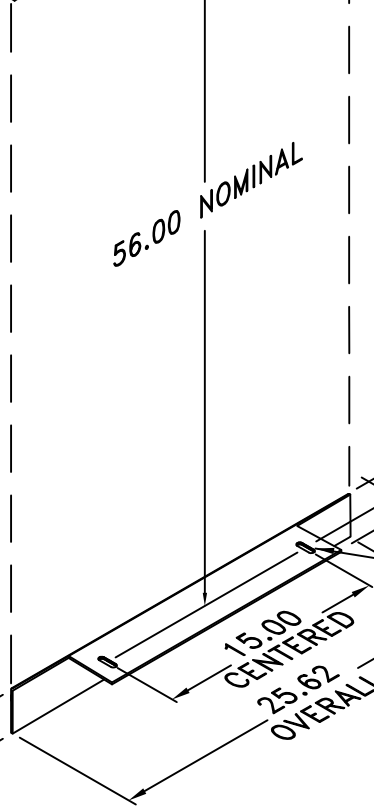
CABINET HOUSING #3 DETAILS
SHEET 3 OF 7

	NO SCALE
TEES 2020	A6–34

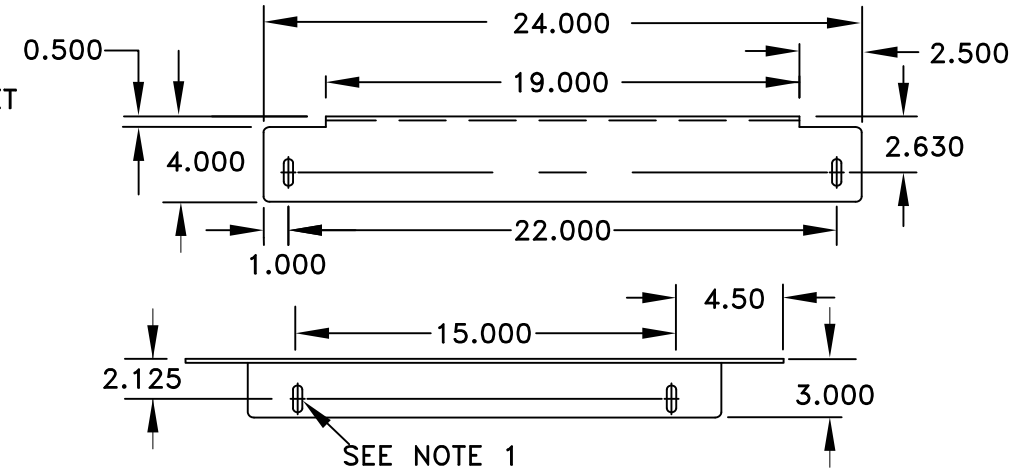
HOUSINGS 3 TO CAGE 1 SUPPORT DETAILS

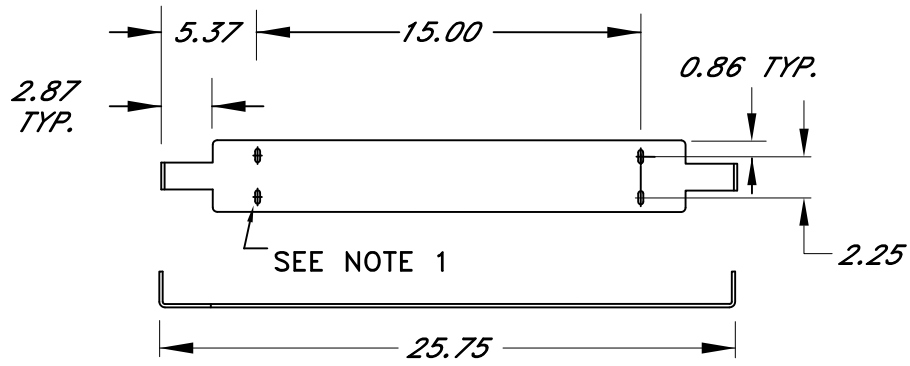
SPANNER BRACKET ATTACHED TO SIDE OF CABINET



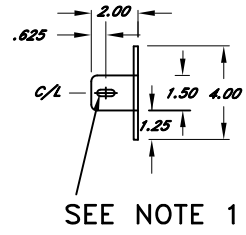


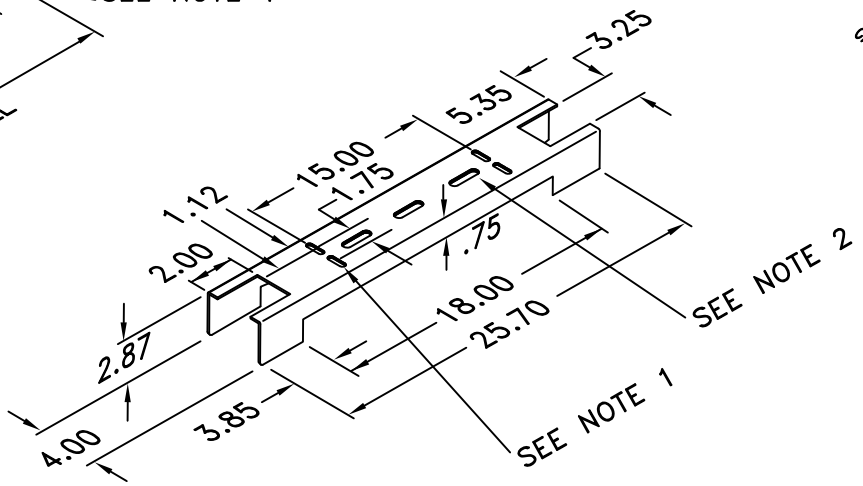
SPANNER BRACKET DETAIL





TOP RACK SUPPORT





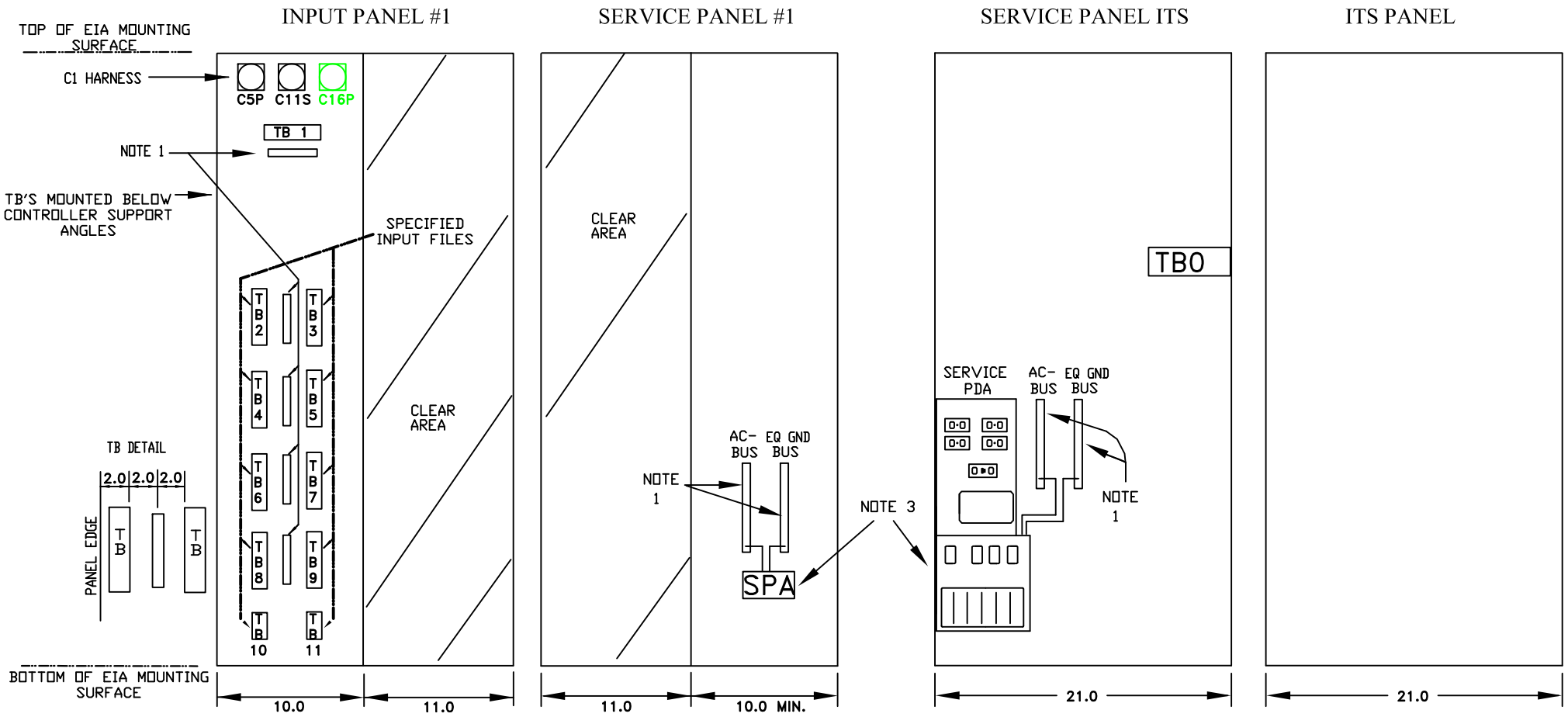
CENTER CHANNEL
PART IS WELDED TO BOTTOM PLATE

NOTES:

1. Hole Slot Detail B see Cabinet Housings 3 Detail 2
2. Hole Slot Detail A see Cabinet Housings 3 Detail 2
3. All dimensions shown are in inches.

TITLE: CABINET HOUSING #3 DETAILS SHEET 4 OF 7	
	NO SCALE
TEES 2020	A6–35

MODEL 342LX SIDE PANEL

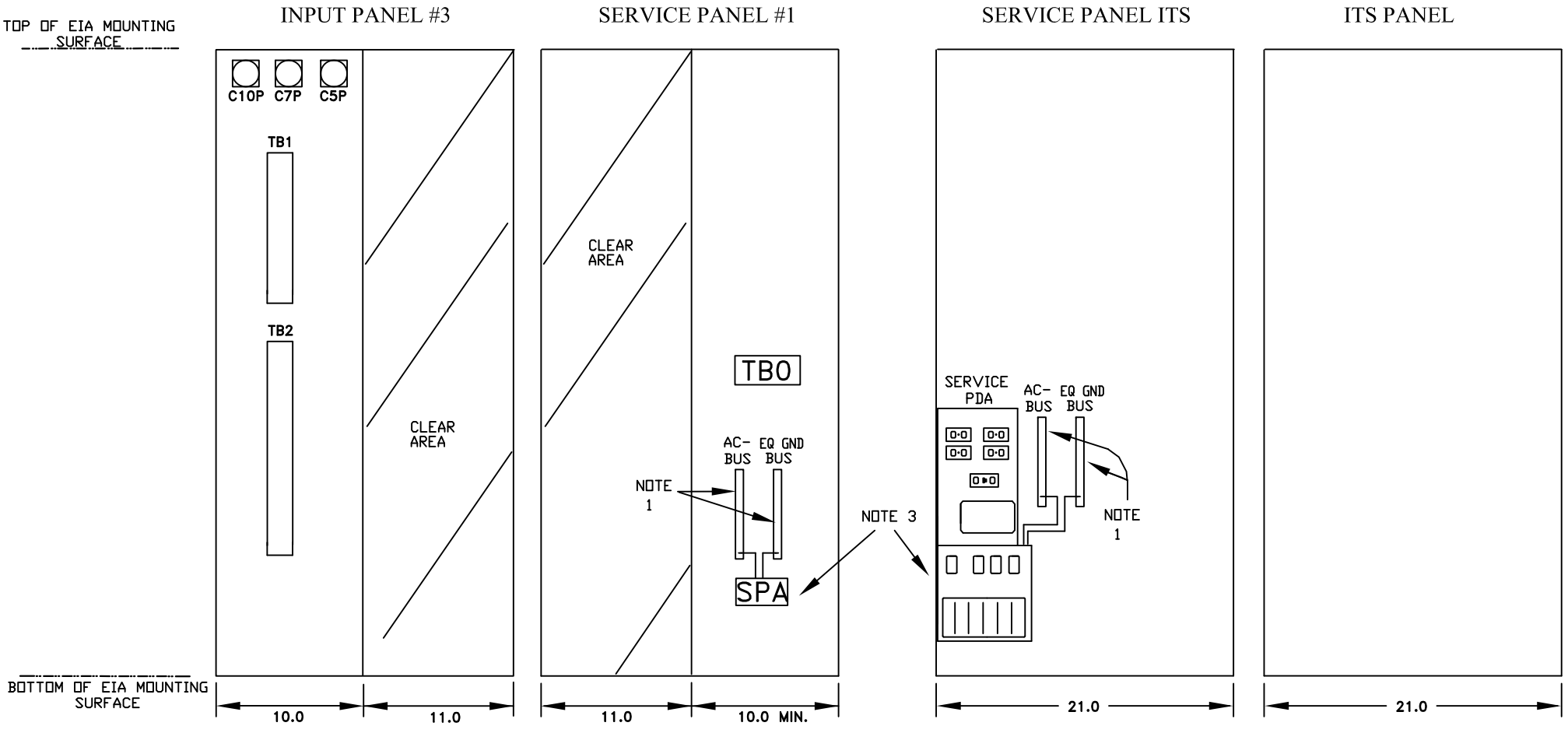


NOTES:

1. 10 terminal (#8 wire) minimum copper bus.
2. The terminal block shall have terminal positions necessary to match position assignments. Terminal position screws shall be 8–32 except for TBS, RTBO, TB3, which shall be 10–32
3. 4. SPA and the Service PDA shall be bolted on the Rail and firmly attached to the Service Panel.
4. All dimensions shown are in inches.

TITLE: MODEL 342LX SIDE PANEL DETAIL	
	NO SCALE
TEES 2020	A6-36

MODEL 344LX SIDE PANEL

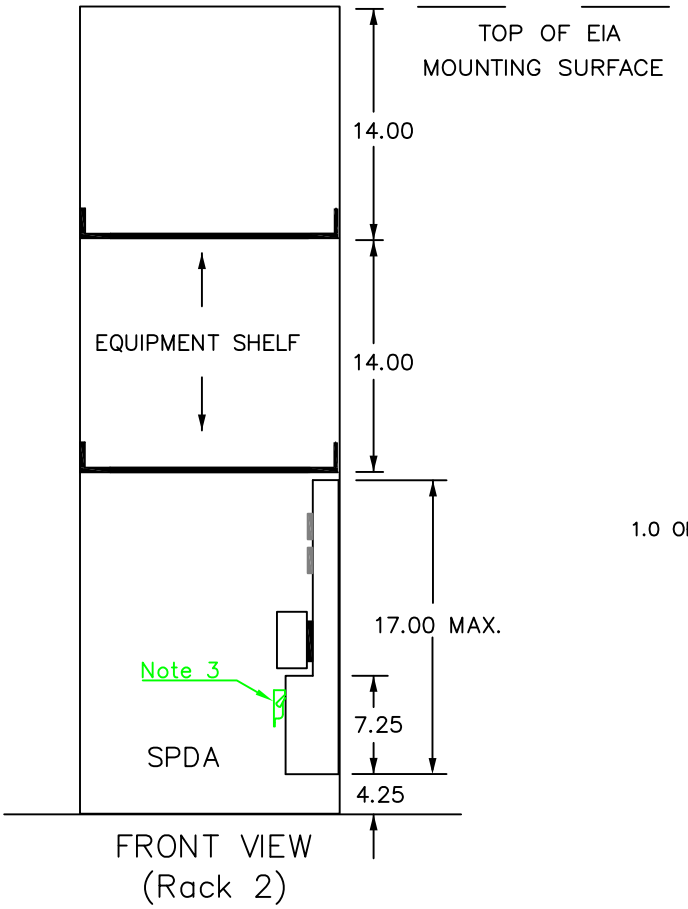


NOTES:

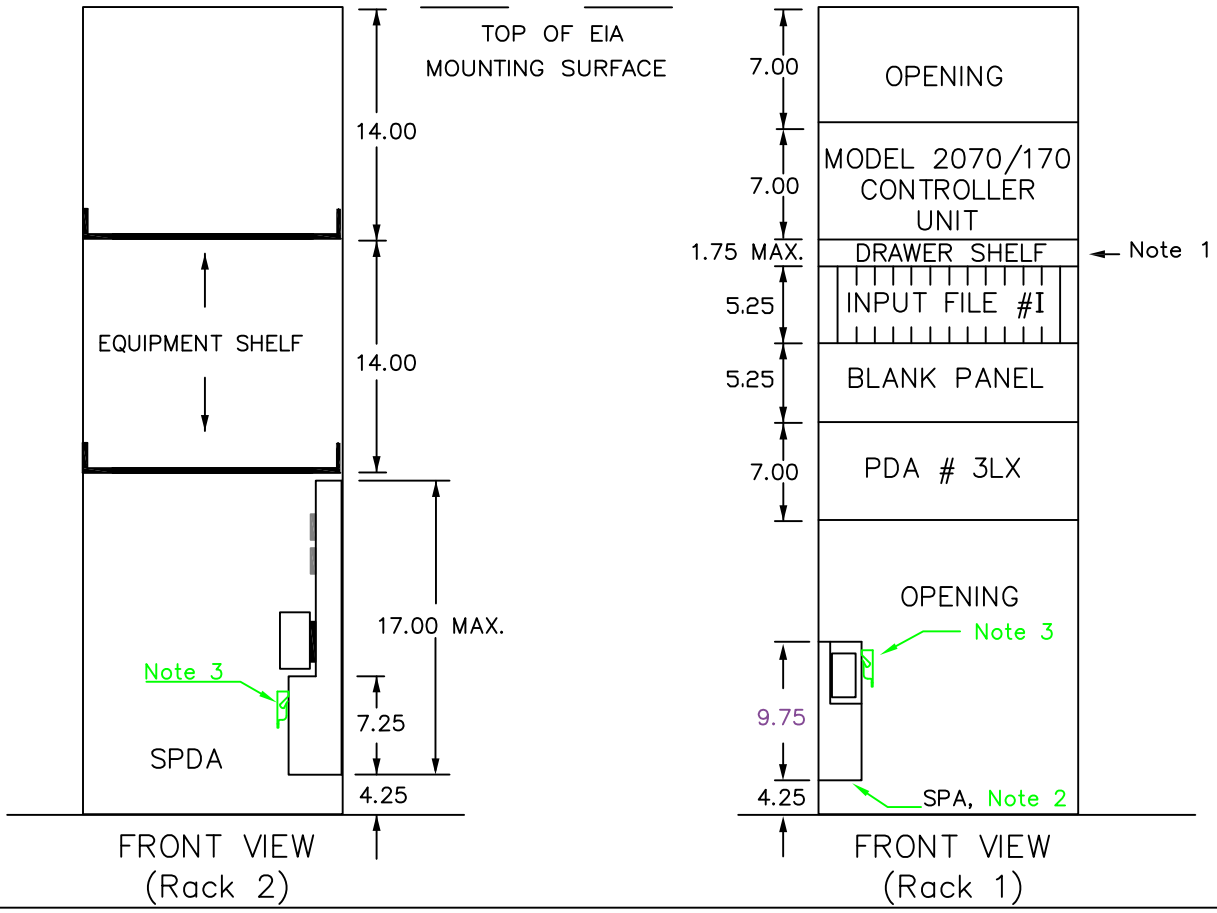
1. 10 terminal (#8 wire) minimum copper bus.
2. The terminal block shall have terminal positions necessary to match position assignments. Terminal position screws shall be 8–32 except for TBS, TBO, TB3, which shall be 10–32
3. SPA and the Service PDA shall be bolted on the Rail and firmly attached to the Service Panel.
4. All dimensions shown are in inches.

TITLE: MODEL 344LX SIDE PANEL DETAIL	
	NO SCALE
TEES 2020	A6-37

MODEL 342LX



MODEL 344LX



TITLE: CABINET EQUIPMENT MOUNTING DETAILS
SHEET 2 OF 3

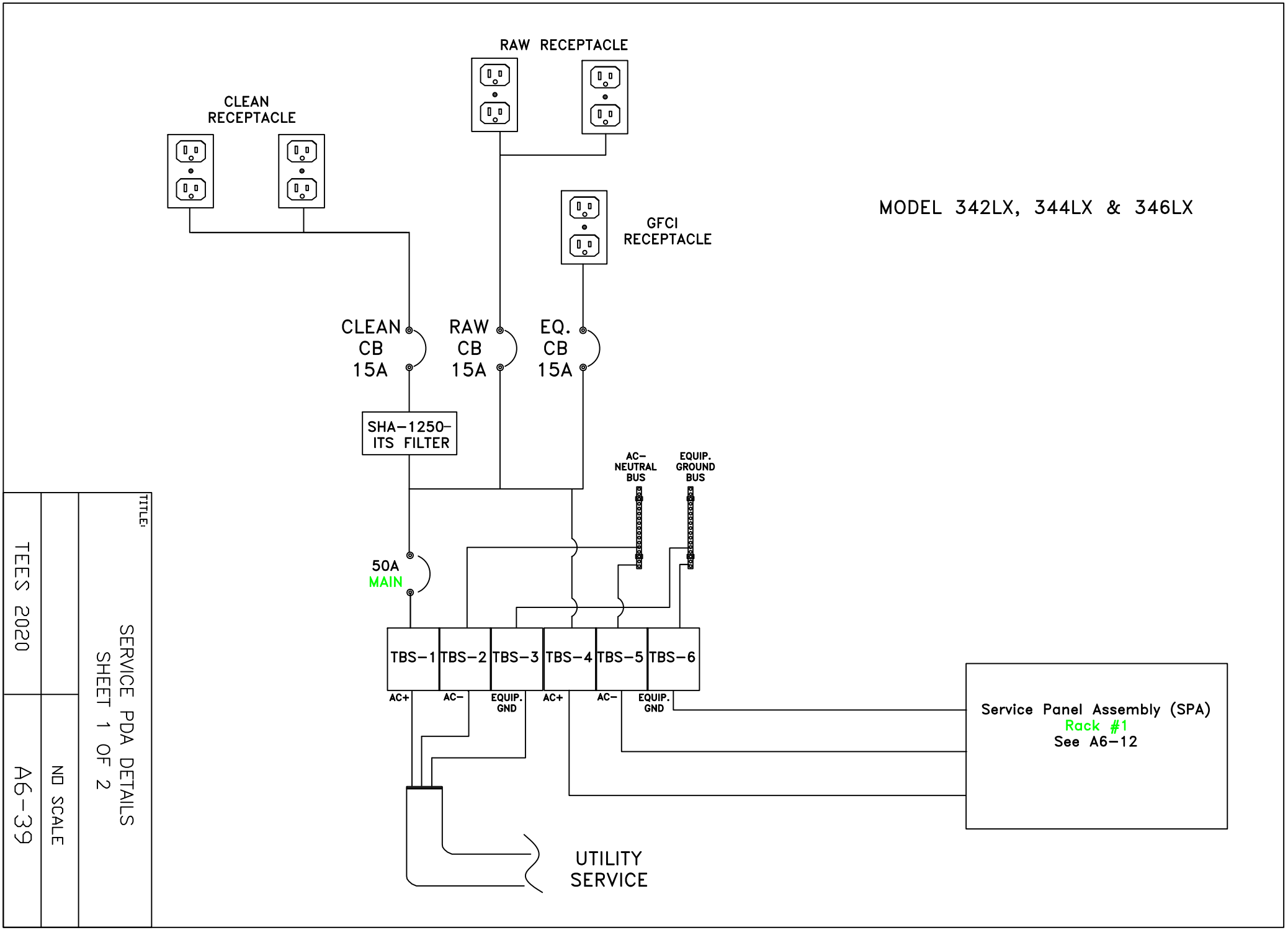
NO SCALE

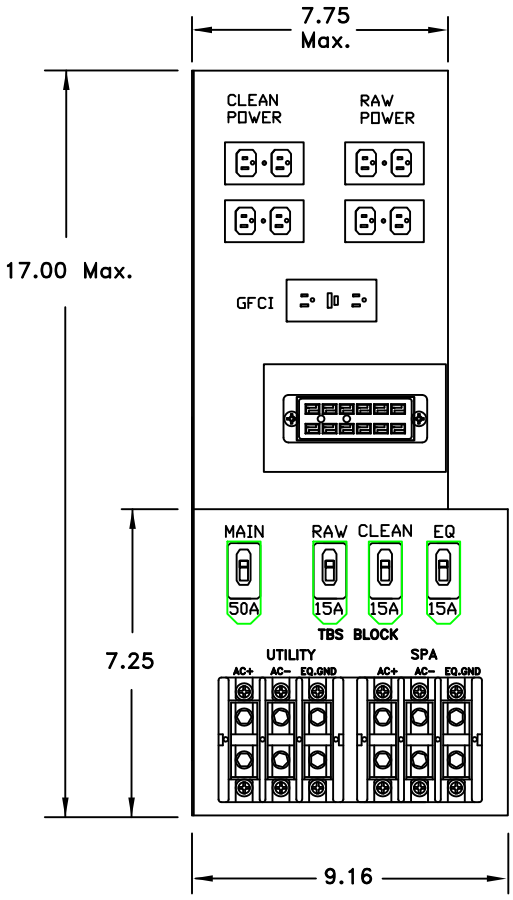
A6-38

TEES 2020

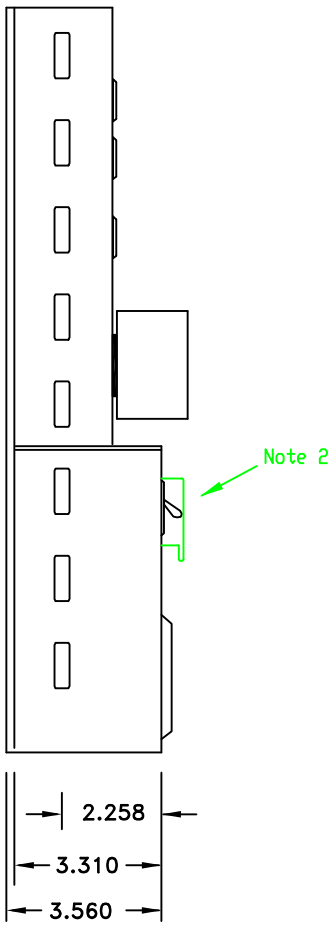
NOTE:

1. Controller unit support drawer shelf assembly.
2. SPA shall be bolted on the rail and firmly attached to the Service Panel.
3. Switch Guard, see A6-60.
4. All dimensions shown are in inches.


RAW RECEPTACLE
CLEAN RECEPTACLE
GFCI RECEPTACLE
MODEL 342LX, 344LX & 346LX
CLEAN CB 15A
RAW CB 15A
EQ. CB 15A
SHA-1250-ITS FILTER
AC- NEUTRAL BUS
EQUIP. GROUND BUS
50A MAIN
TBS-1
TBS-2
TBS-3
TBS-4
TBS-5
TBS-6
AC+
AC-
EQUIP. GND
AC+
AC-
EQUIP. GND
Service Panel Assembly (SPA)
Rack #1
See A6-12
UTILITY SERVICE
TITLE:
SERVICE PDA DETAILS
SHEET 1 OF 2
NO SCALE
TEES 2020
A6-39



REAR VIEW
(LEFT SIDE)



REAR VIEW

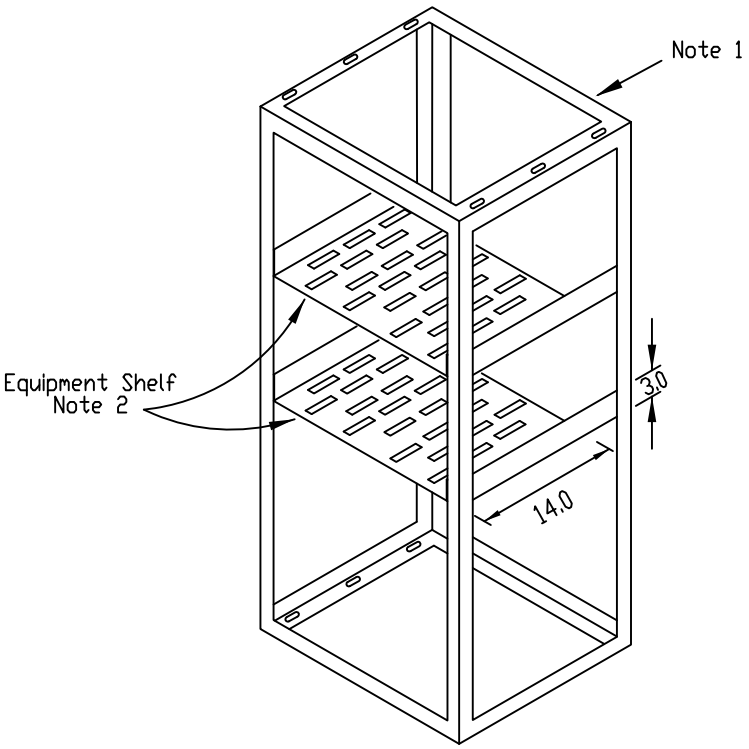
MODEL 342LX, 344LX & 346LX

NOTES:

1. The Service PDA shall be mounted at least 4.25in above the bottom of the LX cabinet.
2. Switch Guard, see A6-60.
3. All dimensions shown are in inches.

TITLE: SERVICE PDA DETAILS SHEET 2 OF 2	
	NO SCALE
TEES 2020	A6-40

Rack #2 EQUIPMENT SHELF INSTALLATION DETAILS
(FOR CABINET HOUSING #3)



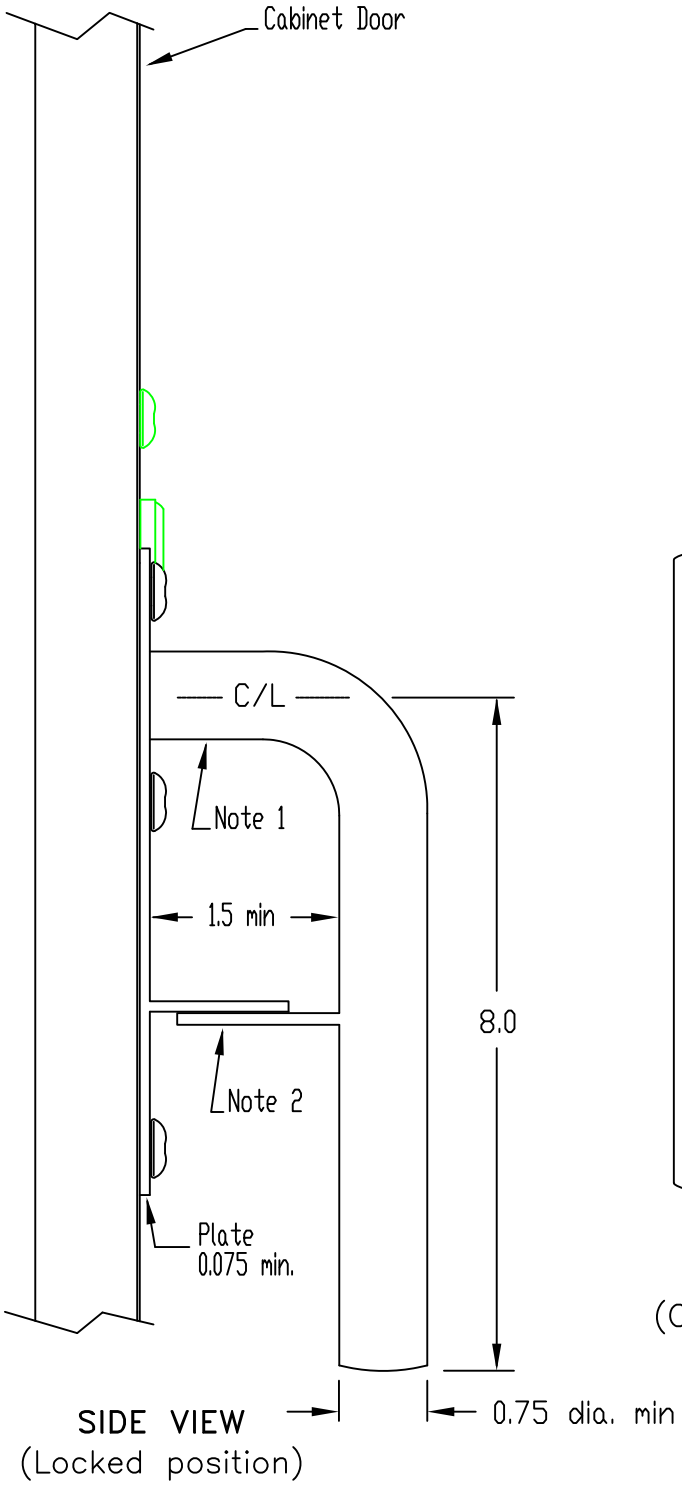
FRONT VIEW

NOTE:

1. Cabinet Housing #3 details, A6-32 & A6-34.
2. Equipment Shelf with Air Vents
3. All dimensions shown are in inches

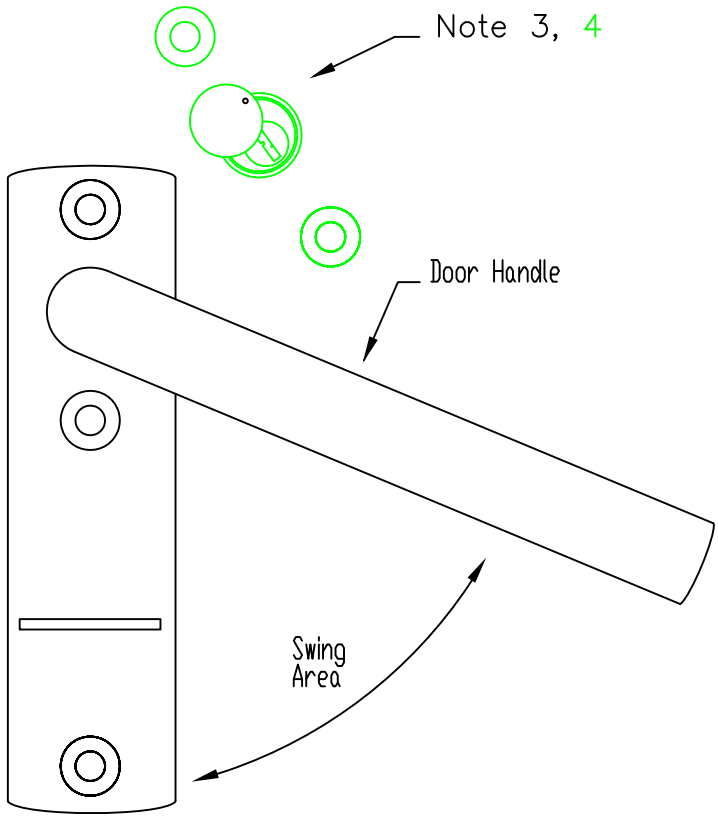
TITLE: RACK #2 EQUIPMENT SHELF INSTALLATION DETAILS	
	NO SCALE
TEES 2020	A6-41

HOUSING 1B, 2, 3 & 4 HANDLE DETAILS



SIDE VIEW
(Locked position)

LOCK DETAILS



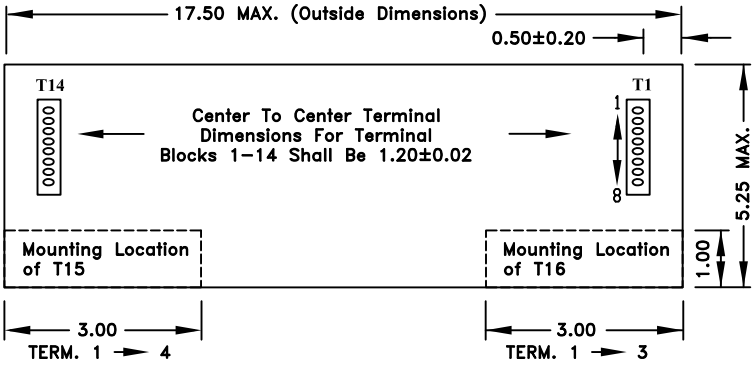
FRONT VIEW
(Open position)

NOTES:

1. Handle shank, 0.5 inch minimum
2. Provision for padlock, horizontal or verticle position.
3. Door lock, Corbin 2 Type or equal.
4. Door lock shall be above the the door handle to avoid key blocking the handle.
5. Door handle shall be Stainless Steel.
6. All dimensions shown are in inches.

TITLE: CABINET DOOR HANDLE DETAILS SHEET 1 OF 1	
	No Scale
TEES 2020	A6-42

INPUT FILE DETAIL



REAR VIEW

INPUT FILE TERMINAL ASSIGNMENT DETAIL

T1 - 14

TERM	PIN – FUNCTION
1	SP – SPARE
2	F – CHANNEL 1 OUTPUT
3	W – CHANNEL 2 OUTPUT
4	D – CHANNEL 1 INPUT
5	E – CHANNEL 1 INPUT
6	J – CHANNEL 2 INPUT
7	K – CHANNEL 2 INPUT
8	L – EQUIP. GROUND

T15

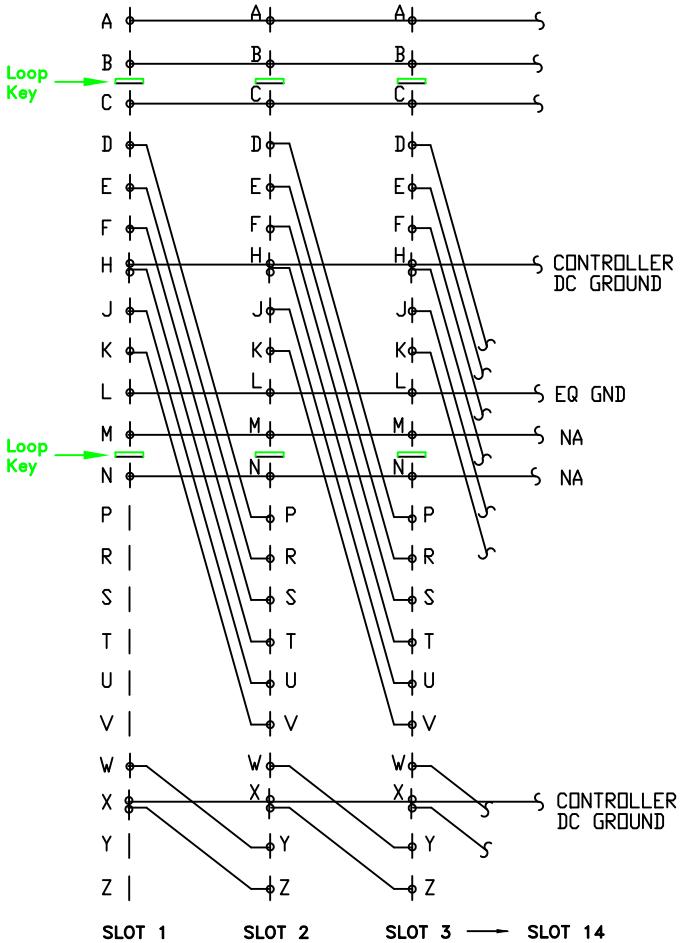
TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	DETECTOR RESET
4	C1 HARNESS DC GROUND

T16

TERM	FUNCTION
1	NA
2	NA
3	NA

INPUT FILE WIRING DIAGRAM

A	DC GROUND		
B	+24 VDC		
C	DETECTOR RESET		
D	LOOP No.1 MAGNETOMETER No.1		
E	LOOP No.1 MAGNETOMETER No.1		
F	LOOP No.1 MAGNETOMETER No.1	(COLLECTOR)	OUTPUT
H	LOOP No.1 MAGNETOMETER No.1	(EMITTER)	OUTPUT
J	LOOP No.2 MAGNETOMETER No.1		EXCITATION
K	LOOP No.2 MAGNETOMETER No.1		EXCITATION
L	CHASSIS GROUND		
M	NA		
N	NA		
P	LOOP No.3 MAGNETOMETER No.2		
R	LOOP No.3 MAGNETOMETER No.2		
S	LOOP No.3 MAGNETOMETER No.2	(COLLECTOR)	OUTPUT
T	LOOP No.3 MAGNETOMETER No.2	(EMITTER)	OUTPUT
U	LOOP No.4 MAGNETOMETER No.2		EXCITATION
V	LOOP No.4 MAGNETOMETER No.2		EXCITATION
W	LOOP No.2	(COLLECTOR)	OUTPUT
X	LOOP No.2	(EMITTER)	OUTPUT
Y	LOOP No.4	(COLLECTOR)	OUTPUT
Z	LOOP No.4	(EMITTER)	OUTPUT



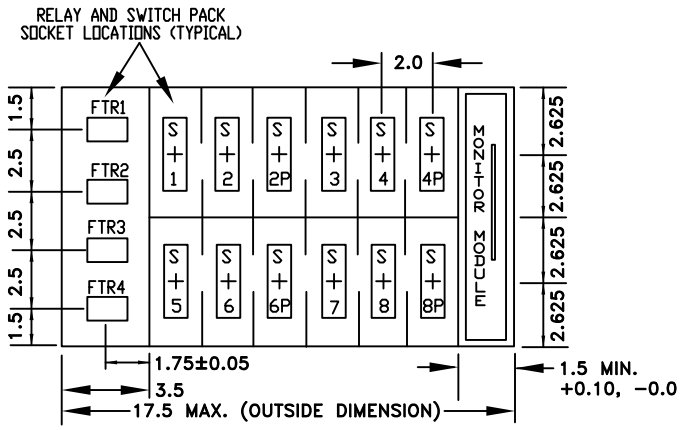
NOTE:
All dimensions shown are in inches.

TITLE:
INPUT/OUTPUT FILE LX DETAILS
SHEET 1 OF 13

NO SCALE

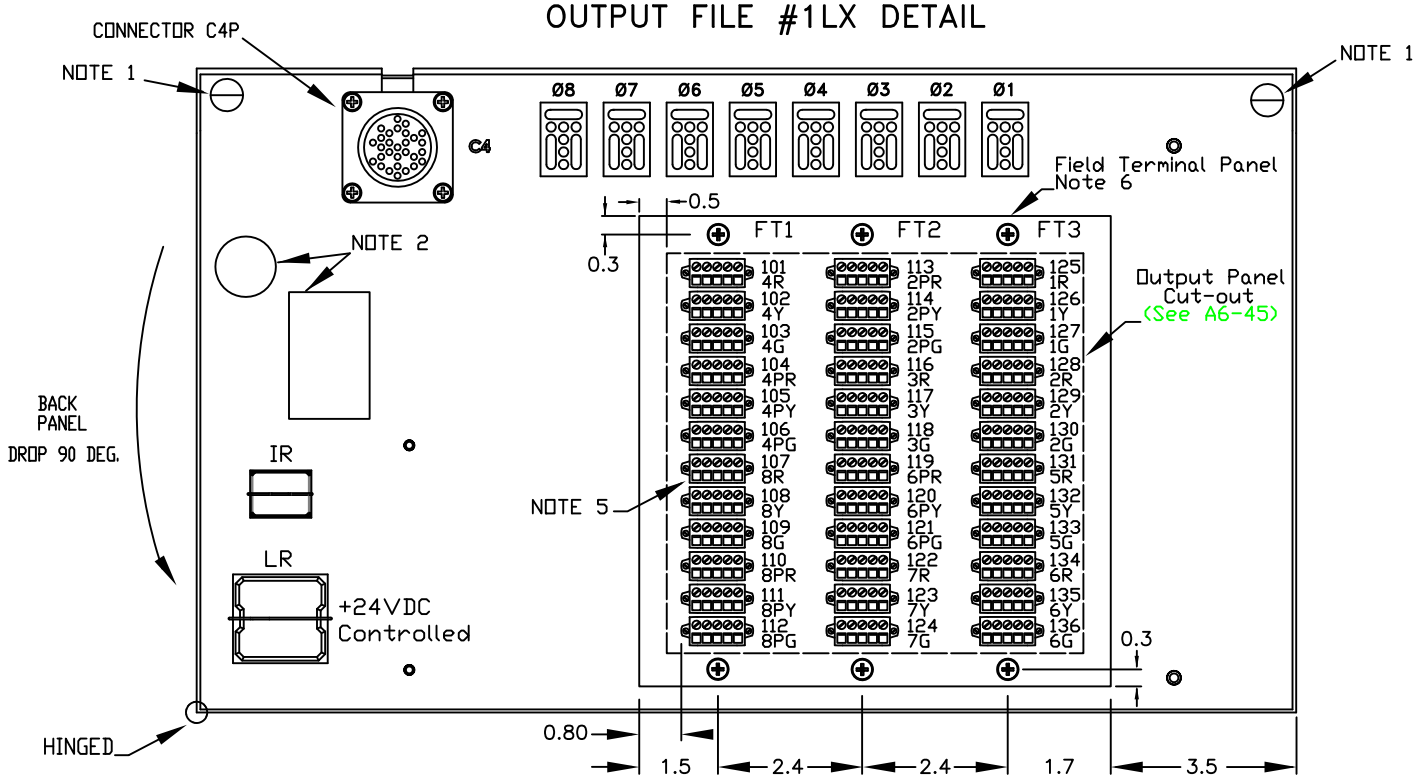
TEES 2020

A6-43



FRONT VIEW

OUTPUT FILE #1LX DETAIL



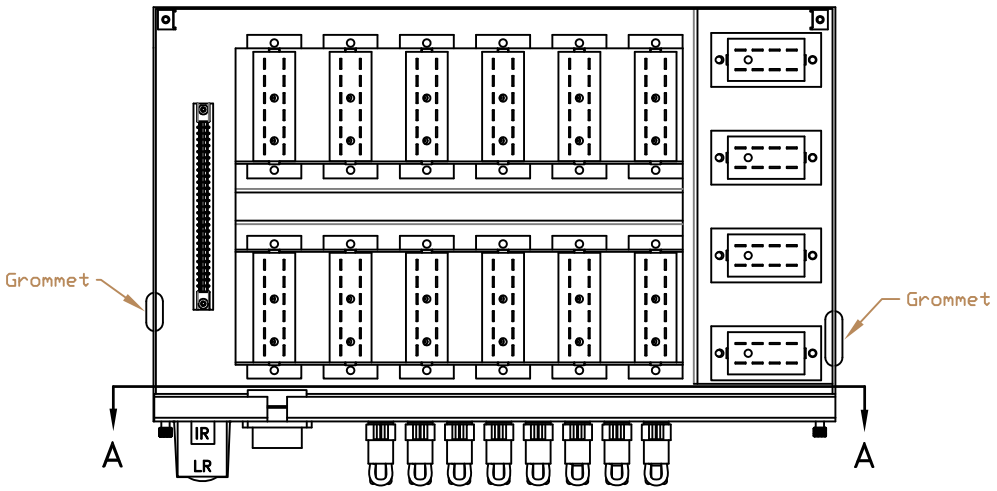
REAR VIEW

NOTE:

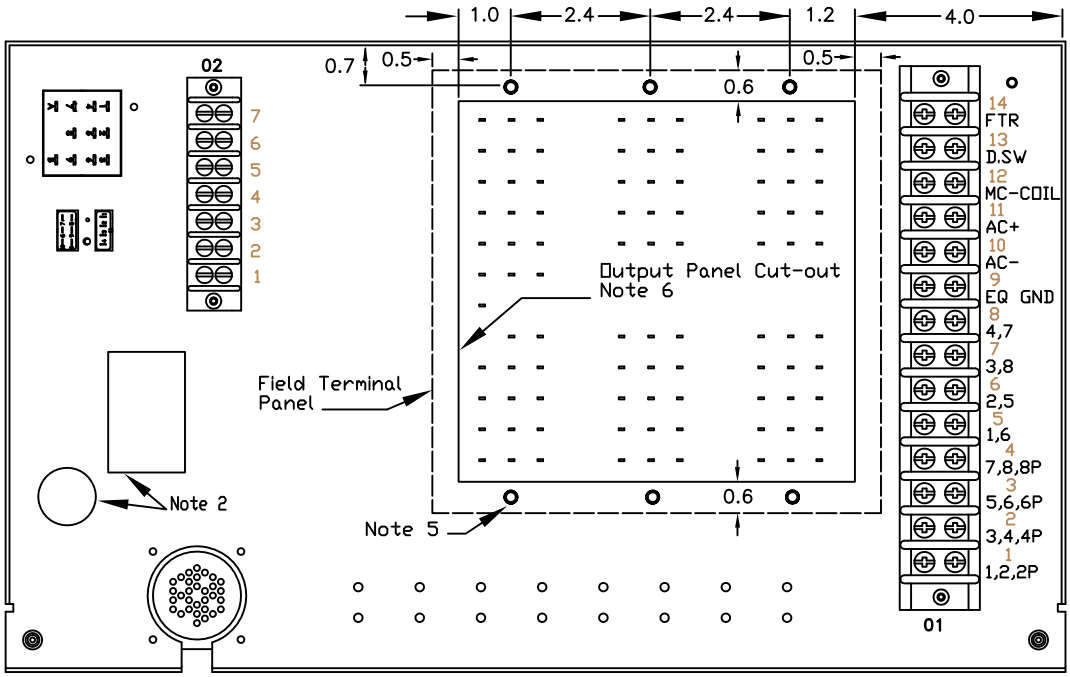
1. Thumb screws device
2. Panel stamped for OL Monitor Input Cable and Red Monitor Program Board, but Board not installed.
3. For Terminal Assignment, see Output File #1L detail.
4. See A6–50, A6–54 & A6–55 for sheets 8, 12 & 13.
5. Field Terminal contacts shall be 5–pin screw type Weidmuller BLT–C36, Phoenix Contact, or equivalent.
6. Height = 8.2 – 8.5, Width = 8
7. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE #1LX DETAILS SHEET 2 OF 13	
	NO SCALE
TEES 2020	A6–44

OUTPUT FILE #1LX DETAIL



REAR VIEW
(BACK PANEL - OPEN)



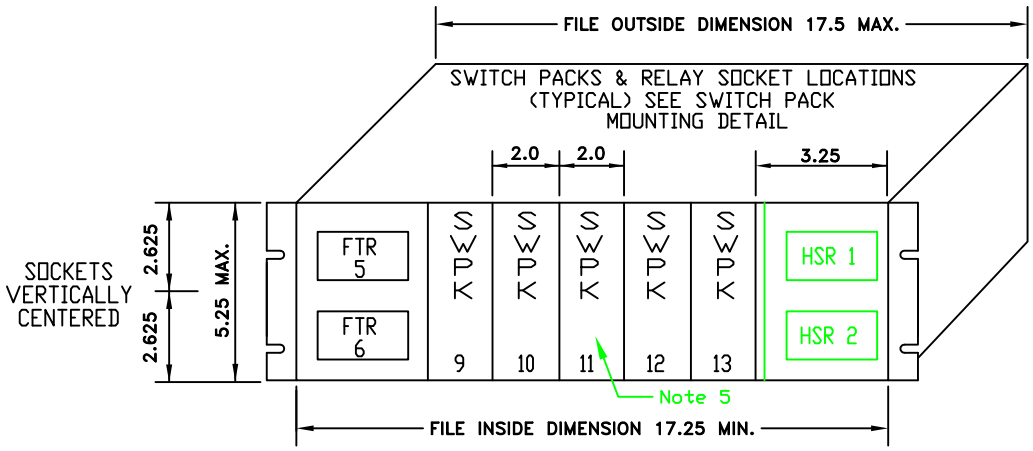
VIEW A-A

NOTE:

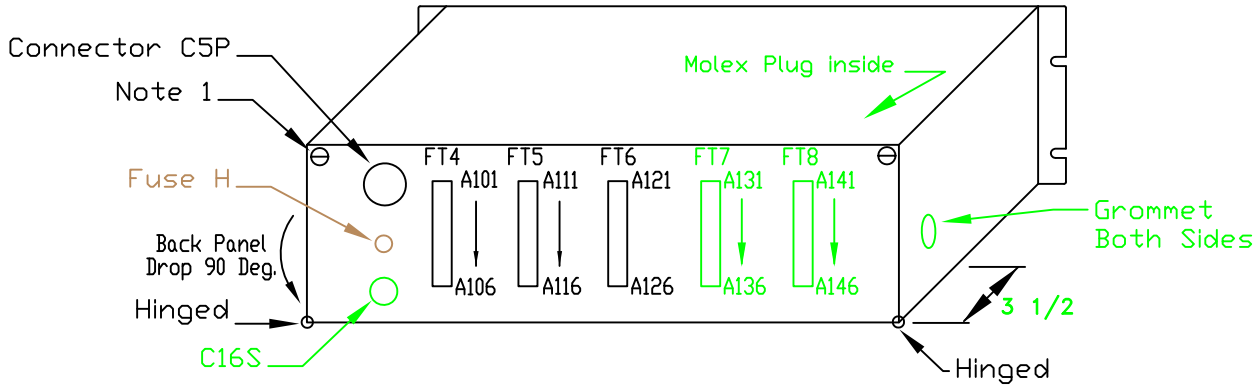
1. Thumb screws device
2. Panel stamped for OL Monitor Input Cable and Red Monitor Program Board, but board not installed.
3. For Terminal Assignment, see Output File #1 detail.
4. See A6-50, A6-54 & A6-55 for sheets 8, 12 & 13.
5. Holes 0.2 Dia. for Field Terminal Panel & Output Panels.
6. Cut-out Height = 7 - 7.3, Width = 7
7. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE #1LX DETAILS SHEET 3 OF 13	
	NO SCALE
TEES 2020	A6-45

MODEL #520 OUTPUT FILE #2LX DETAIL



FRONT VIEW



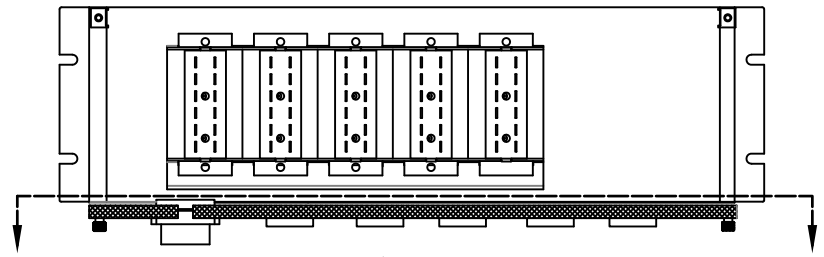
REAR VIEW
(BACK PANEL - CLOSED)

NOTE:

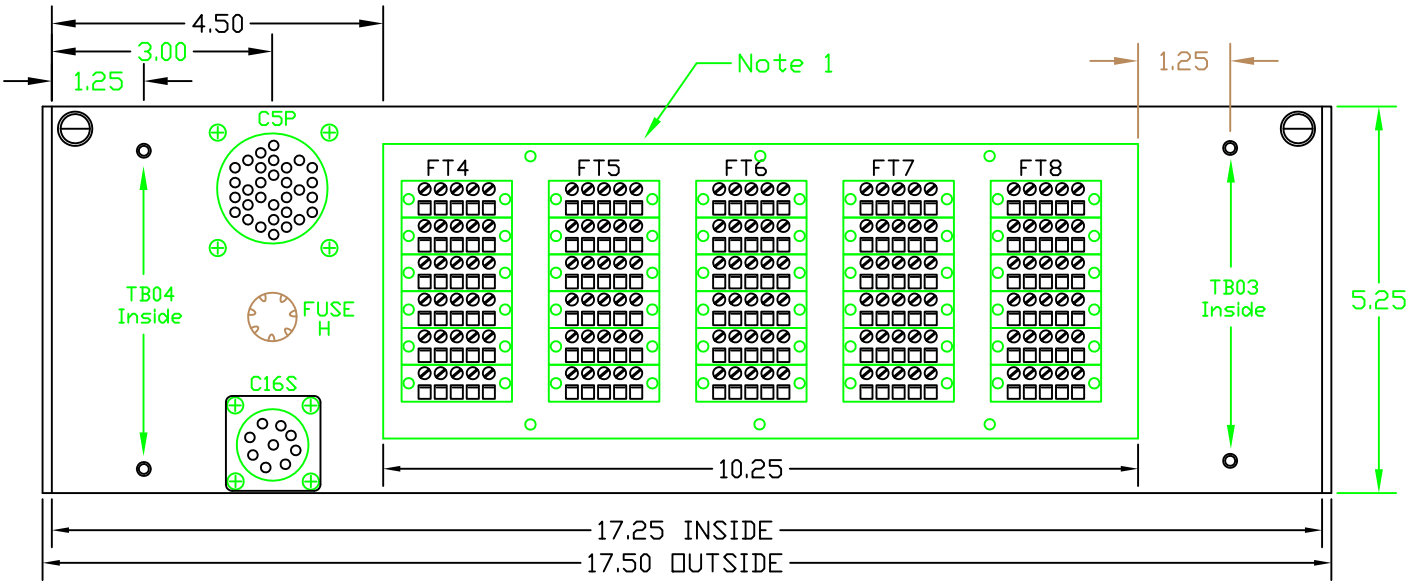
1. Thumb screws device
2. Back Panel Drop 90 Deg.
3. HSR=Health Status Relay,
4. For Terminal Assignment, see A6-51.
5. Health Status SWPK
6. Field Terminal contacts shall be 5-pin screw type, Weidmuller BLT-C18, Phoenix or equivalent.
7. TB03 and TB04 are inside the back panel.
8. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE #2LX DETAILS SHEET 4 OF 13	
	NO SCALE
TEES 2020	A6-46

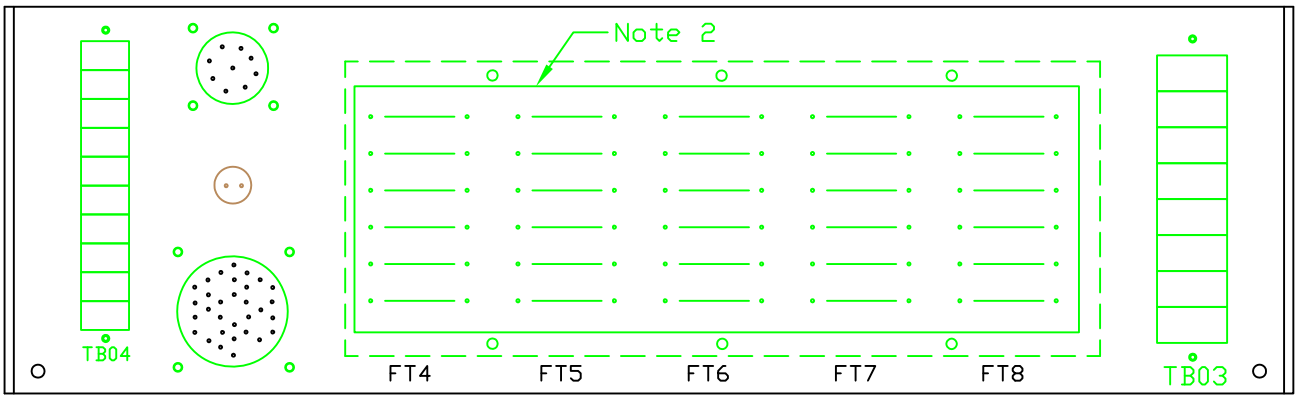
MODEL #520 OUTPUT FILE #2LX DETAILS



REAR VIEW
(BACK PANEL - OPEN)



REAR VIEW
(BACK PANEL CLOSED)



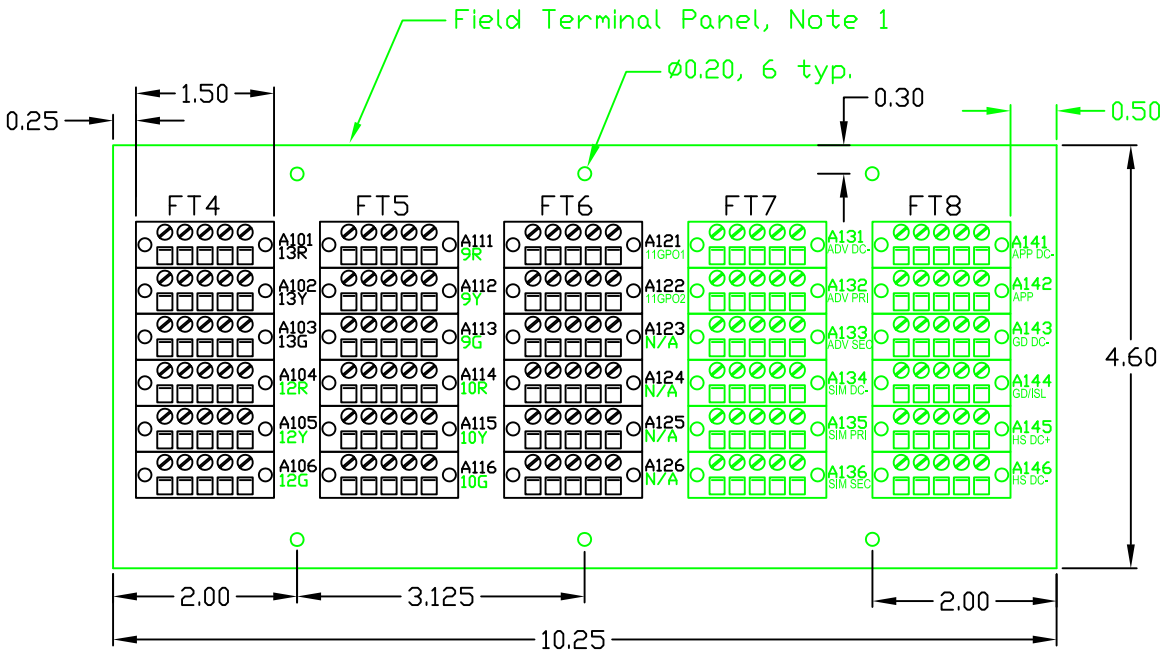
REAR VIEW A-A
(BACK PANEL)

NOTE: (This sheet only)

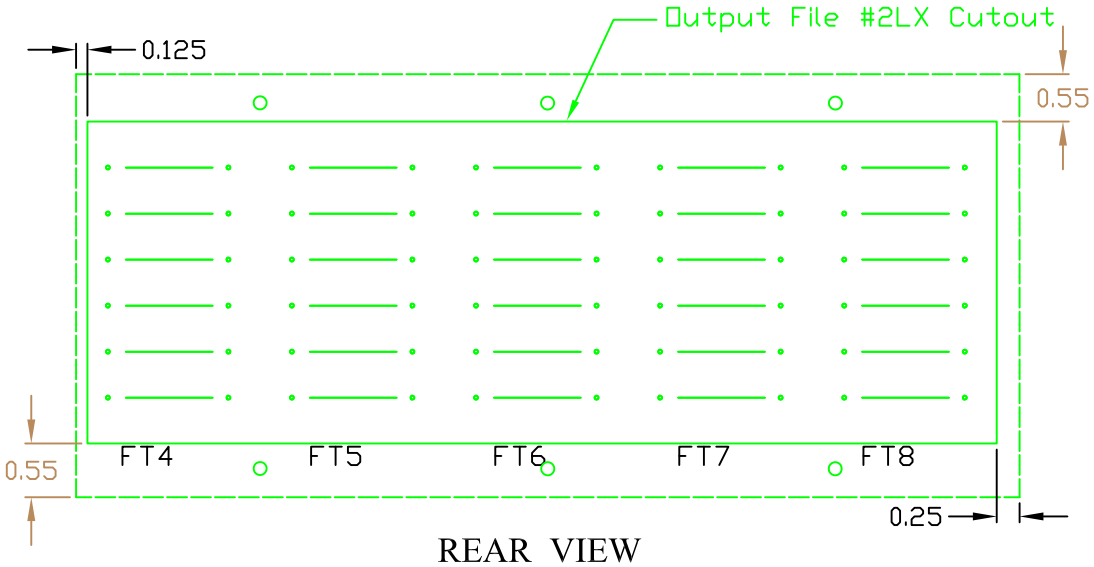
1. Field Terminal Panel, see A6-48 for details.
2. Panel cutout, see A6-48 for details.
3. All fuses shall be 0.5 Amps.
4. For Terminal Assignment, see A6-51.
5. TB03 and TB04 are inside the back panel.
6. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE #2LX DETAILS SHEET 5 OF 13	
	NO SCALE
TEES 2020	A6-47

MODEL #520 OUTPUT FILE #2LX
(FTP-2LXR)



REAR VIEW



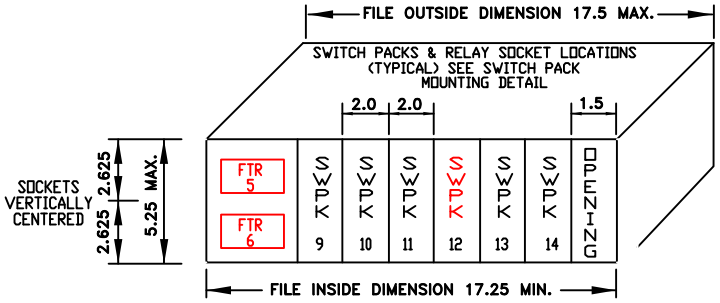
REAR VIEW
(INSIDE BACK PANEL)

NOTE: (This sheet only)

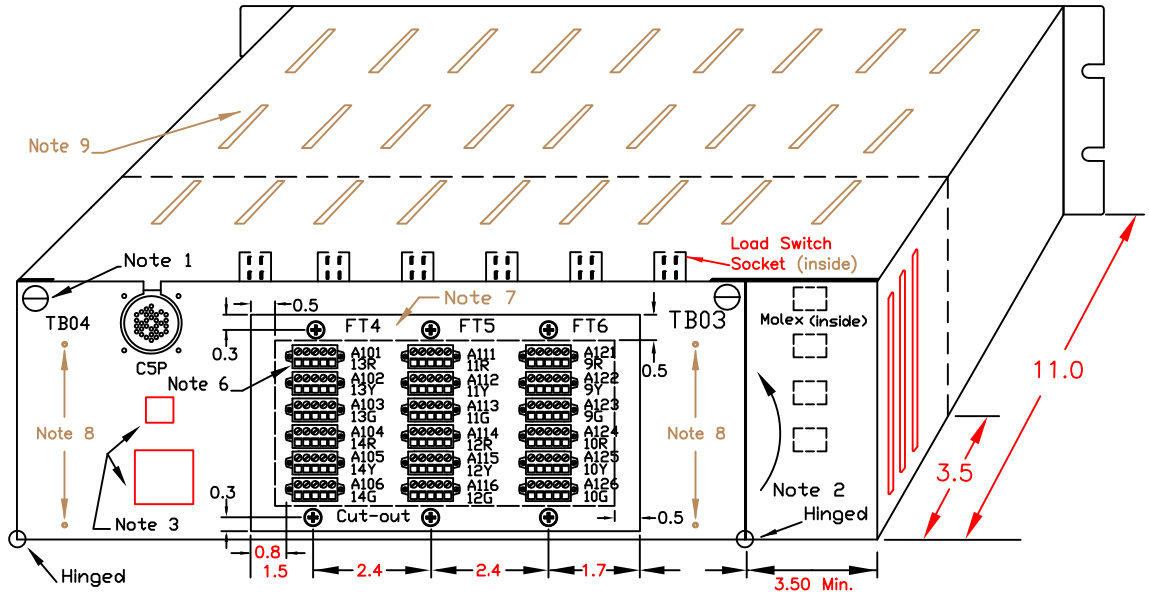
1. Field Terminal Panel (FTP-2LXR)
   Height=4.6 – 4.8, Width=10.25
2. For Terminal Assignment, see A6-51.
3. Field Terminal contacts shall be 5-pin screw type, Weidmuller BLT-C18, Phoenix or equivalent.
4. 11GPO1 = General Purpose Output #1
   11GPO2 = General Purpose Output #2
5. All dimensions shown are in inches.

TITLE: INPUT/OUTPUT FILE #2LX DETAILS SHEET 6 OF 13	
	NO SCALE
TEES 2020	A6-48

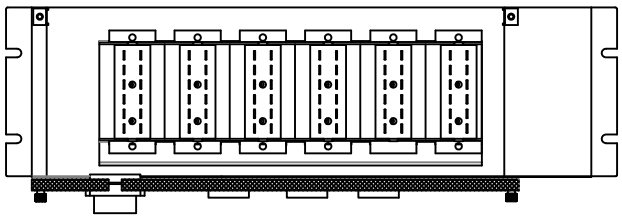
MODEL #420 OUTPUT FILE #2LX DETAIL
(AUX. FILE)



FRONT VIEW



REAR VIEW
(BACK PANEL - CLOSED)



REAR VIEW
(BACK PANEL - OPEN)

NOTE:

1. Thumb screws device
2. Back Panel Drop 90 Deg.
3. Panel stamped for IR & LR relay sockets, but relays not installed
4. For Terminal Assignment, see Output File #2LX detail.
5. See A6–50 for sheet 8.
6. Field Terminal contacts shall be 5–pin screw type, Weidmuller BLT–C18, Phoenix or equivalent.
7. Field Terminal Panel (FTP–2LX), Height = 4.6 – 4.8, Width = 8.0
8. TB03 inside the back panel.
9. Perforation on top and bottom.
10. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE #2LX DETAILS SHEET 7 OF 13	
	NO SCALE
TEES 2020	A6–49

OUTPUT FILE #1LX TERMINAL ASSIGNMENT DETAIL

01 TERM	FUNCTION
1	PDA CKT1/SWPKS 1,2,2P-1
2	PDA CKT2/SWPKS 3,4,4P-1
3	PDA CKT3/SWPKS 5,6,6P-1
4	PDA CKT4/SWPKS 7,8,8P-1
5	PDA FU1 CKT1/FTR1
6	PDA FU1 CKT2/FTR2
7	PDA FU2 CKT1/FTR3
8	PDA FU2 CKT2/FTR4
9	EQUIP. GROUND
10	AC-
11	AC+ (FROM PDA)
12	SSR (TO PDA)
13	DOOR SW. (FROM POL PAN)
14	FTR COILS (TO)

02 TERM	FUNCTION
1	+24VDC TO LOGIC RELAY (LR) COIL
2	DC GROUND
3	IFI-14J, STOP TIME (FROM M.U)
4	IFI-14D, FLASH SENSE (FROM I.R)
5	EXTERNAL (M.U) RESET
6	NA
7	+24VDC (CONTROLLED) TO SWITCHPACKS (1-12) POSITION 9

FT1 TERM	FUNCTION
101	SWPK 4-RED
102	SWPK 4-YEL
103	SWPK 4-GRN
104	SWPK 4P-RED
105	SWPK 4P-YEL
106	SWPK 4P-GRN
107	SWPK 8-RED
108	SWPK 8-YEL
109	SWPK 8-GRN
110	SWPK 8P-RED
111	SWPK 8P-YEL
112	SWPK 8P-GRN

FT2 TERM	FUNCTION
113	SWPK 2P-RED
114	SWPK 2P-YEL
115	SWPK 2P-GRN
116	SWPK 3-RED
117	SWPK 3-YEL
118	SWPK 3-GRN
119	SWPK 6P-RED
120	SWPK 6P-YEL
121	SWPK 6P-GRN
122	SWPK 7-RED
123	SWPK 7-YEL
124	SWPK 7-GRN

FT3 TERM	FUNCTION
125	SWPK 1-RED
126	SWPK 1-YEL
127	SWPK 1-GRN
128	SWPK 2-RED
129	SWPK 2-YEL
130	SWPK 2-GRN
131	SWPK 5-RED
132	SWPK 5-YEL
133	SWPK 5-GRN
134	SWPK 6-RED
135	SWPK 6-YEL
136	SWPK 6-GRN

Model #420. OUTPUT FILE #2LX TERMINAL ASSIGNMENT DETAIL

O3 TERM	FUNCTION
1	PDA FU1 CKT1/FTR5
2	PDA FU2 CKT2/FTR6
3	FTR COILS (TO)
4	AC-
5	PDA CKT5/SWPKS 9,10,11-1
6	PDA CKT6/SWPKS 12,13,14-1
7	EQUIP. GROUND
8	AC+ (FROM PDA)

O4 TERM	FUNCTION
1	+24VDC
2	DC GROUND
3	IFI-14J, STOP TIME (FROM M.U)
4	IFI-14D, FLASH SENSE (FROM I.R)
5	EXTERNAL (M.U) RESET
6	WDT INPUT
7	LR COIL (UNIT IN)
8	SSR (PDA)

FT4 TERM	FUNCTION	FT5 TERM	FUNCTION	FT6 TERM	FUNCTION
A101	SWPK 13-RED	A111	SWPK 11-RED	A121	SWPK 9-RED
A102	SWPK 13-YEL	A112	SWPK 11-YEL	A122	SWPK 9-YEL
A103	SWPK 13-GRN	A113	SWPK 11-GRN	A123	SWPK 9-GRN
A104	SWPK 14-RED	A114	SWPK 12-RED	A124	SWPK 10-RED
A105	SWPK 14-YEL	A115	SWPK 12-YEL	A125	SWPK 10-YEL
A106	SWPK 14-GRN	A116	SWPK 12-GRN	A126	SWPK 10-GRN

NOTE:

1. Thumb screws device.
2. All dimensions shown are in inches.

TITLE:

INPUT/OUTPUT FILE DETAILS

SHEET 8 OF 13

NO SCALE

TEES 2020

A6-50

MODEL #520. OUTPUT FILE #2LX TERMINAL ASSIGNMENT DETAIL

O3 TERM	FUNCTION
1	PDA FU1 CKT1/FTR5
2	PDA FU2 CKT2/FTR6
3	FTR COILS (TO)
4	AC-
5	PDA CKT5/SWPKS 9,10,11-1
6	PDA CKT6/SWPKS 12,13
7	EQUIP. GROUND
8	AC+ (FROM PDA)

O4 TERM	FUNCTION
1	+24VDC (controlled)
2	DC GROUND
3	IFI-14J, STOP TIME (FROM M.U)
4	IFI-14D, FLASH SENSE (FROM I.R)
5	EXTERNAL (M.U) RESET
6	WDT INPUT
7	LR COIL (UNIT IN)
8	SSR (PDA)
9	+24VDC
10	N/A

FT4 TERM	FUNCTION
A101	SWPK 13-RED
A102	SWPK 13-YEL
A103	SWPK 13-GRN
A104	SWPK 12-RED
A105	SWPK 12-YEL
A106	SWPK 12-GRN

FT5 TERM	FUNCTION
A111	SWPK 9-RED
A112	SWPK 9-YEL
A113	SWPK 9-GRN
A114	SWPK 10-RED
A115	SWPK 10-YEL
A116	SWPK 10-GRN

FT6 TERM	FUNCTION
A121	SWPK 11-GPO1
A122	SWPK 11-GPO2
A123	N/A
A124	N/A
A125	N/A
A126	N/A

FT7 TERM	FUNCTION
A131	ADV DC-
A132	ADV PRI
A133	ADV SEC
A134	SIM DC-
A135	SIM PRI
A136	SIM SEC

FT8 TERM	FUNCTION
A141	APP DC-
A142	APP IN
A143	GD DC-
A144	GD/ISL
A145	HS +24DC (Out)
A146	HS DC- (IN)

TERM.	FT7		FT8		HEALTH STATUS CIRCUIT		C16P		TB03		TB04	
POS/ SIDE	A	B	A	B	Contact	Contact	Pin	B	A	B	A	B
1	A131	TB04, 2	A141	TB04, 2	A145	HSR1, 6	1	A142				
2	A132	C16S, 5	A142	C16S, 1	HSR1, 4	HSR2, 6	2	A144				A146
3	A133	C16S, 6	A143	TB04, 2	HSR2, 4	FUSE H, 2	3	A135		HSR1, 2		
4	A134	TB04, 2	A144	C16S, 2	SWPK 11, 3	HSR2, 2	4	A136				
5	A135	C16S, 3	A145	HSR1, 6	N/A	N/A	5	A132				
6	A136	C16S, 4	A146	TB04, 2	N/A	N/A	6	A133				
7	N/A	N/A	N/A	N/A	N/A	N/A	7	N/A				
8	N/A	N/A	N/A	N/A	N/A	N/A	8	N/A				
9	N/A	N/A	N/A	N/A	N/A	N/A	9	N/A		N/A		FUSE H, 1
10	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A		N/A		N/A

NOTE:

1. A=external side, B=internal side.
   GPO2=General Purpose Output #2
   HSR1=Health Status Relay #1
2. See Health Status Circuit sheet and HSR Connector Wiring sheet for more details.
3. All dimensions shown are in inches.

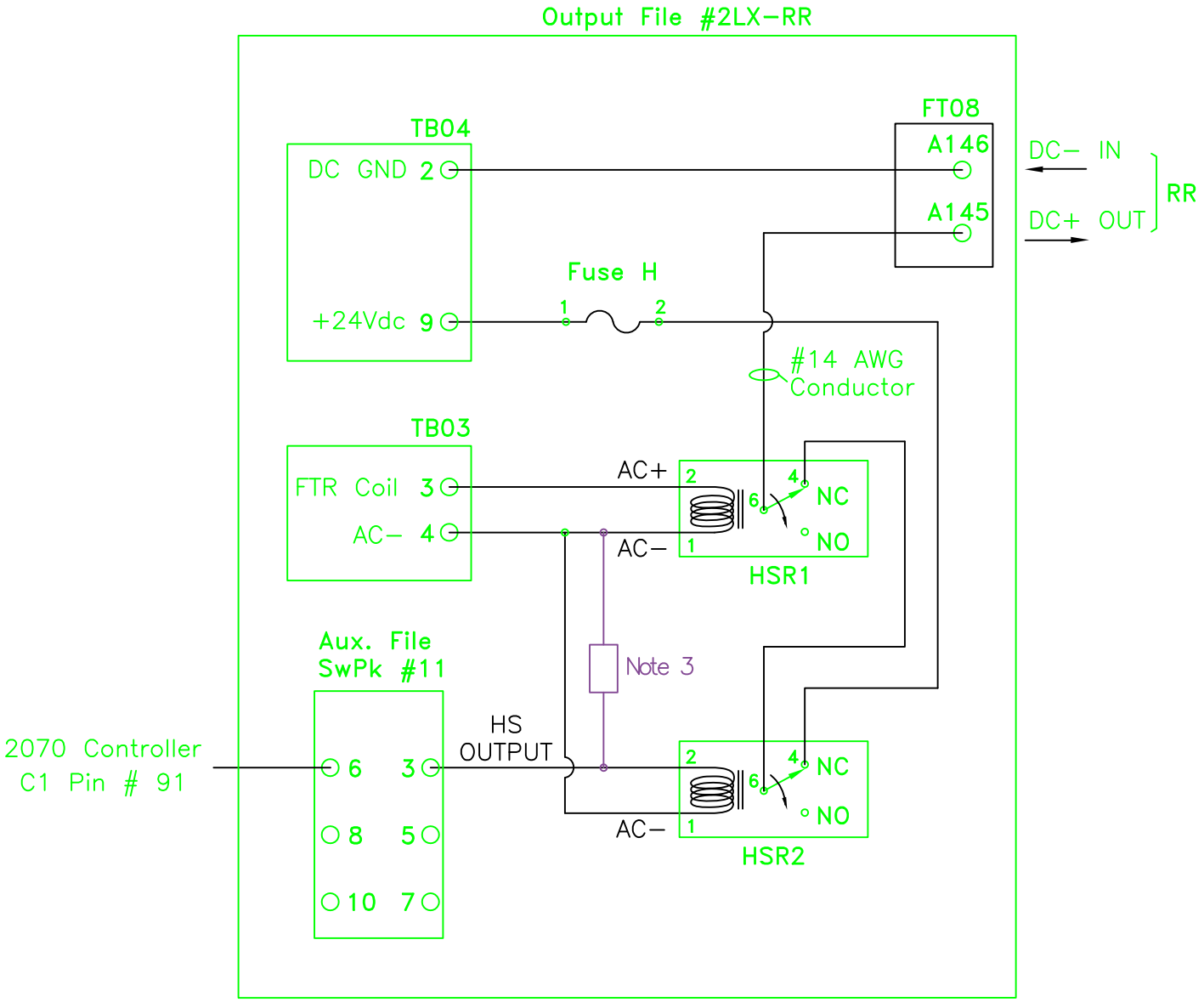
TITLE:
INPUT/OUTPUT FILE DETAILS
SHEET 9 OF 13

NO SCALE

TEES 2020

A6-51

HEALTH STATUS CIRCUIT



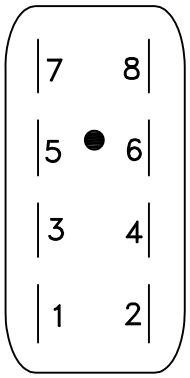
NOTES: (FOR THIS DETAIL)

1. HS=Health Status, HSR1=Health Status Relay 1, FTR=Flash Transfer Relay, Aux. File=Auxillary Output File or Output File #2
2. Fuse H shall be 0.5 Amp.
3. Add Snubber circuit for load.
4. All dimensions shown are in inches.

TITLE: INPUT/OUTPUT FILE DETAILS SHEET 10 OF 13	
	NO SCALE
TEES 2020	A6-52

HSR1 RELAY SOCKET DETAIL

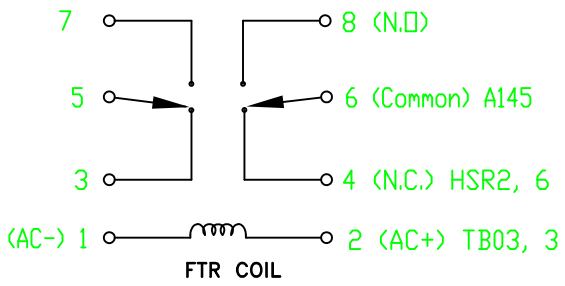
PIN	FUNCTION
1	COIL
2	COIL
3	N/A
4	RR
5	N/A
6	RR
7	N/A
8	N/A



MODEL 205 -
BEAU P-5408-LAB (Or Equal)

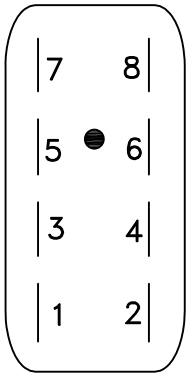
REAR VIEW

HEALTH STATUS RELAY (HSR1) CONNECTOR WIRING DETAIL



HSR2 RELAY SOCKET DETAIL

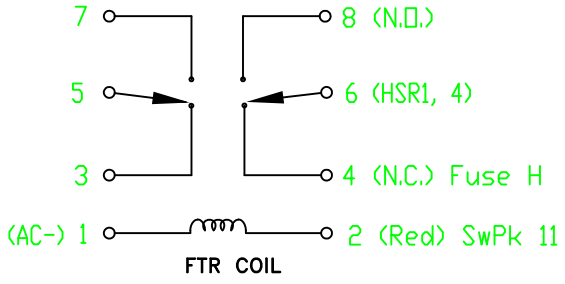
PIN	FUNCTION
1	COIL
2	SWPK 11, RED
3	N/A
4	DC+
5	N/A
6	RR
7	N/A
8	N/A



MODEL 205 -
BEAU P-5408-LAB (Or Equal)

REAR VIEW

HEALTH STATUS RELAY (HSR2) CONNECTOR WIRING DETAIL

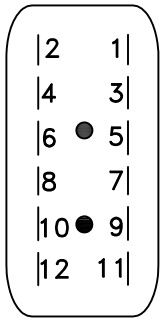


NOTE:
1. FT = Field Terminal,
   HSR=Health Status Relay
   RR=Railroad
2. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE HSR DETAILS SHEET 11 OF 13	
	NO SCALE
TEES 2020	A6-53

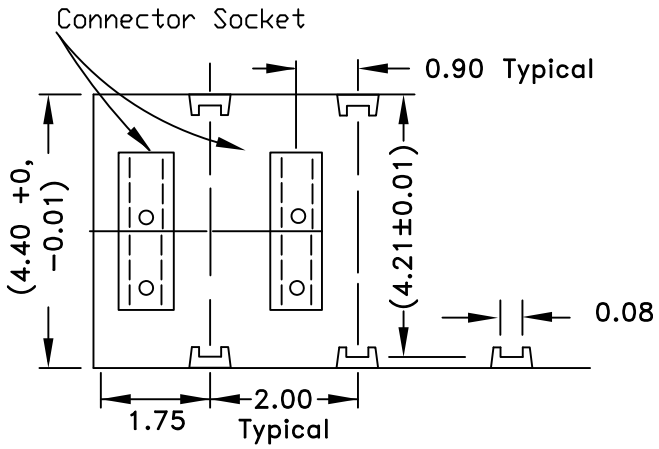
MODEL 200 SWITCH PACK SOCKET DETAIL

PIN	FUNCTION
1	AC+
2	EQUIP. GROUND
3	RED OUTPUT
4	NA
5	YELLOW OUTPUT
6	RED INPUT
7	GREEN OUTPUT
8	YELLOW INPUT
9	+24 VDC
10	GREEN INPUT
11	NA
12	NA

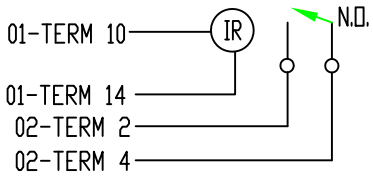


REAR VIEW

MODEL 200 SWITCH PACK MOUNTING DETAIL

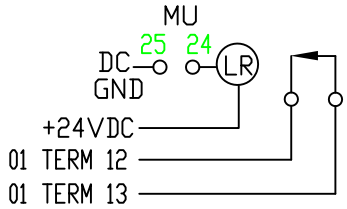


ISOLATION RELAY (IR) DETAIL



(Refer to detail A6-49)

LOGIC RELAY (LR) DETAIL



(Refer to detail A6-49)

NOTE:

1. Flash Transfer Relay, see A6-16.
2. All dimensions shown are in inches

TITLE: INPUT/OUTPUT FILE DETAIL SHEET 12 OF 13	
	NO SCALE
TEES 2020	A6-54

MODEL 210 MONITOR UNIT PIN ASSIGNMENT

CONNECTOR PIN No.	MONITOR FUNCTION	TERMINATION	CONNECTOR PIN No.	MONITOR FUNCTION	TERMINATION
1	SWPKS 2 GRN		A	SWPKS 2 YEL	
2	SWPKS 2P GRN		B	SWPKS 6 GRN	
3	SWPKS 6 YEL		C	SWPKS 6P GRN	
4	SWPKS 4 GRN		D	SWPKS 4 YEL	
5	SWPKS 4P GRN		E	SWPKS 8 GRN	
6	SWPKS 8 YEL		F	SWPKS 8P GRN	
7	SWPKS 5 GRN		H	SWPKS 5 YEL	
8	T&B		J	SWPKS 1 GRN	
9	SWPKS 1 YEL		K	T&B	
10	SWPKS 7 GRN		L	SWPKS 7 YEL	
11	T&B		M	SWPKS 3 GRN	
12	SWPKS 3 YEL		N	T&B	
13	T&B		P	NA	
14	NA		R	T&B	
15	T&B		S	T&B	
16	T&B		T	NA	
17	NA		U	T&B	
18	T&B		V	T&B	
19	NA		W	NA	
20	EQUIP. GROUND	01-TERM 9	X	NA	
21	AC-	01-TERM 10	Y	DC GROUND	02-TERM 2
22	WATCHDOG TIMER	C4-37	Z	EXTERNAL RESET	02-TERM 5
23	+24 VDC	02-TERM 1	AA	T&B	
24	B.D. OUT CKT	LOGIC RELAY COIL	BB	STOPTIME	02-TERM 3
25	B.D. OUT CKT	DC GROUND	CC	NA	
26	NA		DD	NA	
27	NA		EE	OUTPUT SW-SIDE 2	01-TERM 12
28	OUTPUT-SW SIDE 1	AC+	FF	AC+	01-TERM 11

NOTES: (FOR THIS DETAIL)

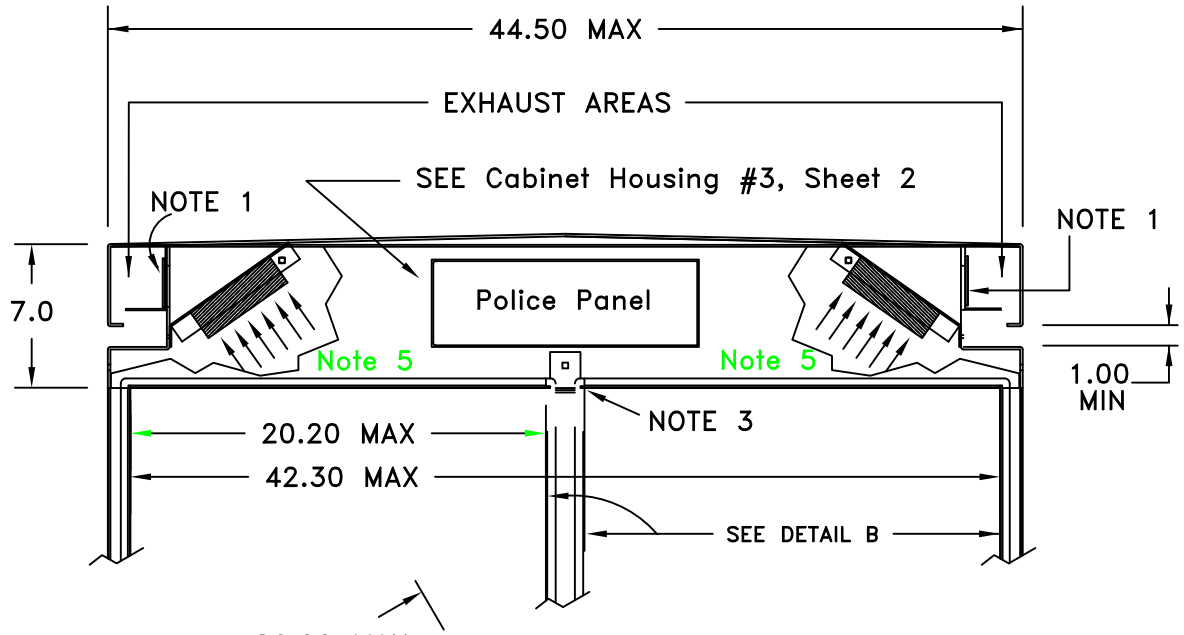
1. Top of relays shall be flush with face of file.
2. The isolation relay shall be Potter & Brumfield R10-E1-X2-115 (or equal). The logic relay (LR) shall be Potter & Brumfield KUP11(D11 or 15) or equal.
3. See connectors C4 & C5 wiring lists for connector/file interface.
4. Sheet definitions:
   - CKT = CIRCUIT
   - FU = FLASHER UNIT
   - FTR = FLASH TRANSFER RELAY
   - IFI-14D = INPUT FILE "I", TB 14, POSITION D
   - SSR = SOLID STATE RELAY
   - MU = MONITOR UNIT
   - N.C. = NORMALLY CLOSED RELAY CIRCUIT
   - N.O = NORMALLY OPEN RELAY CIRCUIT
   - PDA FU1 CKT1 = PDA FLASHER UNIT 1, OUTPUT CIRCUIT 1
   - POL PAN = POLICE PANEL
   - SW = SWITCH
   - SWPK(S) = SWITCH PACK(S)
   - T&B = CONDUCTORS CONNECTED TO PIN, TWO FEET IN LENGTH WITH RING LUG ON UNCONNECTED END, TIED & BUNDLED SEPARETELY.
   - 2P-2 = PHASE 2 PED. PIN 2
5. For details, see A3-3 & A3-4.
6. All dimensions shown are in inches.

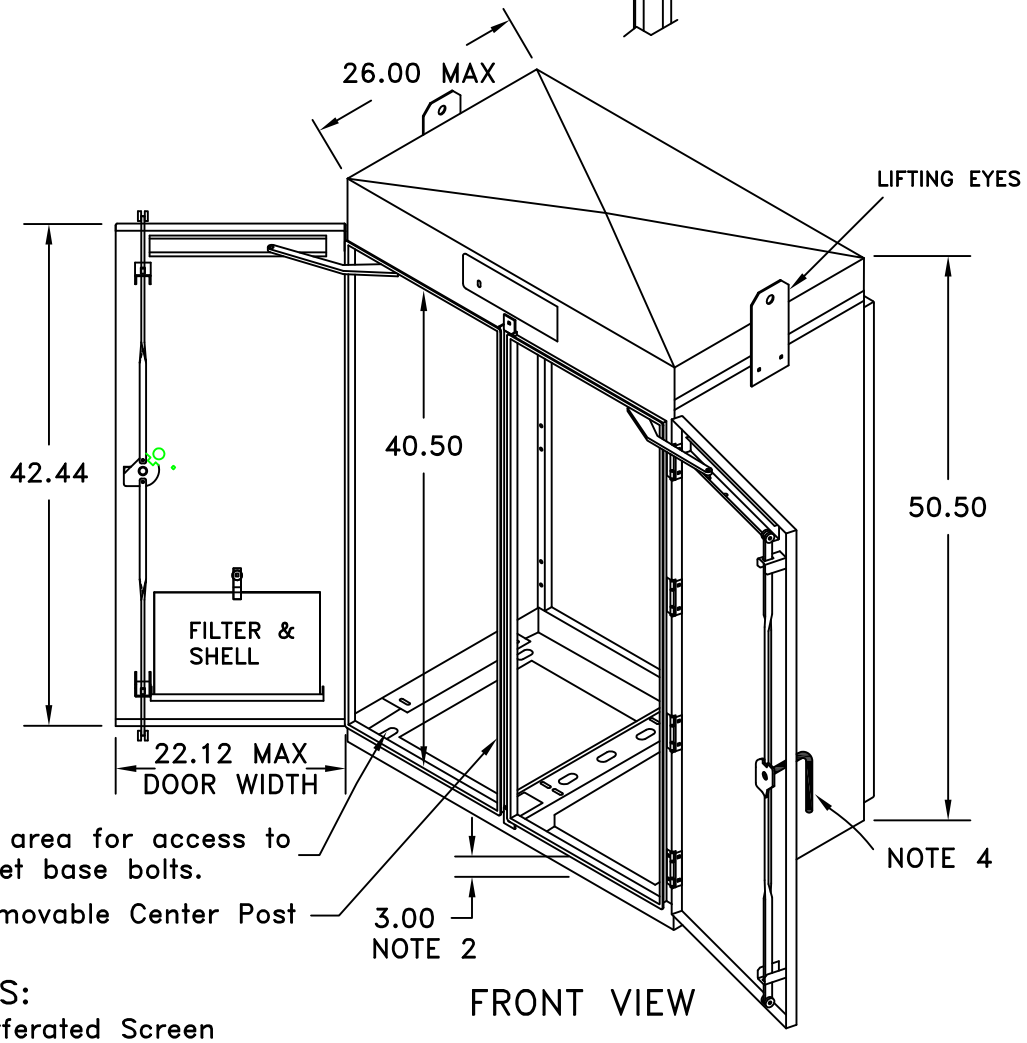
TITLE:

INPUT/OUTPUT FILE DETAILS
SHEET 13 OF 13

	NO SCALE
TEES 2020	A6-55

EXHAUST DETAIL





FRONT VIEW

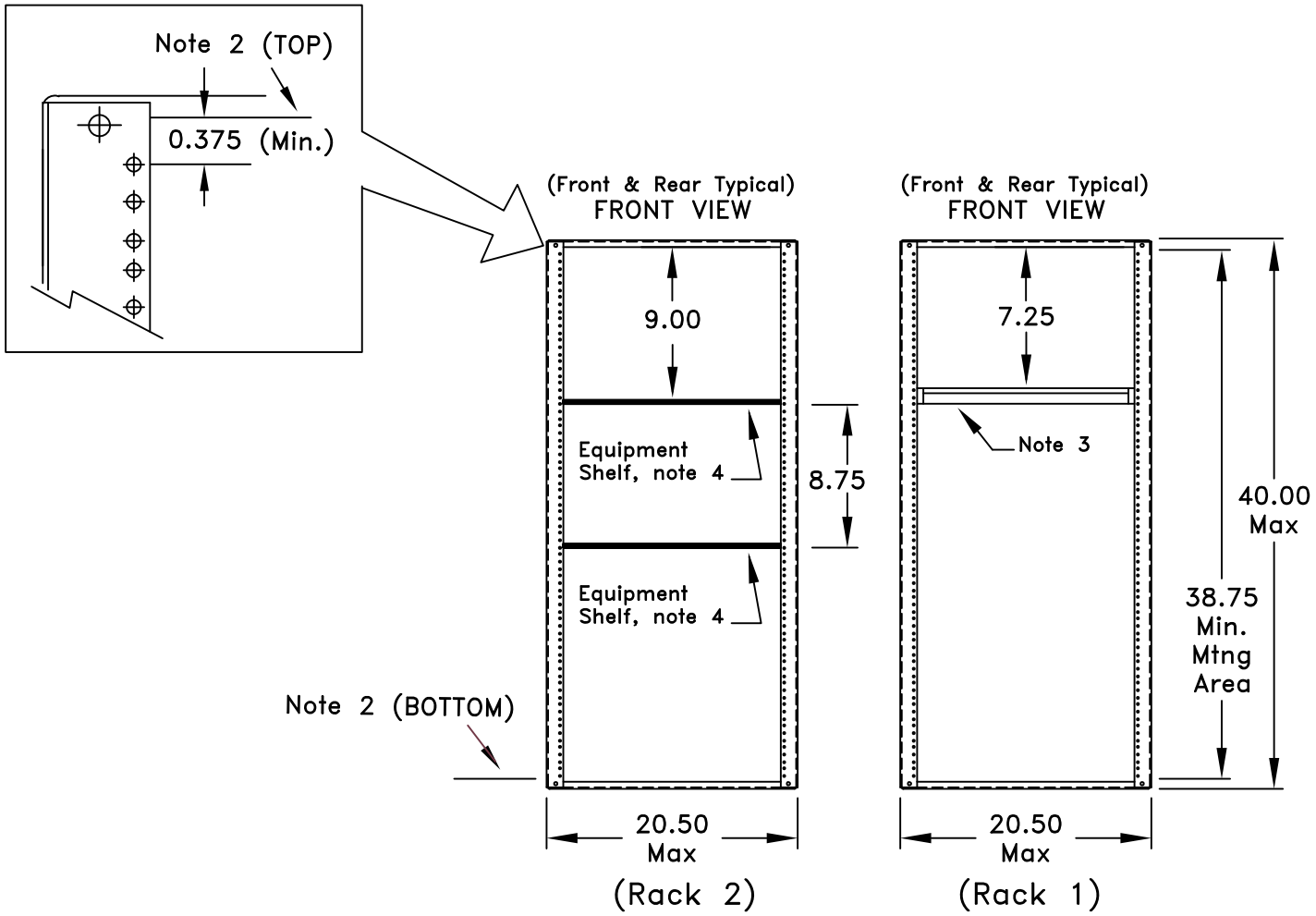
NOTES:

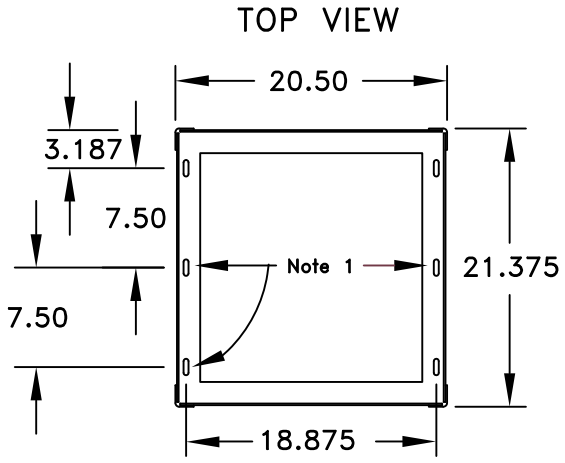
1. Perforated Screen
2. From Cabinet base to door lip
3. After center post is installed a sealant shall be applied to prevent leakage.
4. The handles shall be centered vertically on the door opposite from the hinges on both, the rear & front.
5. Two fans each side.
6. All dimensions shown are in inches.

TITLE:

CABINET HOUSING #4 DETAILS
SHEET 5 OF 7

	NO SCALE
TEES 2020	A6–56





HOLE SLOT DETAIL
B

0.375X1.250 OBROUND

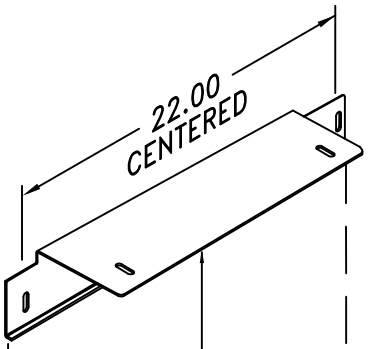
NOTES

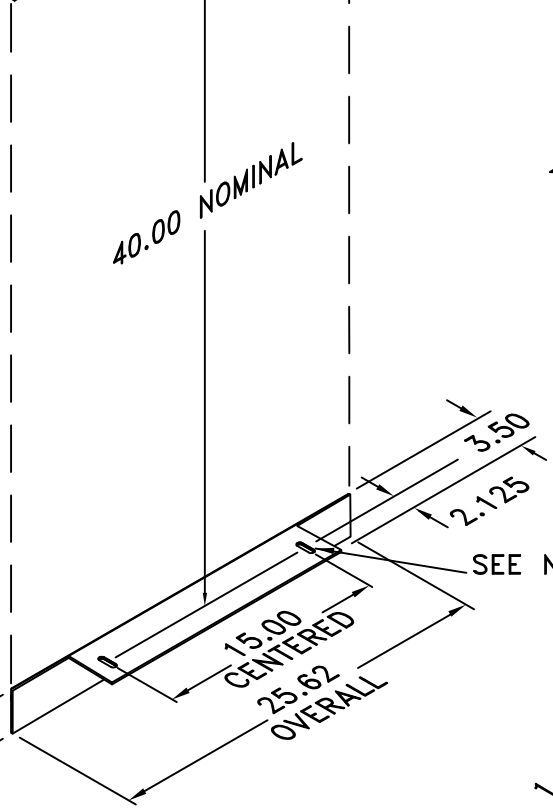
1. Hole Slot Detail B, Cage #2 details A6–2.
2. TOP, Refers to the bottom lip of the top hat.
   BOTTOM, Refers to the top lip of the bottom hat.
3. Controller unit support drawer shelf assembly, A6–6.
4. Equipment shelf, A6–41.

TITLE: CABINET HOUSING #4 DETAILS SHEET 6 OF 7	
	NO SCALE
TEES 2020	A6–57

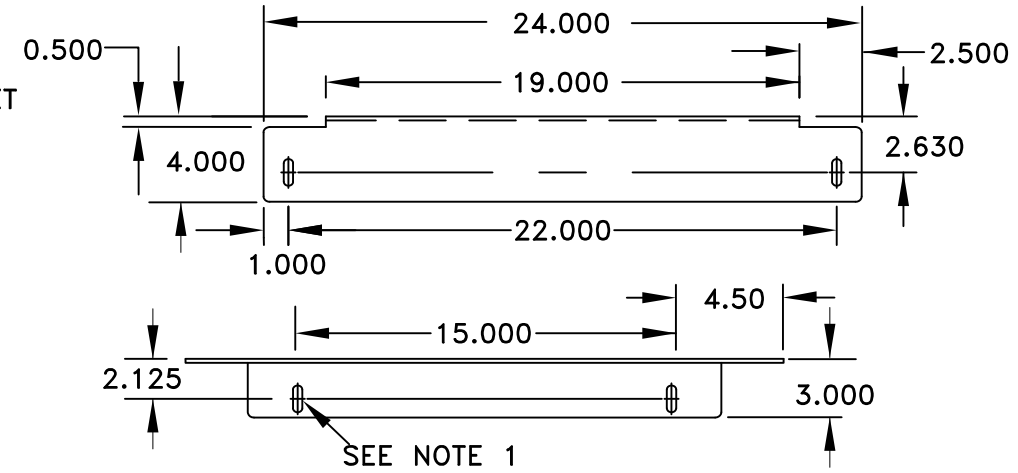
HOUSINGS 4 TO CAGE 1 SUPPORT DETAILS

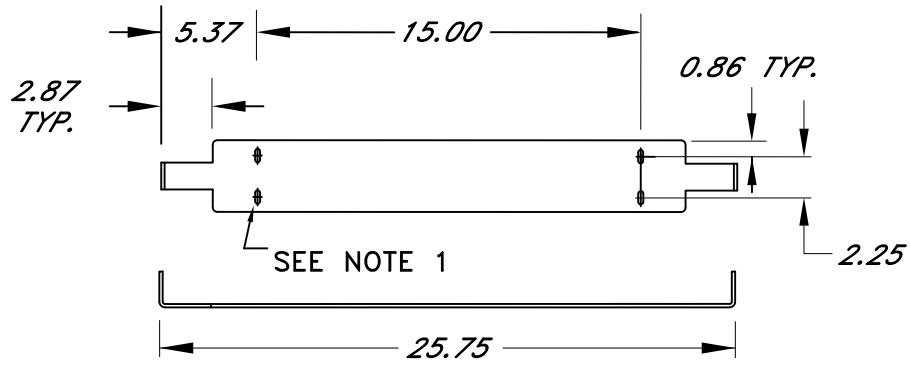
SPANNER BRACKET ATTACHED TO SIDE OF CABINET



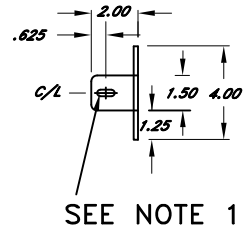


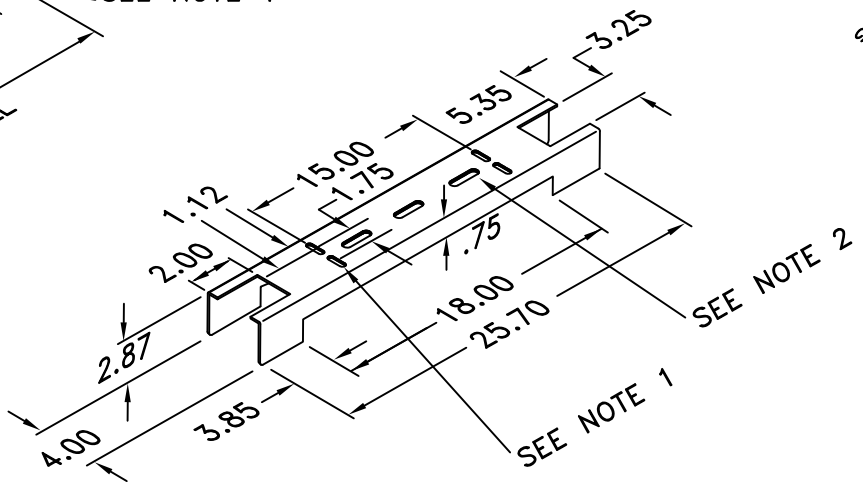
SPANNER BRACKET DETAIL





TOP RACK SUPPORT





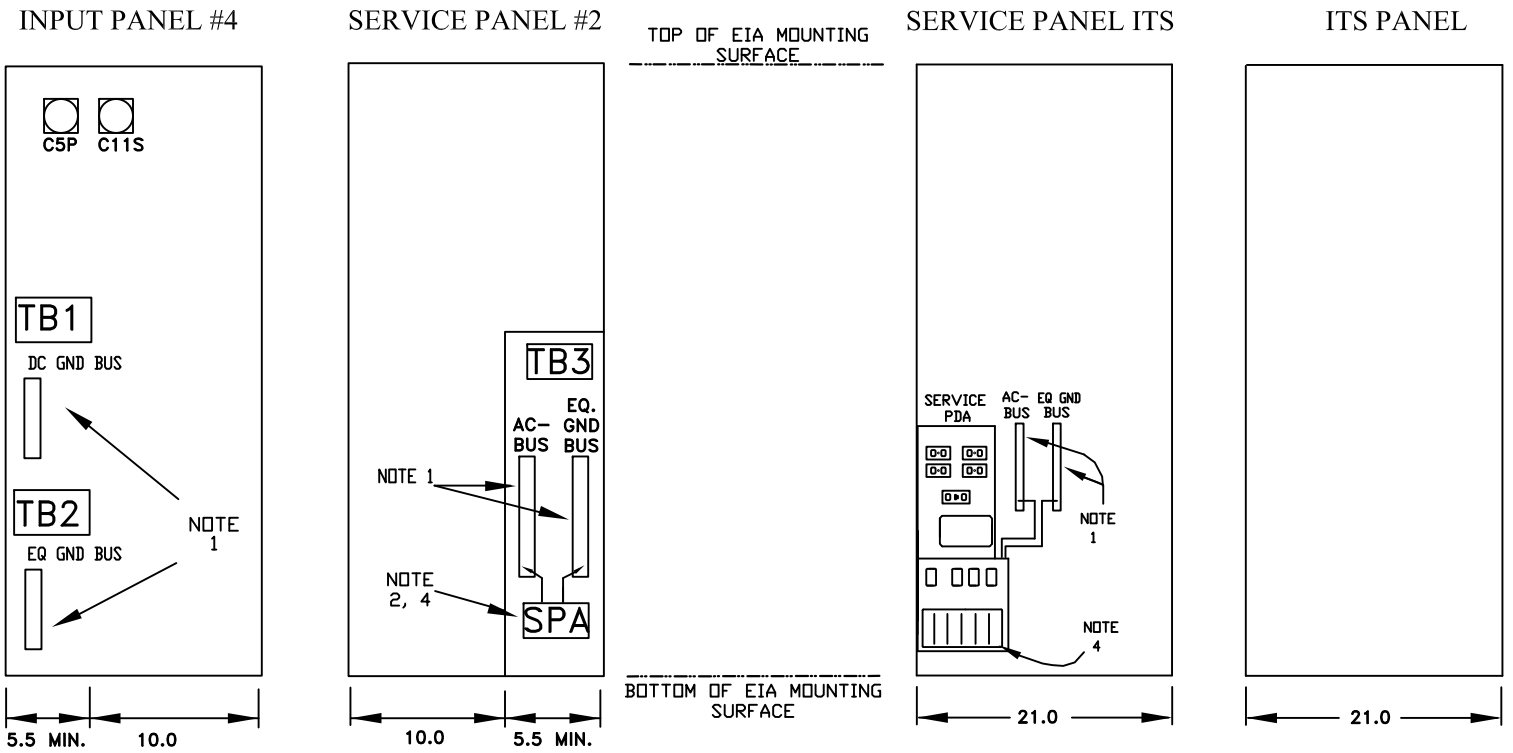
CENTER CHANNEL
PART IS WELDED TO BOTTOM PLATE

NOTES:

1. Hole Slot Detail B see Cabinet Housings 3 Detail 2
2. Hole Slot Detail A see Cabinet Housings 3 Detail 2
3. All dimensions shown are in inches.

TITLE: CABINET HOUSING #4 DETAILS SHEET 7 OF 7	
	NO SCALE
TEES 2020	A6–58

MODEL 346LX SIDE PANEL

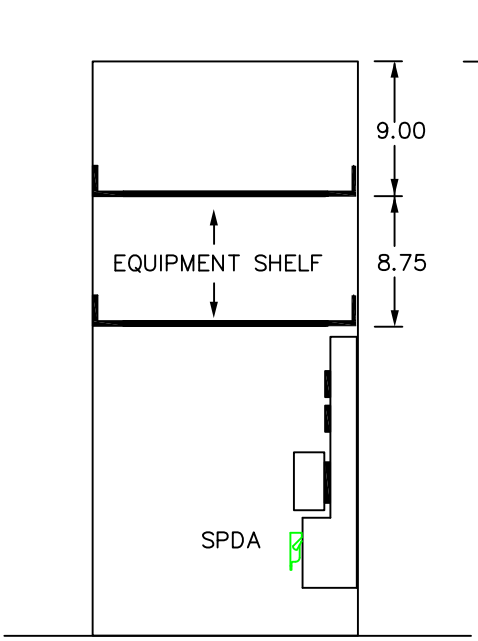


NOTES:

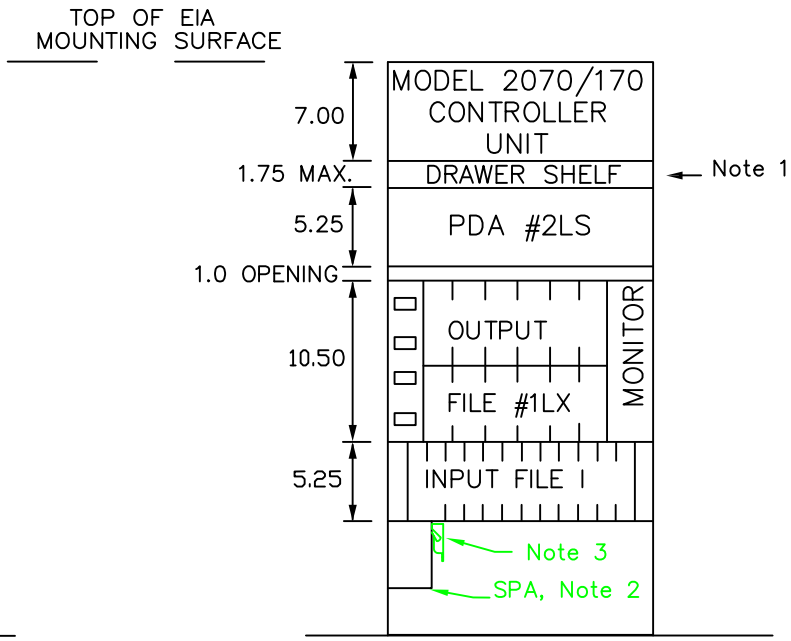
1. 10 terminal (#8 wire) minimum copper bus.
2. The terminal block shall have terminal positions necessary to match position assignments.
3. Terminal position screws shall be 8–32 except for RTB0, TBS, TB0, TB3, which shall be 10–32
4. SPA and the Service PDA shall be bolted on the Rail and firmly attached to the Service Panel.
5. The AC terminal blocks shall have touch–safe contacts, Weidmuller or equal.
6. All dimensions shown are in inches.

TITLE: MODEL 346LX SIDE PANEL DETAILS	
	NO SCALE
TEES 2020	A6-59

MODEL 346LX



FRONT VIEW
(Rack 2)



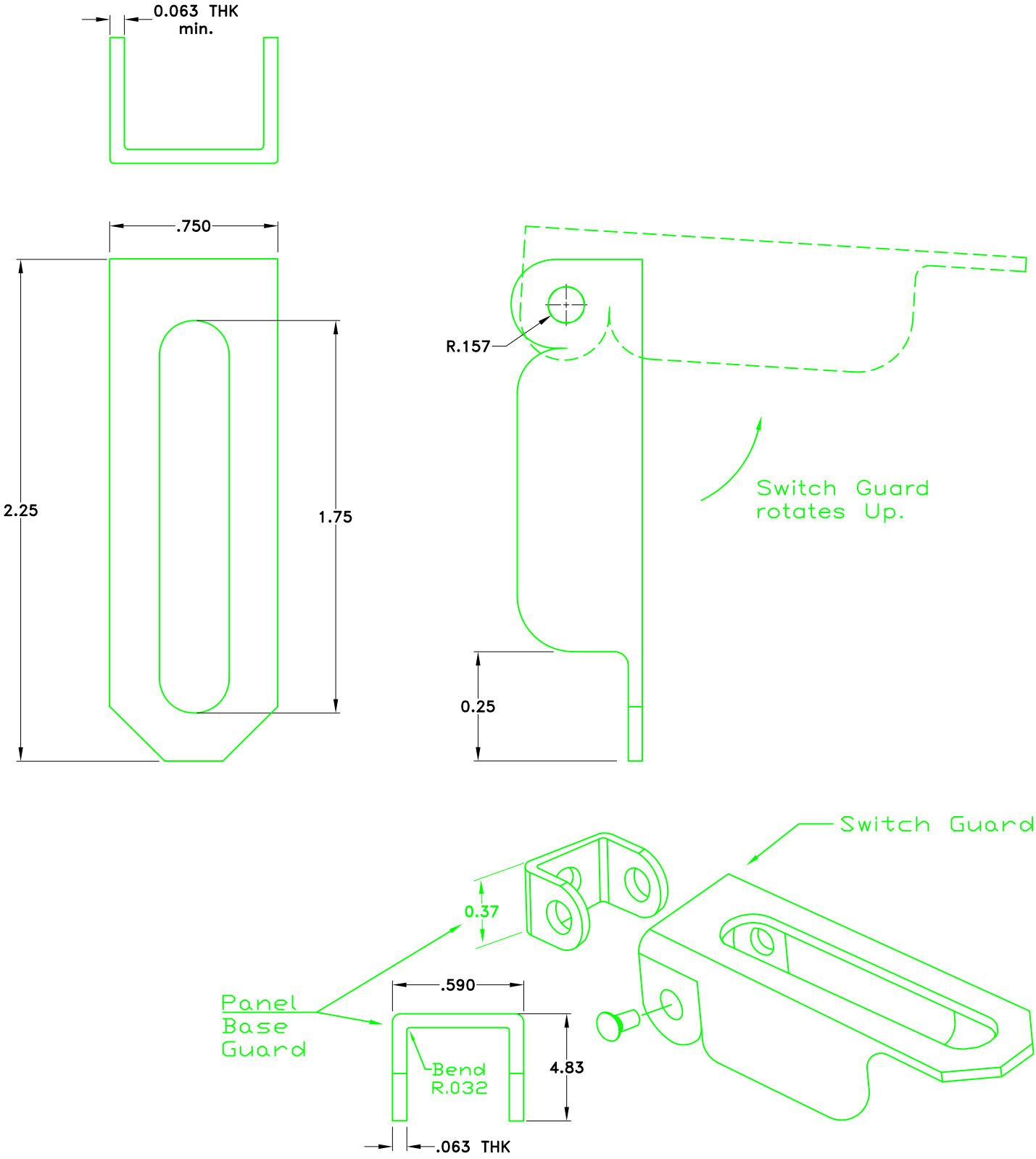
FRONT VIEW
(Rack 1)

NOTE:

1. Controller unit support drawer shelf assembly.
2. SPA shall be bolted on the rail and firmly attached to the Service Panel.
3. Switch Guard, see A6–61.
4. All dimensions shown are in inches.

TITLE: CABINET EQUIPMENT MOUNTING DETAILS SHEET 3 OF 3	
	NO SCALE
TEES 2020	A6–60

CIRCUIT BREAKER SWITCH GUARD

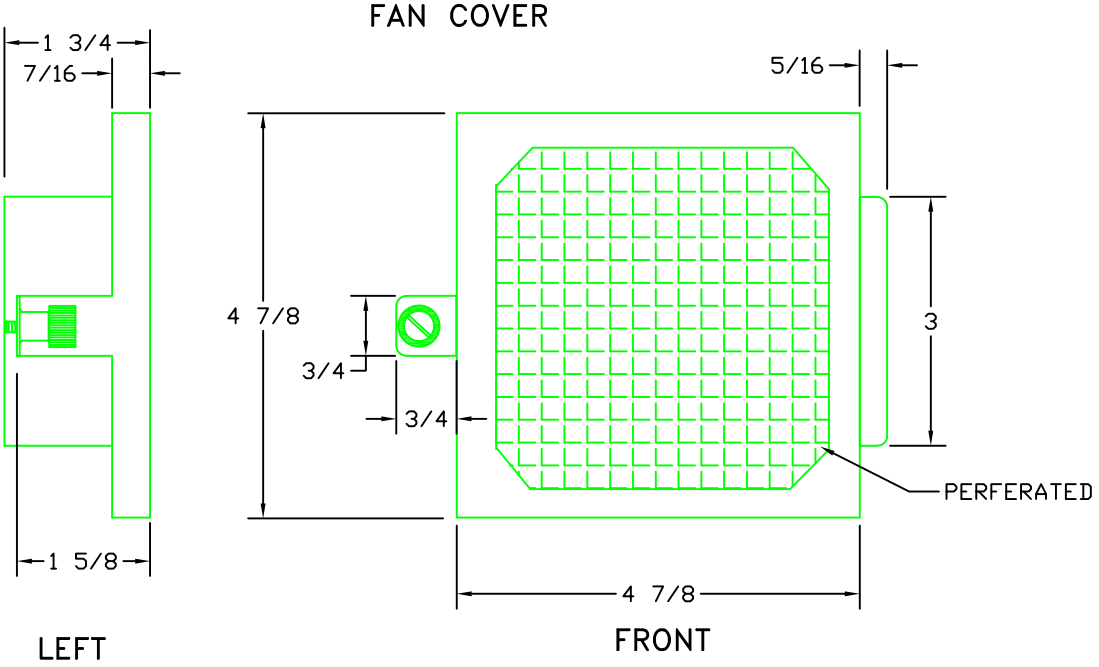


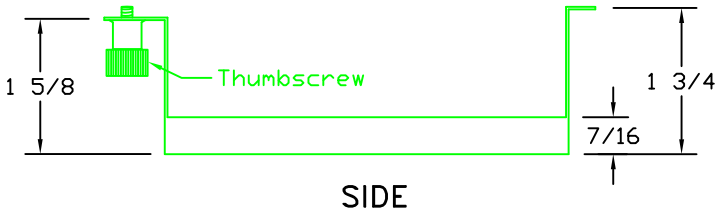
NOTES: (FOR THIS DETAIL)

1. Circuit Breaker Switch Guard for SPA and Service PDA.
2. All dimensions shown are in inches.

TITLE: CIRCUIT BREAKER SWITCH GUARD DETAILS	
	NO SCALE
TEES 2020	A6-61

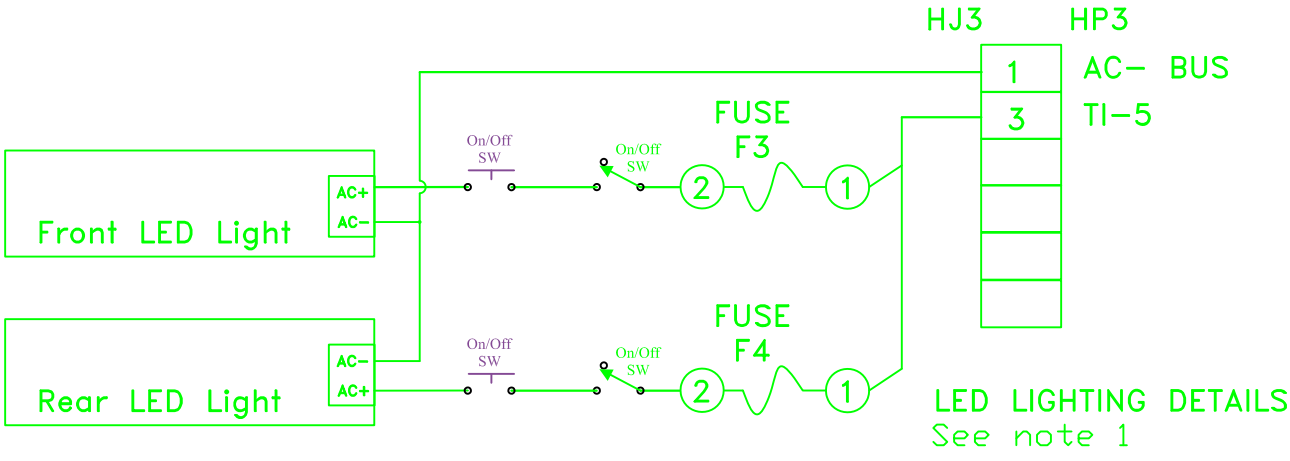
FAN COVER





SIDE

HARNESS JACK/PLUG NO. 3

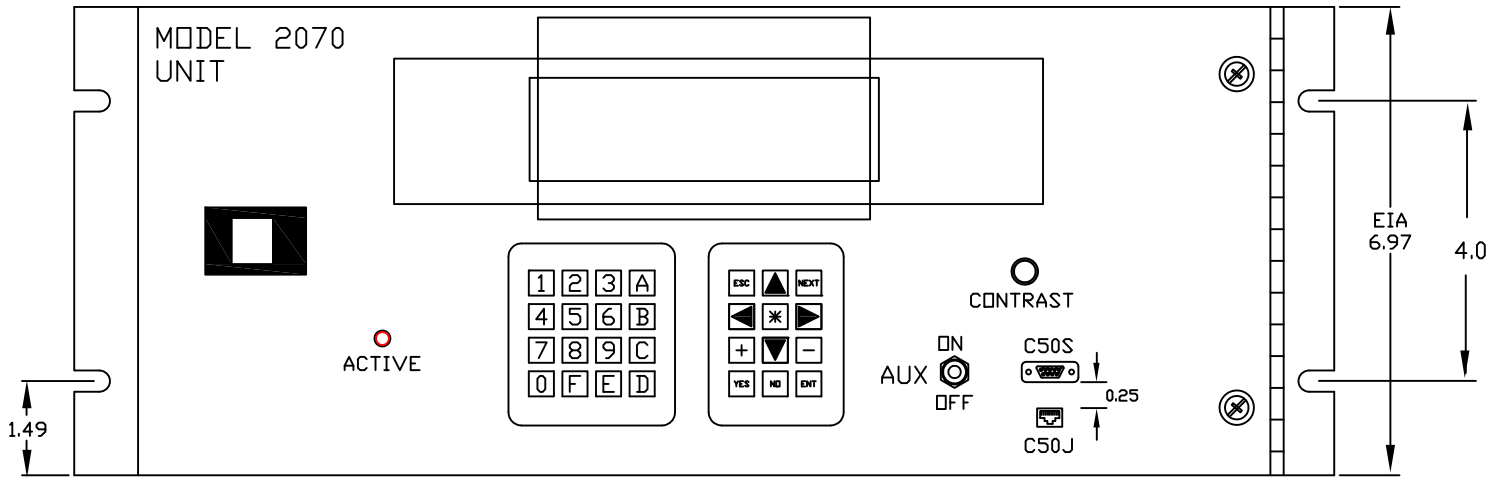


LED LIGHTING DETAILS
See note 1

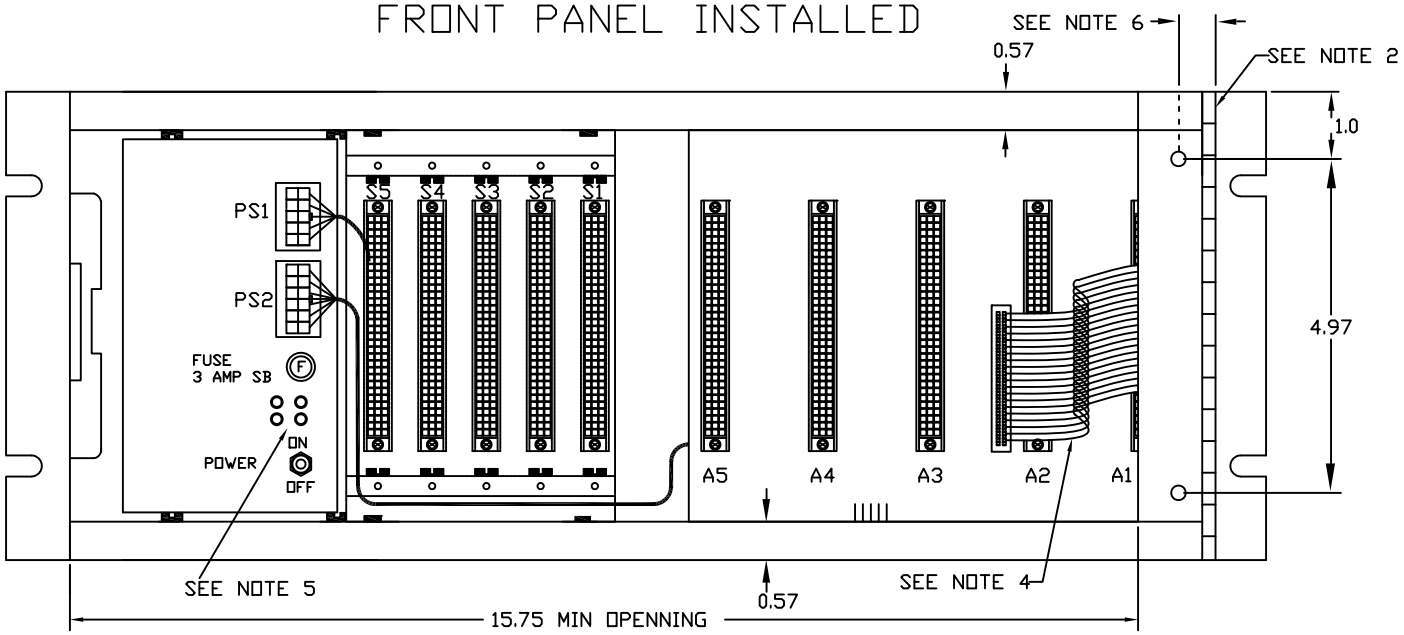
NOTE:
1. LED Lights for 342LX, 344LX and 346LX cabinets
2. The LED switch shall be labeled cabinet lights.
3. Fan cover made of Aluminum
4. All dimensions are in inches

TITLE: FAN COVER AND LED LIGHTING HOUSING	
	NO SCALE
TEES 2020	A6-62

APPENDIX A9
CHAPTER 9 DETAILS



FRONT PANEL INSTALLED

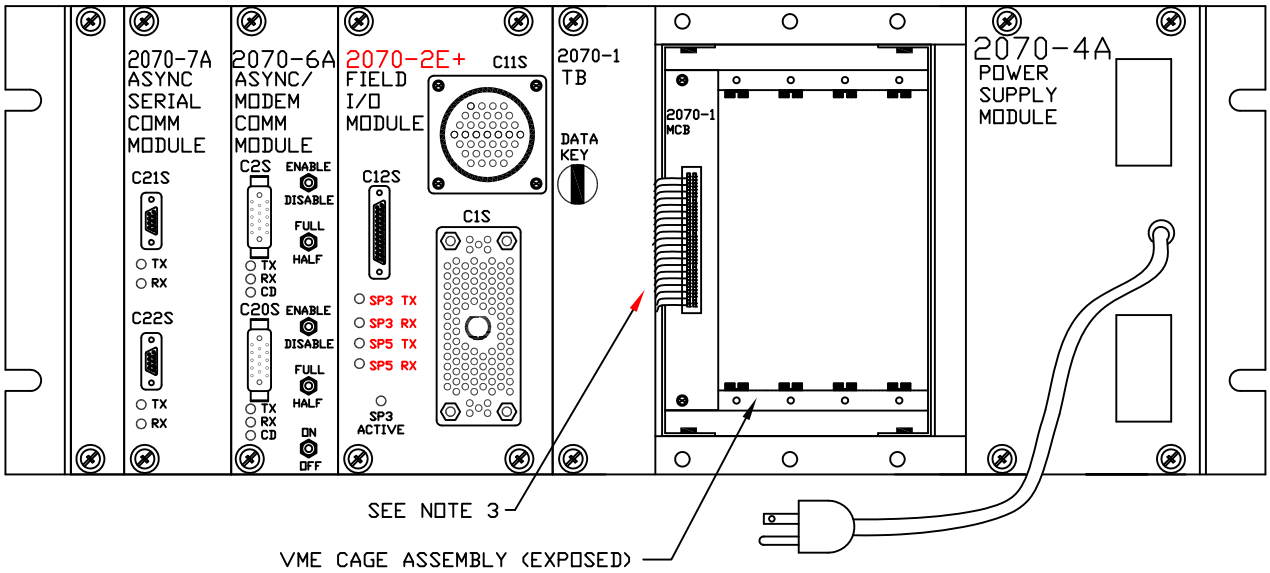


FRONT PANEL REMOVED

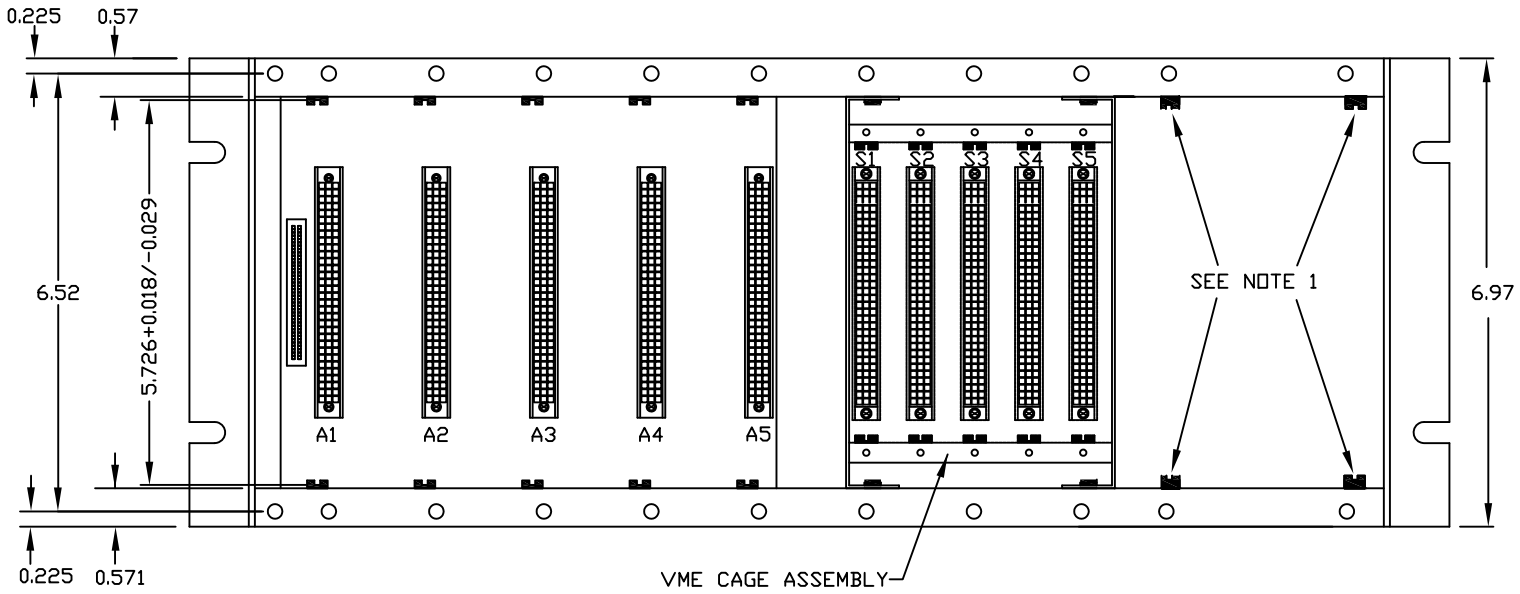
NOTES: (FOR THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA–310B Rack using 4U open end mounting slots.
2. Continuous stainless steel hinge (0.157in maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.
3. Actual location of ACTIVE light, AUX switch, C50S, C50J and contrast control shall be limited to ACTIVE light on the left side of the panel; AUX switch, C50S, C50J and the contrast control on the right side. They shall be located greater than 1 in from the edge of each other, other devices, connector or latch. C50J only needs to be 0.25in minimum from C50S.
4. The length of the Front Panel Harness shall be 5in + 2% and it shall be removeable.
5. LED indicators for each DC voltage shall be provided.
6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside plane) shall be 0.55in.
7. All dimensions shown are in inches.

TITLE: MODEL 2070-CHASSIS FRONT VIEW	
	NO SCALE
TEES 2020	A9-1



REAR VIEW, LOADED

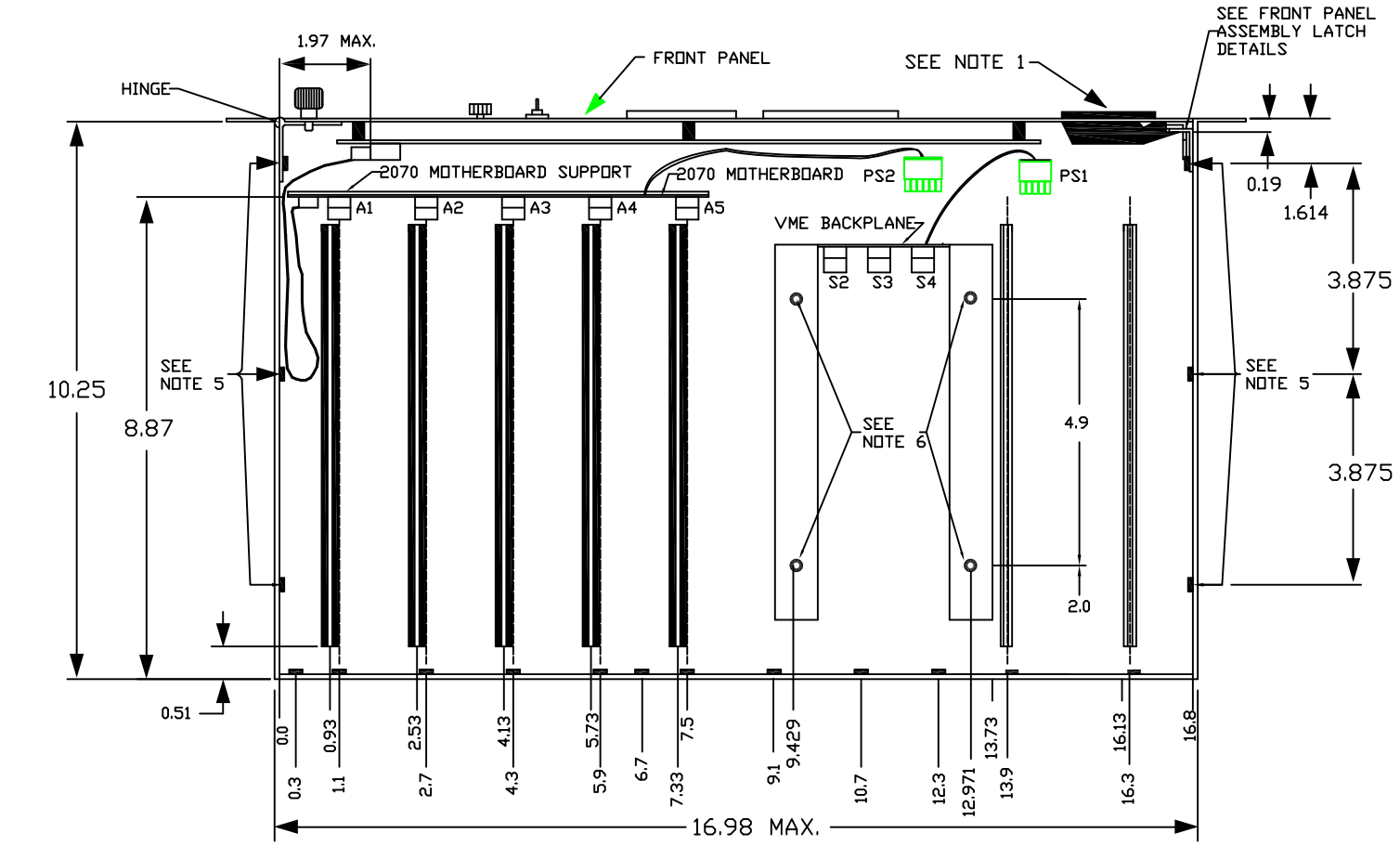


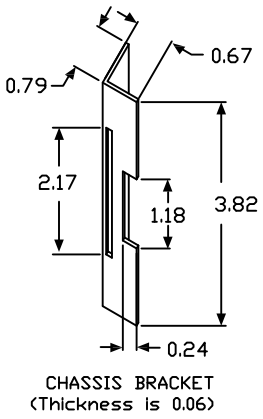
REAR VIEW, UNLOADED

NOTES: (FOR THIS DETAIL)

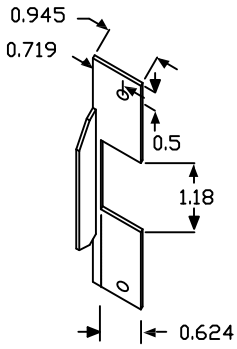
1. Four permanently attached 8in long Card Guides SAE 1800F (OR EQUAL) beginning 0.51in from the backplane mounting surface.
2. TB – TRANSITION BOARD
   MCB – MAIN CONTROLLER BOARD
3. Maximum length of harness shall be 4in, and shall not protrude beyond the back of the 2070 unit.
4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.
5. Blank plates shall cover all unused module openings.
6. All Module Front Plates thickness shall be (0.08±0.005)
7. All dimensions shown are in inches.

TITLE: MODEL 2070-CHASSIS REAR VIEW	
	NO SCALE
TEES 2020	A9-2

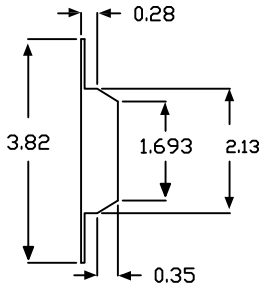




CHASSIS BRACKET
(Thickness is 0.06)



FRONT PANEL BRACKET



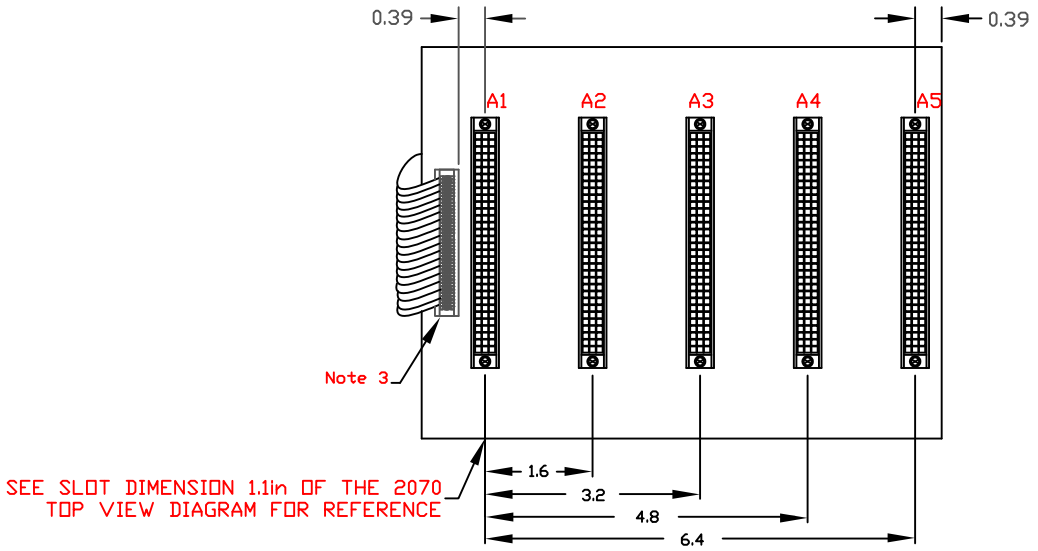
SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

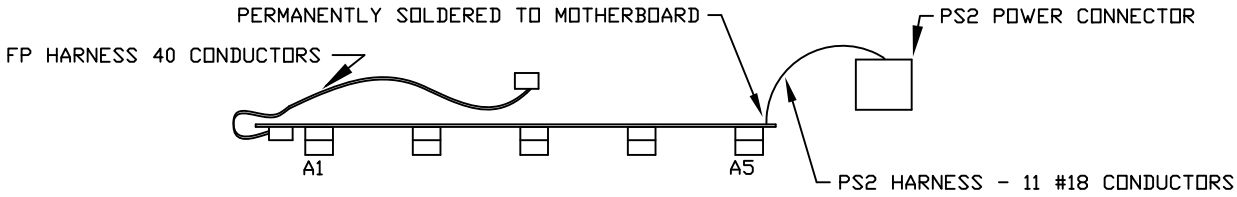
NOTES: (FOR THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 0.51 inch from the Backplane outside surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 1 inch when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 0.25 inch above unit baseline.
6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 0.571 inch folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 0.71 inch as measured from the front surface of the front panel.
8. Chassis side plates shall be 0.090in thick.
9. All dimensions shown are in inches.

TITLE: MODEL 2070-CHASSIS TOP VIEW	
	NO SCALE
TEES 2020	A9-3



CONNECTOR VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4TXD+	2	SP4TXD-
3	SP4RXD+	4	SP4RXD-
5	SP6TXD+	6	SP6TXD-
7	SP6RXD+	8	SP6RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DCG #1	22	DCG #1
23	+12 VDC SER	24	-12 VDC SER
25	DCG #1	26	DCG #1
27	CPU LED	28	DCG #1
29	CPURESET	30	DCG #1
31	DCG #1	32	C50 ENABLE
33	DCG #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISO +12 VDC
7	DCG #2 (ISO +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

NOTES: (FOR THIS DETAIL)

1. The Motherboard shall be a 0.125 inch minimum thickness pcb mechanically mounted in a vertical position.
2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).
3. The FP Harness shall be connected to the Motherboard via a header connector. Pin 1 shall be in the lower right hand corner.
4. Front Panel Harness Connector shall intermate with AMP 102-160-9 or equal located on Front Panel PCB.
5. Angle Brackets shall support the Motherboard to the Model 2070 chassis.
6. All dimensions shown are in inches.

TITLE: MODEL 2070 CHASSIS MOTHERBOARD	
	NO SCALE
TEES 2020	A9-4

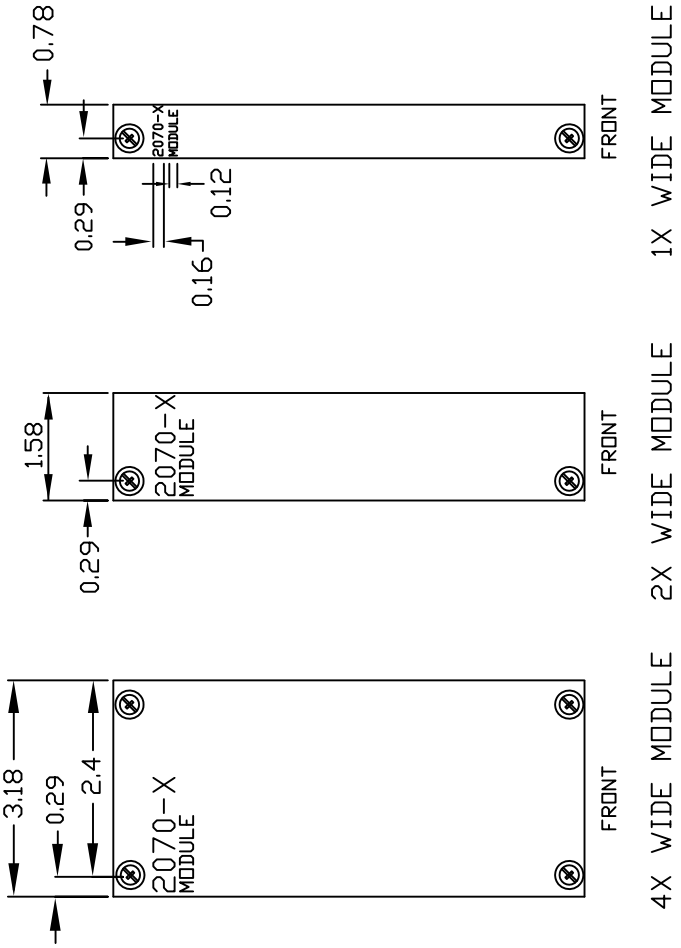
A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXC0+	SP5RXD+
6	SP3RTS-	SP3TXC0-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXC0+
20	NA	NA	SP3TXC0-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NetP5 (TX+)	NA	SP3TXCI-
23	NetP5 (TX-)	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NetP5 (RX+)	POWERUP	CPURESET
26	NetP5 (RX-)	POWERDOWN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

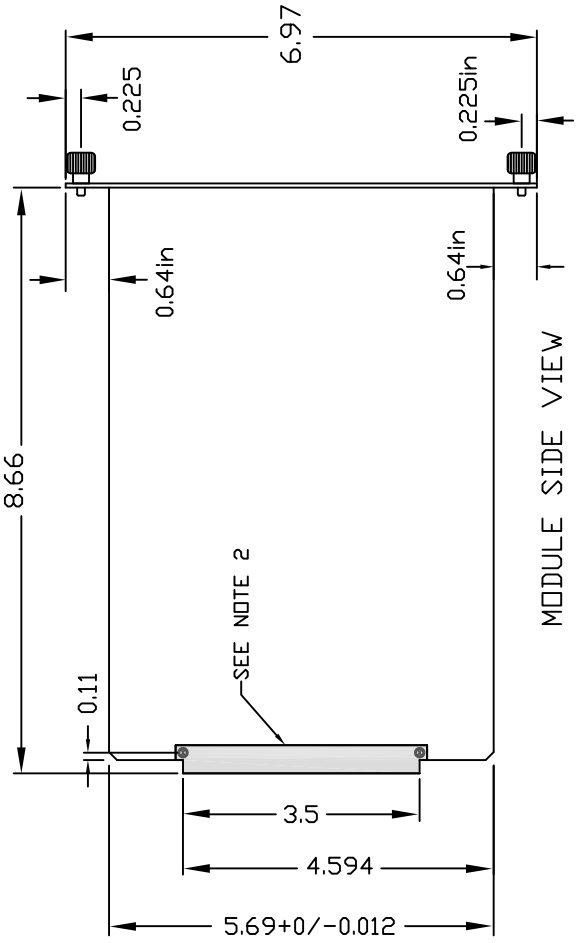
A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXC0+	SP3CTS+
16	SP2RTS-	SP2TXC0-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXC0+
20	SP2DCD-	SP2RXC-	SP3TXC0-
21	DCG #1	NA	SP3TXCI+
22	NetP5 (TX+)	NA	SP3TXCI-
23	NetP5 (TX-)	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NetP5 (RX+)	POWERUP	CPURESET
26	NetP5 (RX-)	POWERDOWN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

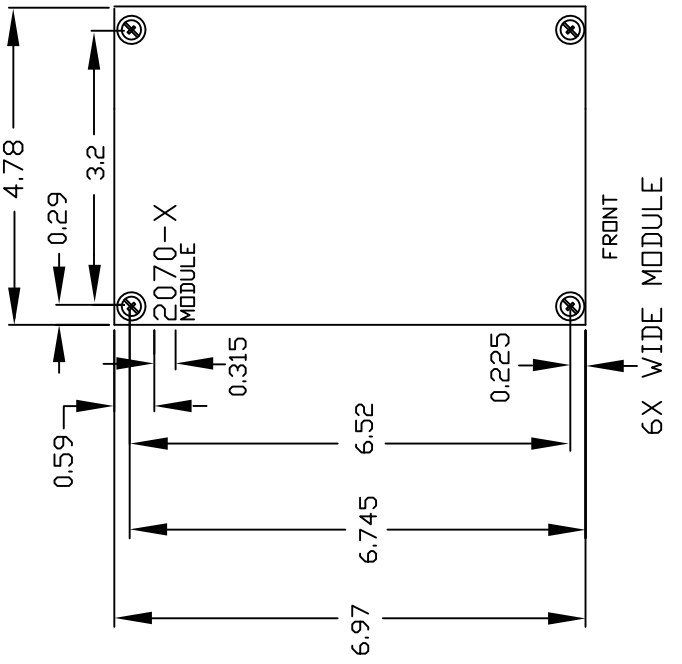
NOTES: (FOR THIS DETAIL)

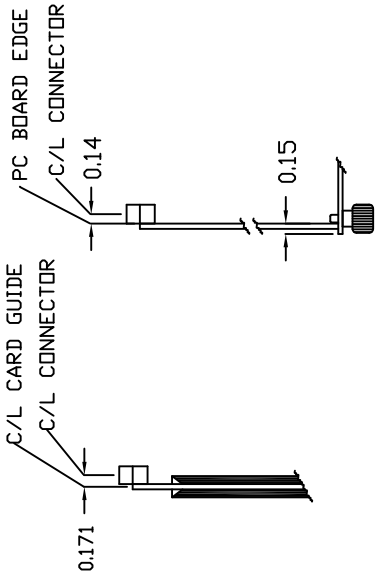
1. Functions are referenced to the CPU.
2. DCG #1 for +5VDC and +/−12VDC SER.
   DCG #2 for ISO +12 VDC.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (NA) is reserved for network protection only, ie., "Ethernet Shield".
6. Module installed in slot A2 enables SP1 & SP2 on 2070−1x modules.
7. Module installed in slot A3 enables SP5, on 2070−1x modules.
8. SP3 and SP6 are always enabled.
9. "C50 ENABLE" Active (e.g. DCG #1) is used by module installed in slot A1 to disable its channel 2 (i.e. SP4).
10. NetP5 signals TX+, TX−, RX+, RX− respectively.

TITLE: MODEL 2070-MOTHERBOARD A1-A5 CONNECTOR PIN OUT	
	NO SCALE
TEES 2020	A9-5







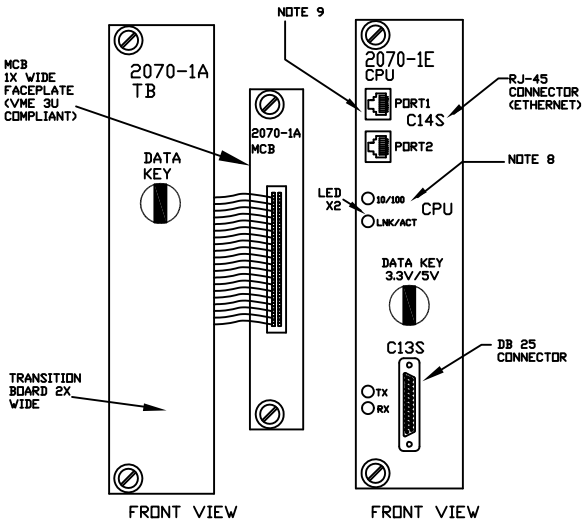


NOTES: (FOR THIS DETAIL)
1. All Thumbscrew devices on modules described in this drawing shall be TSD#3 or equal.
2. 96 pin DIN connector ELCO # 00 8272 96 000 013 or equal.
3. Front panel shall be Aluminum stock or Stainless Steel.
4. All dimensions shown are in inches.

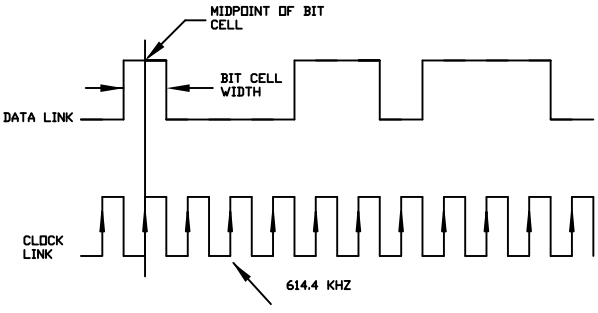
TITLE: MODEL 2070-SYSTEM PCB MODULES GENERAL	
	NO SCALE
TEES 2020	A9-6

SERIAL PORT REQUIREMENTS			
LOGICAL PORT		RATE KBITS	PROTOCOL
SP1		1.2, NOTE 1	ASYNC
SP1S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP2		1.2, NOTE 1	ASYNC
SP2S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP3		1.2, NOTE 1	ASYNC
SP3S		614.4, NOTE 3	SYNC, HDLC, SDLC
SP4		9.6, NOTE 1	ASYNC
SP5		1.2, NOTE 1	ASYNC
SP5S		614.4	SYNC, HDLC, SDLC
SP6		38.4, NOTE 1	ASYNC
SP8**	NOTE 4	9.6, NOTE 1	ASYNC
SP8S**	NOTE 4	153.6	SYNC, HDLC, SDLC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8TXD+	14	SP8TXD-
2	SP8RXD+	15	SP8RXD-
3	SP8TXC+	16	SP8TXC-
4	SP8RXC+	17	SP8RXC-
5	SP8RTS+	18	SP8RTS-
6	SP8CTS+	19	SP8CTS-
7	SP8DCD+	20	SP8DCD-
8	NA	21	NA
9	LINESYNC+	22	LINESYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

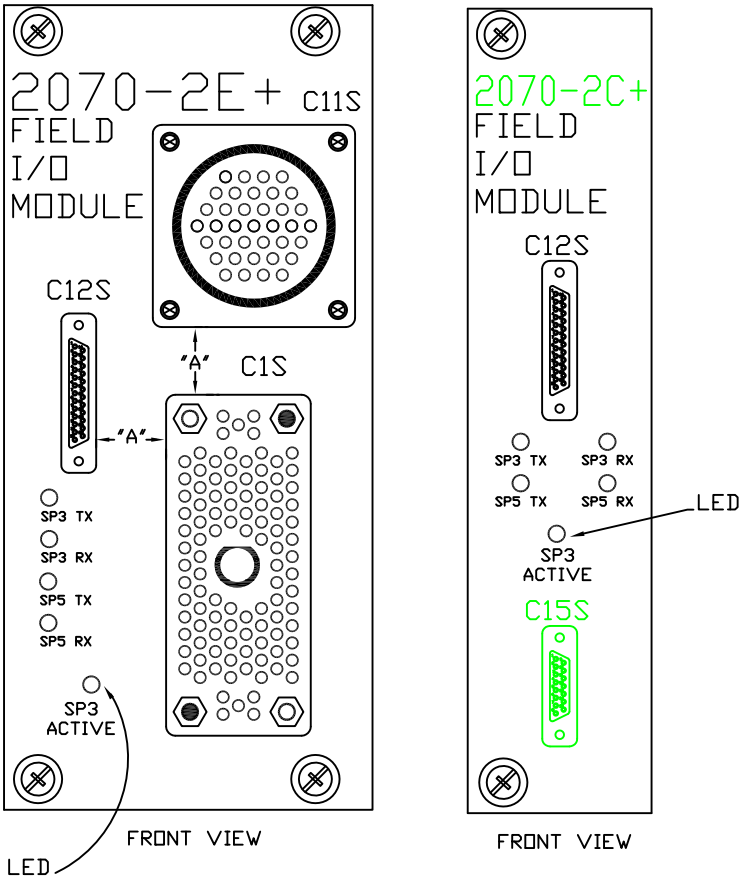
C14S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

1. Additional rates 1.2, 2.4, 4.8, 9.6, 19.2, 38.4.
2. Additional descriptors for other rates:
   SPxSa = 19.2, SPxSb = 38.4, SPxSc = 57.6
   SPxSd = 76.8, SPxSg = 64.0, SPxSe = 153.6.
3. Additional descriptors for other rates:
   SPxSe = 153.6, SPxSf = 614.4.
4. On 2070-1A, SP1 is assigned to 68360 SCC1. On 2070-1E, SP1 and SP8 are assigned to the dual SCC, and ETHERNET is assigned to 68EN360 SCC1.
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.
6. BIAS +5VDC (50mA maximum) refers to voltage required for a Line Terminator device and is derived from the ISO +12VDC Power Supply.
7. EG (Equipment Ground) pin is electrically connected to the faceplate.
8. LED indicators between switch & CPU
9. All RJ-45 connectors shall contain LED indicators 10/100 & LNK/ACT

** 2070-1E only.

TITLE:	MODEL 2070-1E CPU MODULES AND SERIAL PORT/SDLC PROTOCOL	
		NO SCALE
TEES 2020		A9-7



FIELD I/O FACE PANELS

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP5TXD+	14	SP5TXD-
2	SP5RXD+	15	SP5RXD-
3	SP5TXC+	16	SP5TXC-
4	SP5RXC+	17	SP5RXC-
5	SP3TXD+	18	SP3TXD-
6	SP3RXD+	19	SP3RXD-
7	SP3TXC+	20	SP3TXC-
8	SP3RXC+	21	SP3RXC-
9	LINE SYNC+	22	LINE SYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

C15S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP3 TXD+	9	SP3 TXD-
2	DCG #2	10	Port 1 Disable
3	SP3 TXC+	11	SP3 TXC-
4	DCG #2	12	EG
5	SP3 RXD+	13	SP3 RXD-
6	DCG #2	14	DCG #2
7	SP3 RXC+	15	SP3 RXC-
8	DCG #2		

NOTES: (FOR THIS DETAIL)

1. 2070-2E+ front panel shall be 4X wide. 2070-2C front panel shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)
2. Dark Circles in the C1S Connector denote guide pin locations and opencircles denote guide socket locations.
3. Dimension "A" shall be a minimum of 0.5in.
4. C1S - M104 Type. C11S - 37-Pin Circular Plastic Type. C12S - 25-Pin DB Socket Type. C15S - 15-Pin DB Socket Type.
5. C12S pin 12 (BIAS +5VDC) at 50mA maximum is derived from the ISO +12 VDC Power Supply. BIAS +5VDC refers to voltage required for a Line Terminator device.
6. EG (Equipment Ground) pin is electrically connected to the faceplate.
7. LED indicators Tx & Rx for SP3 (field site) and SP5 shall be provided.
8. C1 connector shall be bolted to the Faceplate.
9. Angle Brackets shall support main board to the front panel.
10. Front panel shall be stock Aluminum or Stainless Steel.

TITLE: MODEL 2070-2 FIELD I/O MODULES	
	NO SCALE
TEES 2020	A9-8

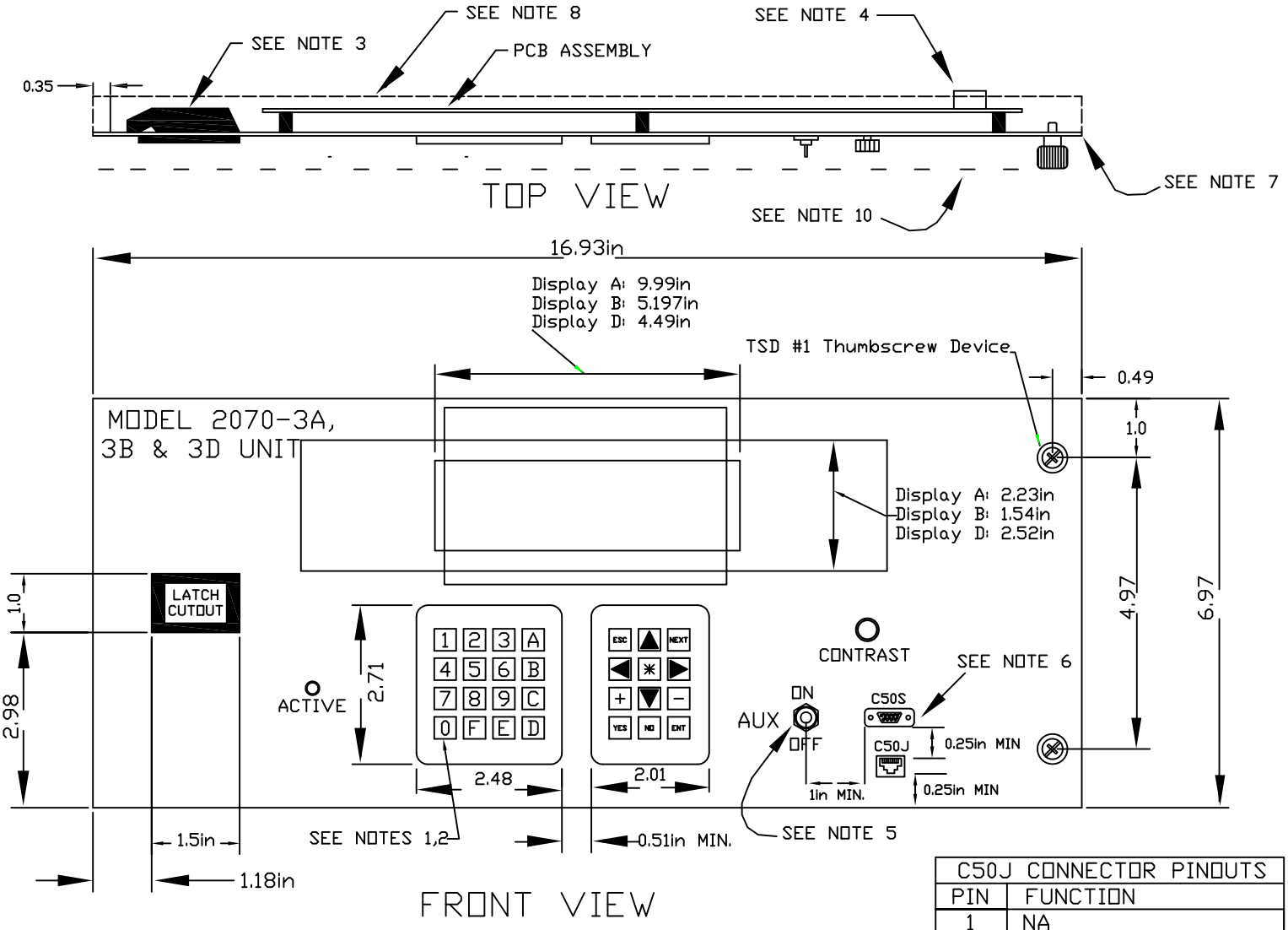
C1S PIN ASSIGNMENT

PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME
1	DCG #2	27	O24	53	I14	79	I44
2	O0	28	O25	54	I15	80	I45
3	O1	29	O26	55	I16	81	I46
4	O2	30	O27	56	I17	82	I47
5	O3	31	O28	57	I18	83	O40
6	O4	32	O29	58	I19	84	O41
7	O5	33	O30	59	I20	85	O42
8	O6	34	O31	60	I21	86	O43
9	O7	35	O32	61	I22	87	O44
10	O8	36	O33	62	I23	88	O45
11	O9	37	O34	63	I28	89	O46
12	O10	38	O35	64	I29	90	O47
13	O11	39	I0	65	I30	91	O48
14	DCG #2	40	I1	66	I31	92	DCG #2
15	O12	41	I2	67	I32	93	O49
16	O13	42	I3	68	I33	94	O50
17	O14	43	I4	69	I34	95	O51
18	O15	44	I5	70	I35	96	O52
19	O16	45	I6	71	I36	97	O53
20	O17	46	I7	72	I37	98	O54
21	O18	47	I8	73	I38	99	O55
22	O19	48	I9	74	I39	100	O36
23	O20	49	I10	75	I40	101	O37
24	O21	50	I11	76	I41	102	O38 DET RES
25	O22	51	I12	77	I42	103	O39 WDT
26	O23	52	I13	78	I43	104	DCG #2

C11S PIN ASSIGNMENT

PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME
1	O56	11	I25	21	I54	31	DCG #2
2	O57	12	I26	22	I55	32	NA
3	O58	13	I27	23	I56	33	NA
4	O59	14	DCG #2	24	I57	34	NA
5	O60	15	I48	25	I58	35	NA
6	O61	16	I49	26	I59	36	NA
7	O62	17	I50	27	I60	37	DCG #2
8	O63	18	I51	28	I61		
9	DCG #2	19	I52	29	I62		
10	I24	20	I53	30	I63		

TITLE:	MODEL 2070-2E+ FIELD I/O MODULE C1S & C11S CONNECTORS
	NO SCALE
TEES 2020	A9-9



NOTES: (FOR THIS DETAIL)

1. Key size shall be (0.3x0.3)in.
2. Key center to center spacing shall be 0.5in.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. The 40 contact connector shall be similar to AMP 102160-9 or equal & compatible to the FP harness in type and pin assignments.
   Center of the FP harness connector shall be vertically positioned (3.54+/-0.197)in as measured fromthe top of the FPA.
   The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
5. Two position LOGIC switch mounted vertically.
6. "C50S" connector shall be a DE-9 socket contact connector. "C50J" shall be a RJ-45 8-position jack. "C60P" connector shall be a DE-9 plug contact connector.
7. Front panel sheet metal thickness shall be (0.06±0.005) in.
8. The FPA shall be provided with a continuous top and bottom 0.63in (inside dimension) lip bent 90 degrees to the front plate and shall extend the full length of the FPA.
9. C60P B Box Power is +5VDC, 350mA max. All signals on C60 P are referenced to isolated interface ground DCG#3.
10. Components shall not protrude beyond the height of the thumbscrews when tightened.
11. See 9.4.1 for components required.
12. All dimensions shown are in inches.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4RXD
3	SP4TXD
4	NA
5	DCG #1
6	NA
7	NA
8	NA
9	NA

C50J CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP4RXD
3	C50 ENABLE
4	NA
5	SP4TXD
6	DCG #1
7	NA
8	NA

C60P CONNECTOR PINOUTS	
PIN	FUNCTION
1	B Box Power, Note 9
2	SP6RXD
3	SP6TXD
4	NA
5	DCG #3
6	NA
7	CPURESET
8	NA
9	CPU LED

TITLE: MODEL 2070-3A, 3B & 3D FRONT PANEL ASSEMBLY	
	NO SCALE
TEES 2020	A9-10

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
	NO SCALE
TEES 2020	A9-11

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 5B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Pn = 0 : Clear Tab at Current Position, Pn = 3 : Clear All Tabs
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 12 h	1B 5B 3F 31 32 68	Heater on
ESC [? 12 l	1B 5B 3F 31 32 6C	Heater off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTES:

1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A 3B & 3D. Command codes shall be available for Option 3C (C60P).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)
ESC [h n	1B 5B 68 6E	ESC [P1 R	1B 5B P1 52	P1: Heater (h,l)
ESC [c	1B 5B 63	ESC [P1 R	1B 5B P1 52	P1; Type (A,B,D)

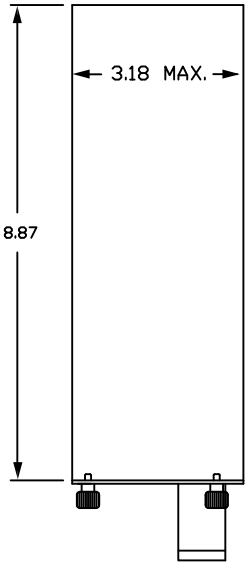
TITLE:

MODEL 2070-3
FRONT PANEL ASSEMBLY
DISPLAY KEY CODES

NO SCALE

TEES 2020

A9-12



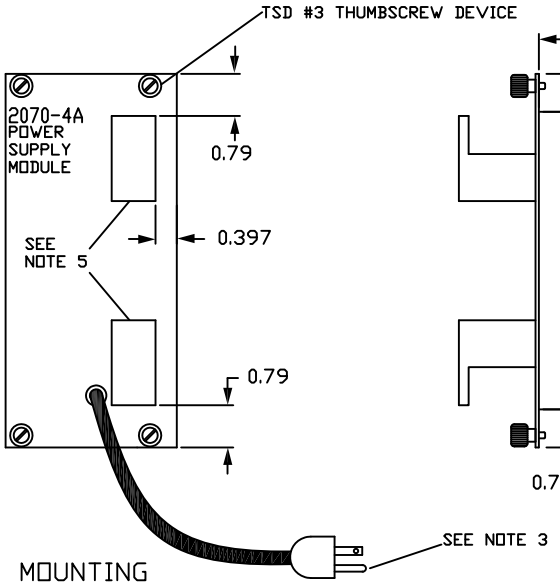
TOP VIEW

PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	+5 VDC SENSE
7	DCG #1 SENSE
8	AC FAIL
9	SYSRESET
10	NA

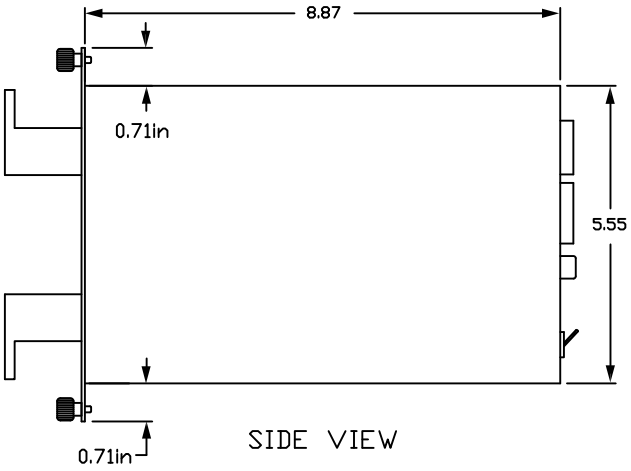
PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISO +12 VDC
7	DCG #2 (ISO +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

NOTES: (FOR THIS DETAIL)

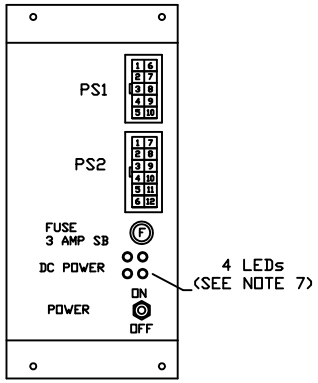
1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three conductor #16 power cable, 4 feet (48 inch) minimum length and permanently attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK 2 CAP Connectors with locking latch devices (OR EQUAL).
   PS1 connector shall be a 10 position PLUG connector.
   PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, ISO +12, +12 SER, -12 SER).
8. Power Supply shall be marked as 2070-4A.
9. The Cord shall be rated for SJT, SJ or Equal,
10. All dimensions shown are in inches.



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



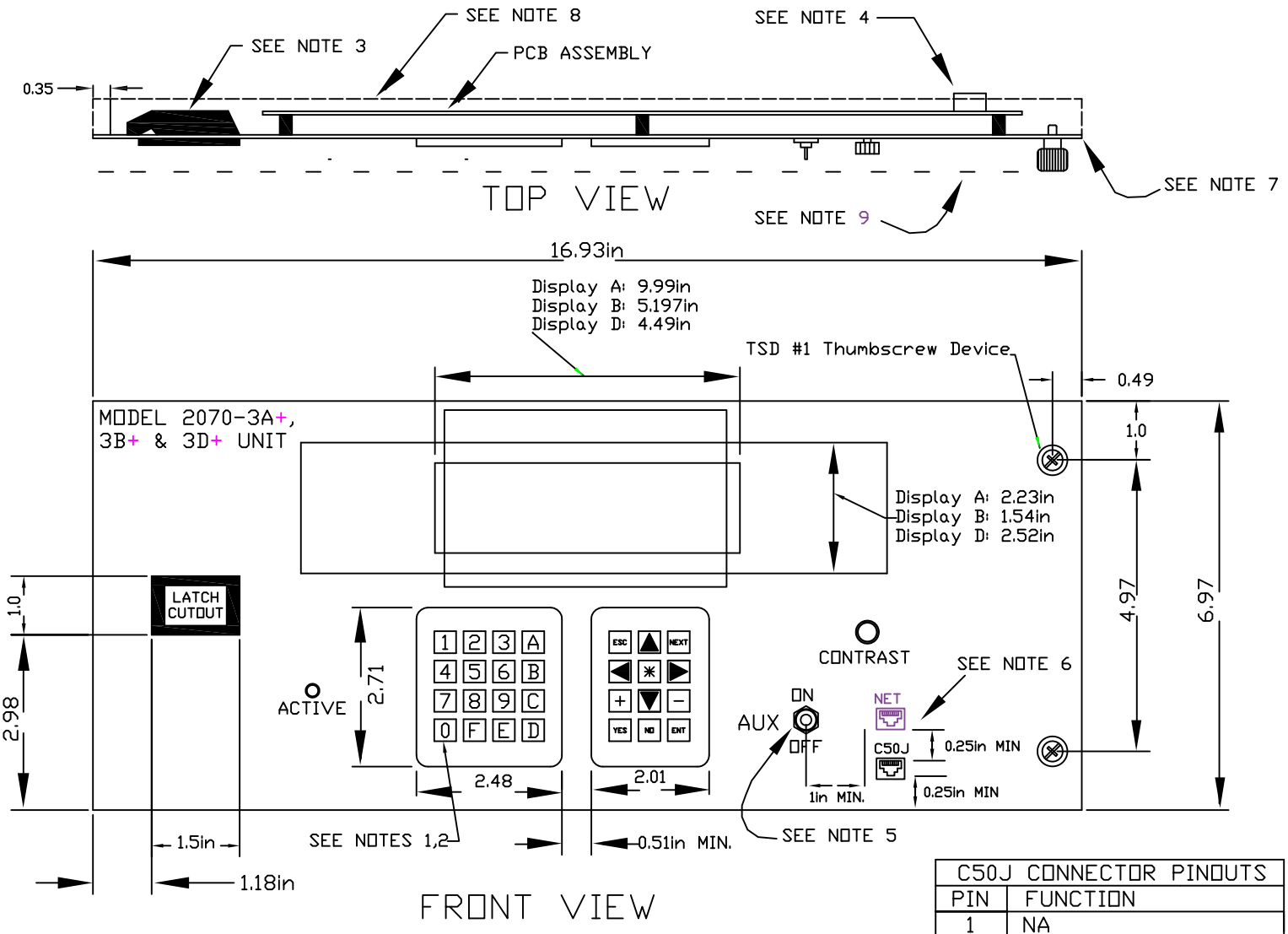
FRONT VIEW

TITLE:
MODEL 2070-4
POWER SUPPLY MODULE

NO SCALE

TEES 2020

A9-13



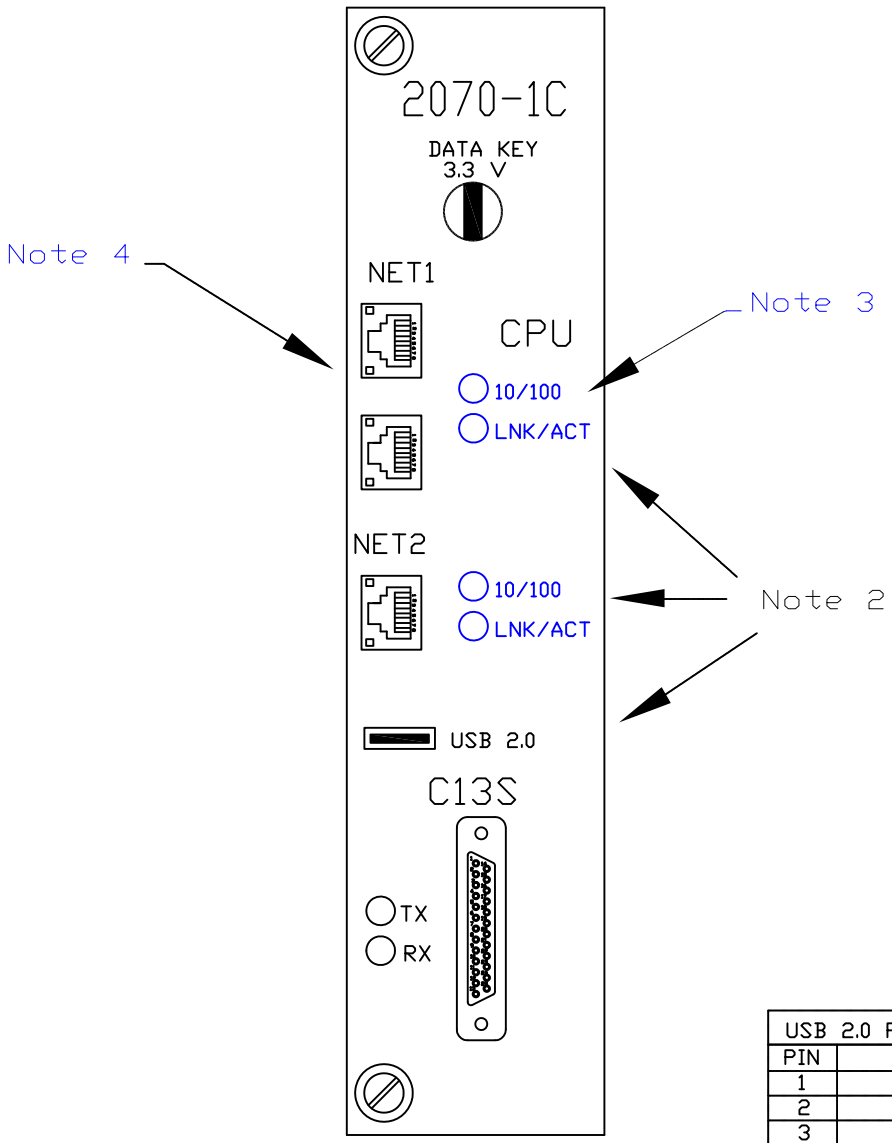
C50J CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP4RXD
3	C50 ENABLE
4	NA
5	SP4TXD
6	DCG #1
7	NA
8	NA

NET CONNECTOR PINOUTS	
PIN	FUNCTION
1	TX +
2	TX -
3	RX +
4	NA
5	NA
6	RX -
7	NA
8	NA

NOTES: (FOR THIS DETAIL)

1. Key size shall be (0.3x0.3)in.
2. Key center to center spacing shall be 0.5in.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. The 40 contact connector shall be similar to AMP 102160-9 or equal & compatible to the FP harness in type and pin assignments.
   Center of the FP harness connector shall be vertically positioned (3.54+/-0.197)in as measured from the top of the FPA.
   The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
5. Two position LOGIC switch mounted vertically.
6. "NET" and "C50J" shall be RJ-45 8-position jack.
7. Front panel sheet metal thickness shall be (0.06±0.005) in.
8. The FPA shall be provided with a continuous top and bottom 0.63in (inside dimension) lip bent 90 degrees to the front plate and shall extend the full length of the FPA.
9. Components shall not protrude beyond the height of the thumbscrews when tightened.
10. See 9.4.1 for components required.
11. All dimensions shown are in inches.

TITLE: MODEL 2070-3A+, 3B+ & 3D+ FRONT PANEL ASSEMBLY	
	NO SCALE
TEES 2020	A9-14



USB 2.0 PIN ASSIGNMENT	
PIN	FUNCTION
1	VCC
2	DATA-
3	DATA+
4	GND

NET1 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NET2 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

NOTES: (FOR THIS DETAIL)

1. BIAS +5VDC refers to voltage required for a Line Terminator device.
2. NET1, NET2, USB & C13S should be placed within the area as shown.
3. LED indicators between switch & CPU.
4. All RJ-45 connectors shall contain LED indicators 10/100 & LNK/ACT.
5. Front panel shall be Aluminum stock or Stainless Steel.

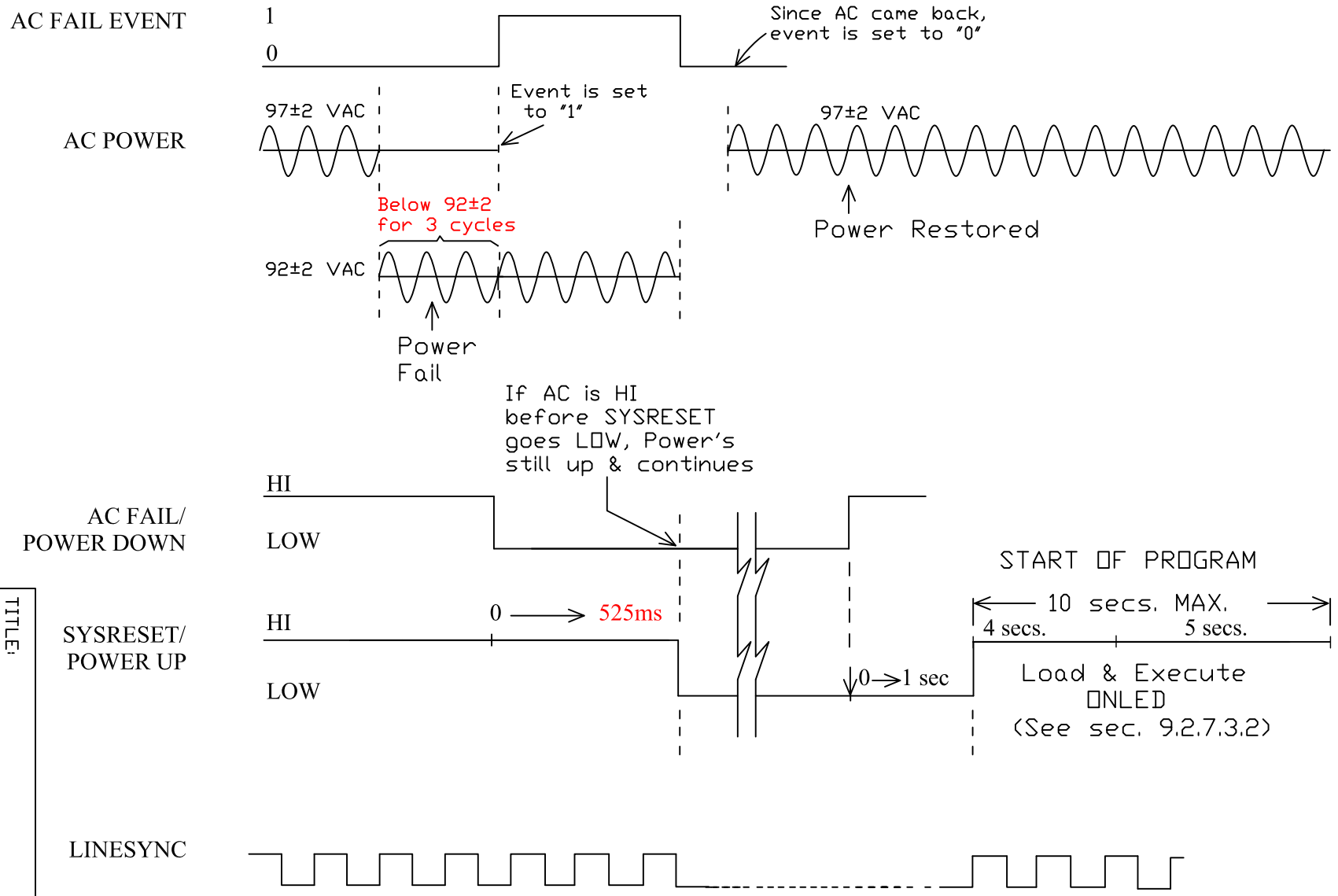
TITLE: MODEL 2070-1C CPU	
	NO SCALE
TEES 2020	A9-15

SERIAL PORT DESCRIPTORS DEFAULTS			
SP1, SP2, SP3 and SP5	SP4	SP6	SP8
noupc	noupc	noupc	noupc
bsb	bsb	bsb	bsb
bsl	bsl	bsl	bsl
noecho	echo	echo	noecho
lf	lf	lf	lf
null=0	null=0	null=0	null=0
nopause	nopause	nopause	nopause
pag=24	pag=24	pag=24	pag=24
bsp=08	bsp=08	bsp=08	bsp=08
del=18	del=18	del=18	del=18
eor=0D	eor=0D	eor=0D	eor=0D
eof=1B	eof=1B	eof=1B	eof=1B
reprint=04	reprint=04	reprint=04	reprint=04
dup=01	dup=01	dup=01	dup=01
psc=17	psc=17	psc=17	psc=17
abort=03	abort=03	abort=03	abort=03
quit=05	quit=05	quit=05	quit=05
bse=08	bse=08	bse=08	bse=08
bell=07	bell=07	bell=07	bell=07
type=00	type=00	type=00	type=00
baud=1200	baud=9600	baud=38400	baud=9600
xon=11	xon=00	xon=11	xon=11
xoff=13	xoff=00	xoff=13	xoff=13
tabc=09	tabc=09	tabc=09	tabc=09
tabs=4	tabs=4	tabs=04	tabs=04

NOTES: (FOR THIS DETAIL)

1. All serial port descriptors shall be set with 8 Bit Word, 1 Stop & no Parity.
2. Model 2070-1C sp4 shall be set to 115.2 Kbps.
3. sp3s & sp5s shall be set to 614.4 Kbps.

TITLE: SERIAL PORT DESCRIPTORS DEFAULTS	
	NO SCALE
TEES 2009	A9-16



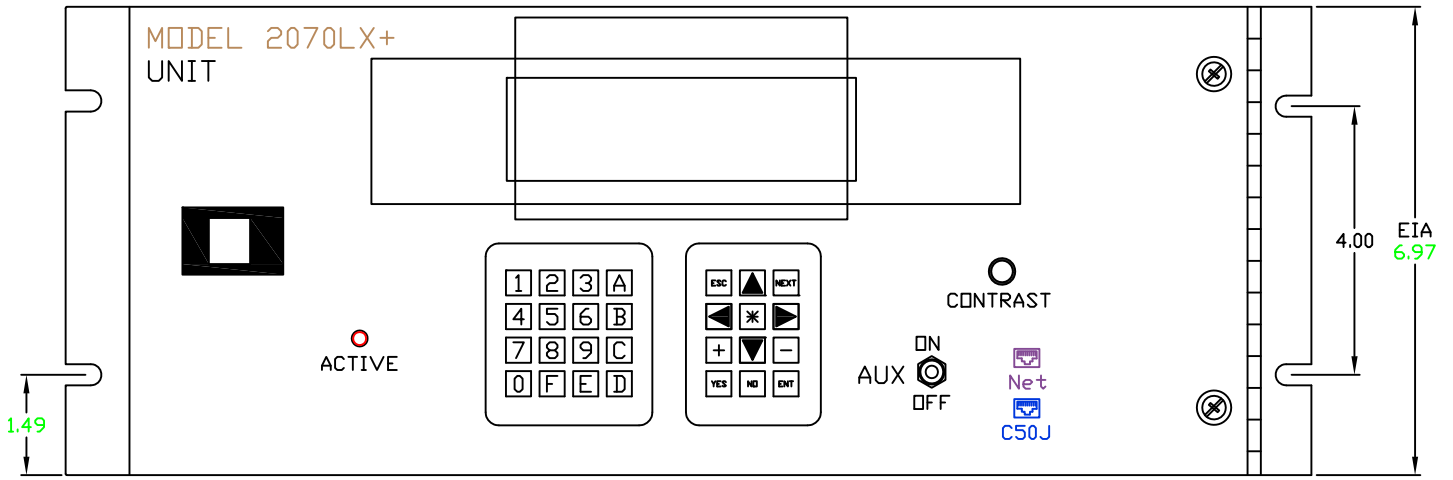
NOTES:

Power Failure: A Power Failure is said to have occured when the incoming line voltage falls below 92+/−2 VAC for 50ms. See Power Conditions.

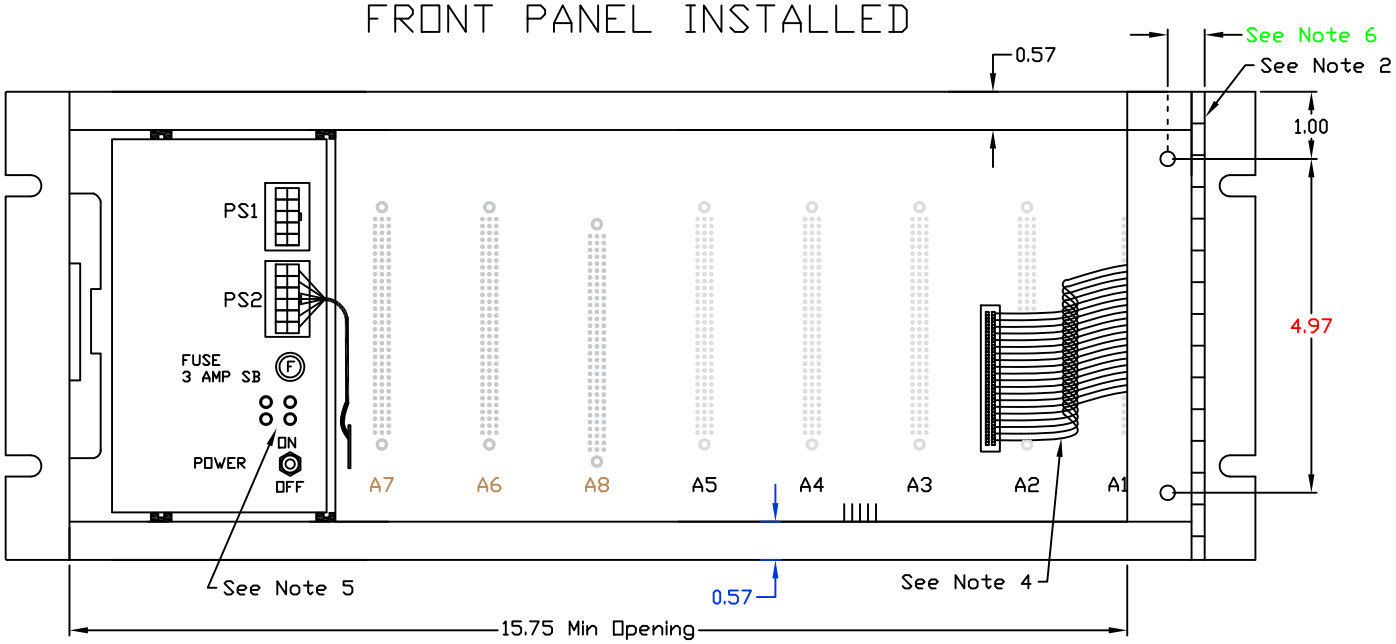
Power Restoration: Power is said to be restored when the incoming line voltage equals or exceeds 97+/−2 VAC for 50ms. See Power Conditions.

Power Conditions: A 16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (67 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.

TEES 2020	TITLE: MODEL 2070 POWER FAILURE REACTION
NO SCALE	
A9-17	



FRONT PANEL INSTALLED

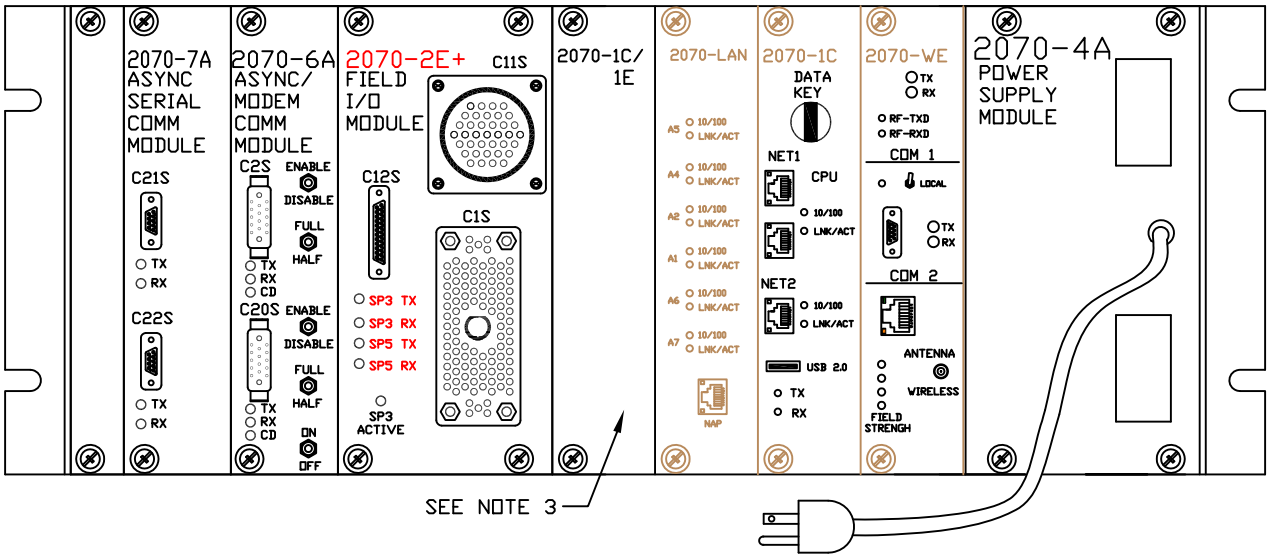


FRONT PANEL REMOVED

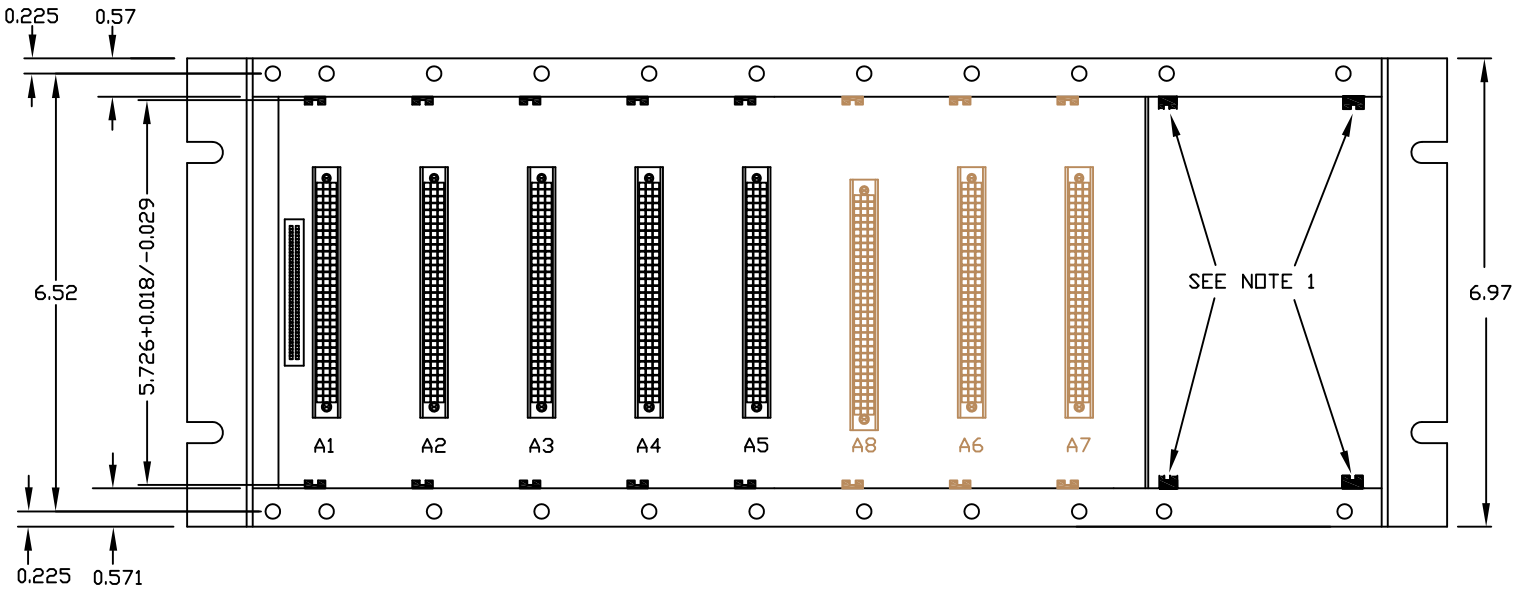
NOTES: (FOR THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA–310B Rack using 4U open end mounting slots.
2. Continuous stainless steel hinge (0.157in maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.
3. Actual location of ACTIVE light, AUX switch, C50J, Net and contrast control shall be limited to ACTIVE light on the left side of the panel; AUX switch, C50J, Net and the contrast control on the right side. They shall be located greater than 1 in from the edge of each other, other devices, connector or latch. Net only needs to be 0.25in minimum from C50J.
4. The length of the Front Panel Harness shall be 5in + 2% and it shall be removable.
5. LED indicators for each DC voltage shall be provided.
6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside plane) shall be 0.55in.
7. All dimensions shown are in inches.

TITLE: MODEL 2070LX+ CHASSIS FRONT VIEW	
	NO SCALE
TEES 2020	A9-18



REAR VIEW, LOADED

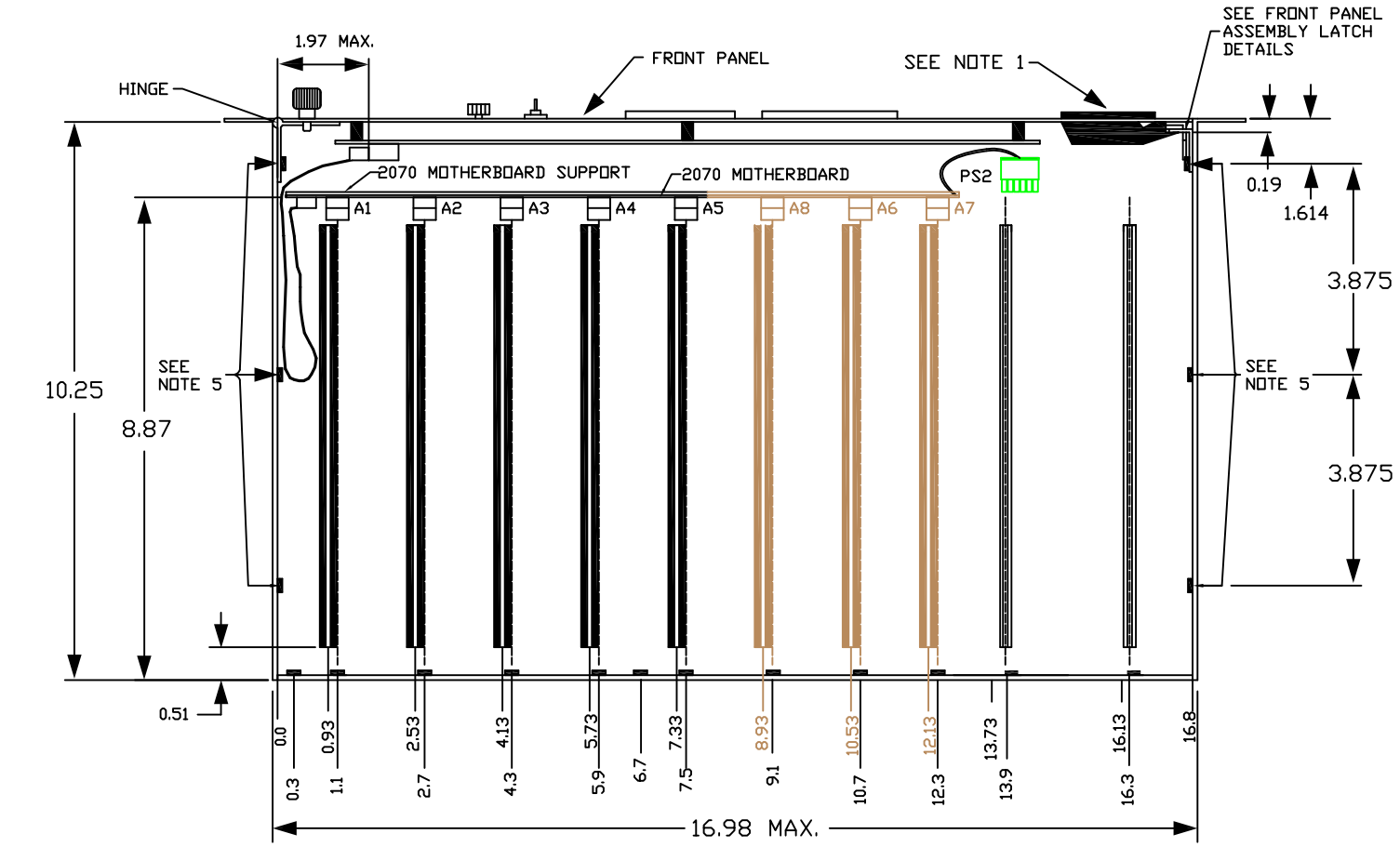


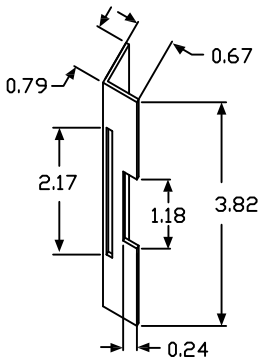
REAR VIEW, UNLOADED

NOTES: (FOR THIS DETAIL)

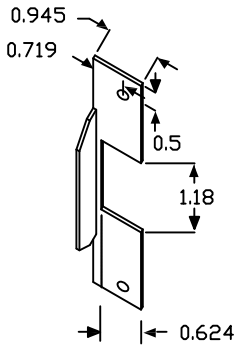
1. Four permanently attached 8in long Card Guides SAE 1800F (OR EQUAL) beginning 0.51in from the backplane mounting surface.
2. Blank plates shall cover all unused module openings.
3. All Module Front Plates thickness shall be (0.08±0.005)
4. All dimensions shown are in inches.

TITLE: MODEL 2070LX+ CHASSIS REAR VIEW	
	NO SCALE
TEES 2020	A9-19

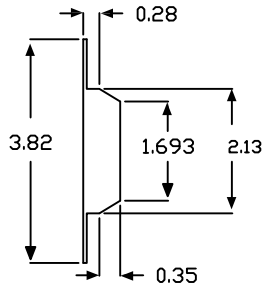




CHASSIS BRACKET
(Thickness is 0.06)



FRONT PANEL BRACKET



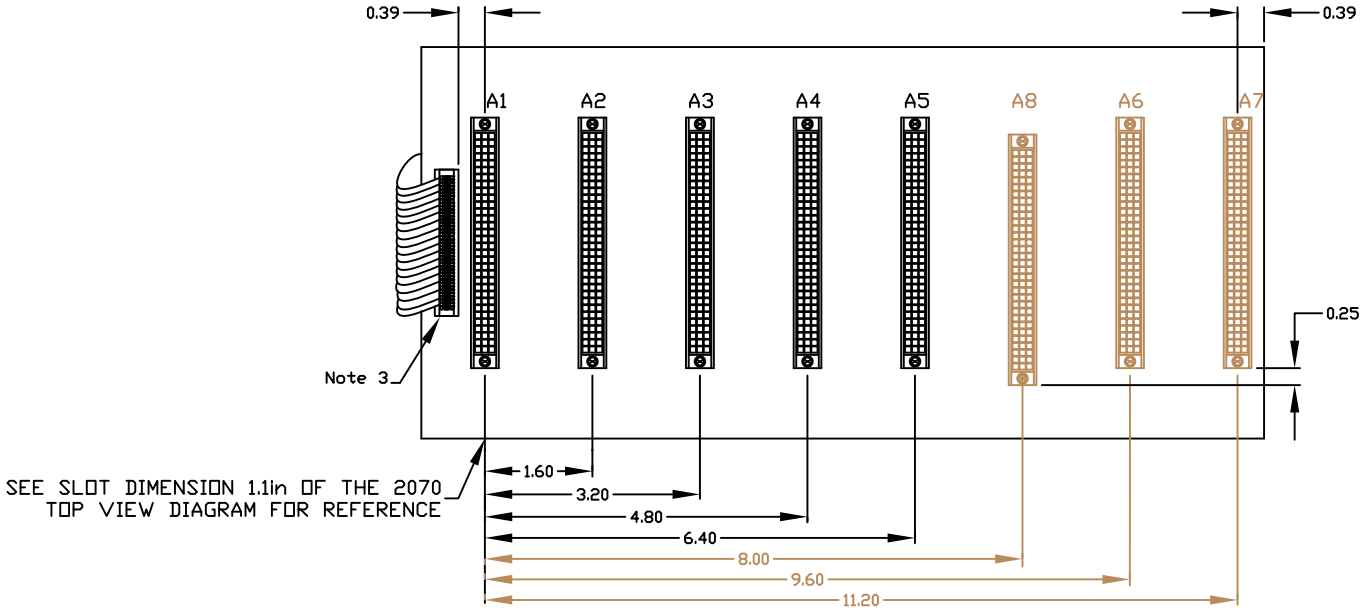
SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

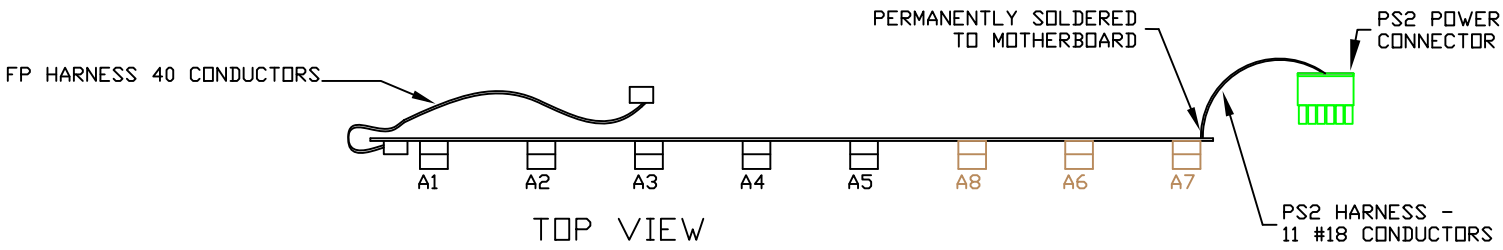
NOTES: (FOR THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A7. The Guides shall begin 0.51 inch from the Backplane outside surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 1 inch when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 0.25 inch above unit baseline.
6. The 2070 chassis top & bottom sections shall be constructed with a continuous 0.571 inch folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 0.71 inch as measured from the front surface of the front panel.
7. Chassis side plates shall be 0.090in thick.
8. All dimensions shown are in inches.

TITLE:	MODEL 2070LX+ CHASSIS TOP VIEW
	NO SCALE
TEES 2020	A9-20



CONNECTOR VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4TXD+	2	SP4TXD-
3	SP4RXD+	4	SP4RXD-
5	SP6TXD+	6	SP6TXD-
7	SP6RXD+	8	SP6RXD-
9	DCG#1	10	DCG#1
11	NetFP1-TX-	12	NetFP1-TX+
13	DCG#1	14	DCG#1
15	NetFP1-RX-	16	NetFP1-RX+
17	NETLINKACT	18	NetPWR
19	NETSPEED	20	DCG#1
21	DCG #1	22	DCG #1
23	+12 VDC SER	24	-12 VDC SER
25	DCG #1	26	DCG #1
27	CPU LED	28	DCG #1
29	CPURESET	30	DCG #1
31	DCG #1	32	C50 ENABLE
33	DCG #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISO +12 VDC
7	DCG #2 (ISO +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

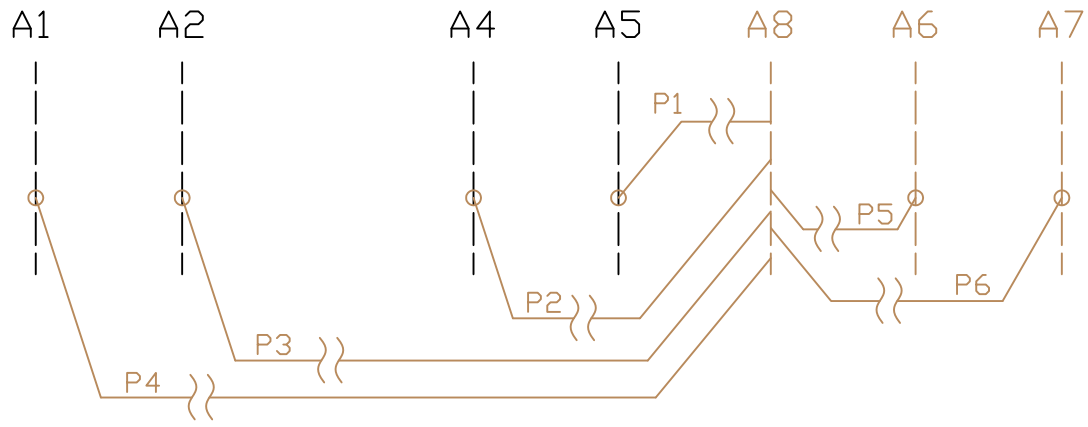
NOTES: (FOR THIS DETAIL)

1. The Motherboard shall be a 0.125 inch minimum thickness pcb mechanically mounted in a vertical position.
2. A1 to A7 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).
3. The FP Harness shall be connected to the Motherboard via a header connector. Pin 1 shall be in the lower right hand corner.
4. Front Panel Harness Connector shall intermate with AMP 102-160-9 or equal located on Front Panel PCB.
5. Angle Brackets shall support the Motherboard to the Model 2070 chassis.
6. All dimensions shown are in inches.

TITLE: MODEL 2070LX+ CHASSIS MOTHERBOARD	
	NO SCALE
TEES 2020	A9-21

A6 TO A7 CONNECTOR PINOUT			
PIN	A	B	C
1	NA	NA	NA
2	NA	NA	NA
3	NA	NA	NA
4	NA	NA	NA
5	NA	NA	NA
6	NA	NA	NA
7	NA	NA	NA
8	NA	NA	NA
9	NA	NA	NA
10	NA	NA	NA
11	NA	NA	NA
12	NA	NA	NA
13	NA	NA	NA
14	NA	NA	NA
15	NA	NA	NA
16	NA	NA	NA
17	NA	NA	NA
18	NA	NA	NA
19	NA	NA	NA
20	NA	NA	NA
21	DCG #1	NA	NA
22	NetP5 (TX+)	NA	NA
23	NetP5 (TX-)	NA	NA
24	NA	LINESYNC	NA
25	NetP5 (RX+)	POWERUP	NA
26	NetP5 (RX-)	POWERDOWN	NA
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

NETWORK SWITCH PORT CONNETOR PIN OUT	
Port 1	A5 Conn Pinout
TX+	22
TX-	23
RX+	25
RX-	26
Port 2	A4 Conn Pinout
TX+	22
TX-	23
RX+	25
RX-	26
Port 3	A2 Conn Pinout
TX+	22
TX-	23
RX+	25
RX-	26
Port 4	A1 Conn Pinout
TX+	22
TX-	23
RX+	25
RX-	26
Port 5	A6 Conn Pinout
TX+	22
TX-	23
RX+	25
RX-	26
Port 6	A7 Conn Pinout
TX+	22
TX-	23
RX+	25
RX-	26



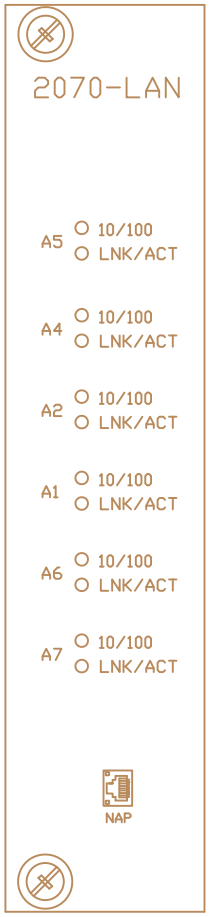
Network Connections A1, A2, A4, A5, A6, A7 & A8

NOTES: (FOR THIS DETAIL)

1. Functions are referenced to CPU.

TITLE: MODEL 2070LX+ NETWORK MOTHERBOARD CONNECTOR PINOUT	
	NO SCALE
TEES 2020	A9-22

A8 CONNECTOR PINOUT			
PIN	A	B	C
1	DCG #1	DCG #1	DCG #1
2	Netwk1-A1	NA	Netwk3-A1
3	Netwk2-A1	NA	Netwk4-A1
4	DCG #1	DCG #1	DCG #1
5	Netwk1-A2	NA	Netwk3-A2
6	Netwk2-A2	NA	Netwk4-A2
7	DCG #1	DCG #1	DCG #1
8	Netwk1-A4	NA	Netwk3-A4
9	Netwk2-A4	NA	Netwk4-A4
10	DCG #1	DCG #1	DCG #1
11	Netwk1-A5	NA	Netwk3-A5
12	Netwk2-A5	NA	Netwk4-A5
13	DCG #1	DCG #1	DCG #1
14	Netwk1-A6	NA	Netwk3-A6
15	Netwk2-A6	NA	Netwk4-A6
16	DCG #1	DCG #1	DCG #1
17	Netwk1-A7	NA	Netwk3-A7
18	Netwk2-A7	NA	Netwk4-A7
19	DCG #1	DCG #1	DCG #1
20	Netwk1-FP	NA	Netwk3-FP
21	Netwk2-FP	NA	Netwk4-FP
22	DCG #1	DCG #1	DCG #1
23	NETLINKACT	NETSPEED	NETPWR
24	NA	LINESYNC	NA
25	NA	POWERUP	CPU RESET
26	DCG #1	POWERDOWN	DCG #1
27	SP6RX+OUT	SP6TX+	SP6RX+IN
28	SP6RX-OUT	SP6TX-	SP6RX-IN
29	PS2-12	NA	NA
30	+5VDC	+5VDC	+5VDC
31	+5VDC	+5VDC	+5VDC
32	DCG #1	DCG #1	DCG #1

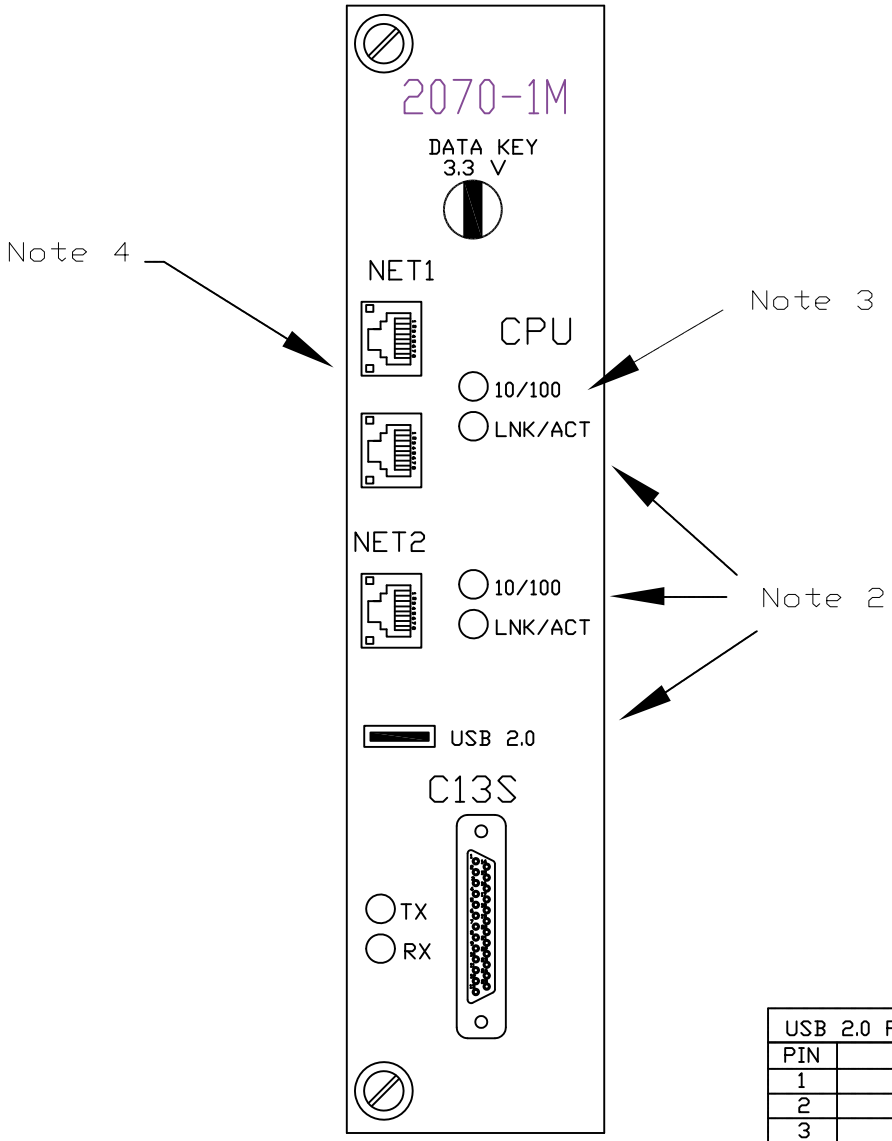


LED Indicators

NOTES: (FOR THIS DETAIL)

1. Functions are referenced to CPU.

TITLE: MODEL 2070-LAN MODULE CONNECTOR PINOUT	
	NO SCALE
TEES 2020	A9-23



USB 2.0 PIN ASSIGNMENT	
PIN	FUNCTION
1	VCC
2	DATA-
3	DATA+
4	GND

NET1 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NET2 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

NOTES: (FOR THIS DETAIL)

1. BIAS +5VDC refers to voltage required for a Line Terminator device.
2. NET1, NET2, USB & C13S should be placed within the area as shown.
3. LED indicators between switch & CPU.
4. All RJ-45 connectors shall contain LED indicators 10/100 & LNK/ACT.
5. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 2070-1M CPU	
	NO SCALE
TEES 2020	A9-24

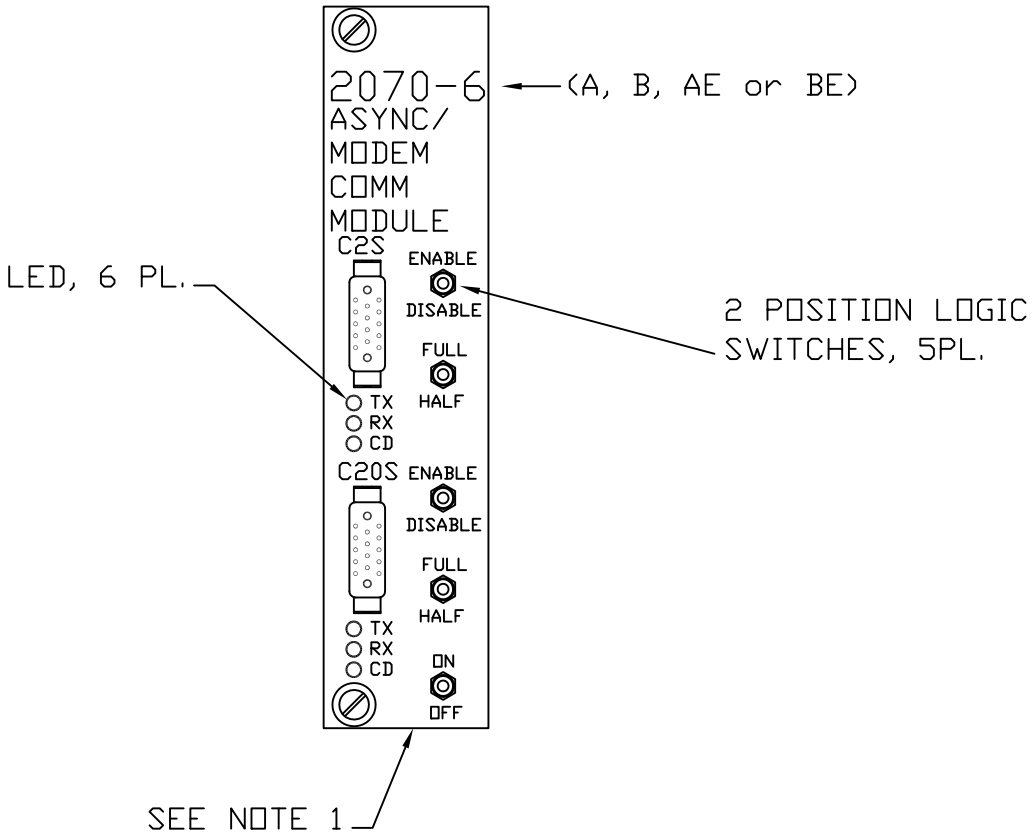
APPENDIX A10
CHAPTER 10 DETAILS

GENERAL NOTES

The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable channel 2 via disabling the RS-485 signals to and from the motherboard.

The Disable line shall be pulled up on the module**.** Line drivers/receivers shall be socket or surface mounted.

Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps. The Comm modules shall be "Hot" swappable without damage to circuitry or operations.

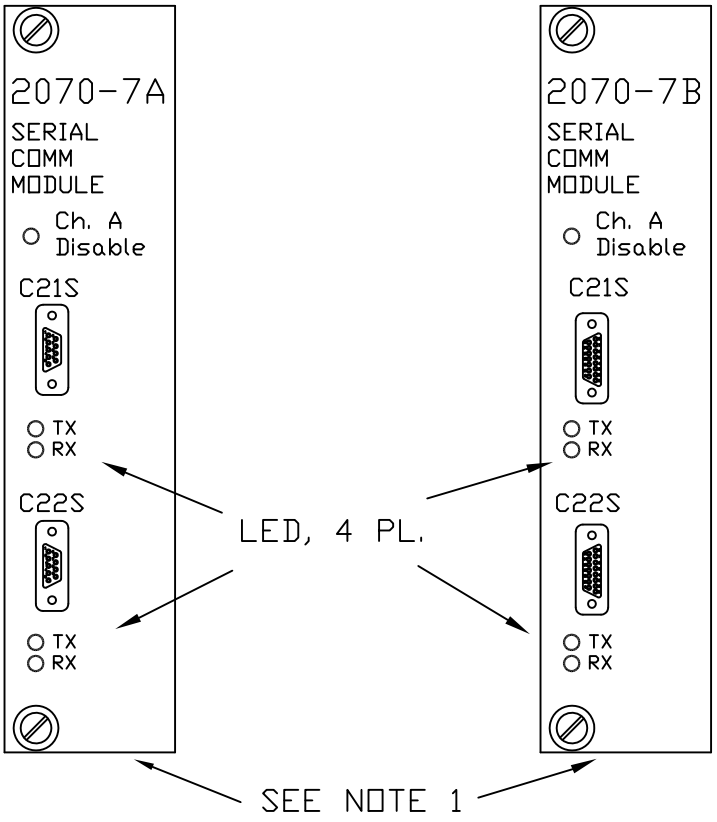


C2S & C20S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	RXD
C	AUDIO OUT	L	TXD
D	IFC +5 VDC	M	CTS
E	AUDIO OUT	N	IFC GND
F	NA	P	NA
H	DCD	R	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.
3. IFC (Interface) Power and Ground is isolated from the internal ground system & is the voltage reference for the EIA-232 signals also.
4. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 2070-6A, 6B, 6AE, 6BE ASYNC/MODEM SERIAL COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-1

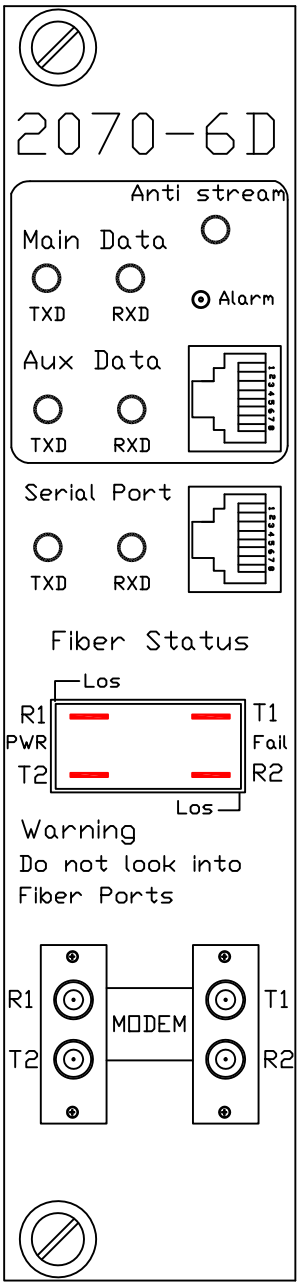


2070-7A (DE-9S)	
C21S & C22S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DA-15S)			
C21S & C22S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TXD+	9	TXD-
2	IFC GND	10	IFC GND
3	TXC+	11	TXC-
4	IFC GND	12	IFC GND
5	RXD+	13	RXD-
6	IFC GND	14	IFC GND
7	RXC+	15	RXC-
8	NA		

NOTES: (FOR THIS DETAIL)
1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. Connectors 21 & 22 are DE 9S for Module 7A & DA 15S for Module 7B.
3. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.
4. On 2070-7B, SPxRTS shall enable/disable TXD+/- & TXCO+/-
5. TXC is jumper selectable to be either TXCO or TXCI.
6. Channel A denotes C21S and Channel B denotes C22S.
7. Front panel shall be Aluminum stock or Stainless Steel.

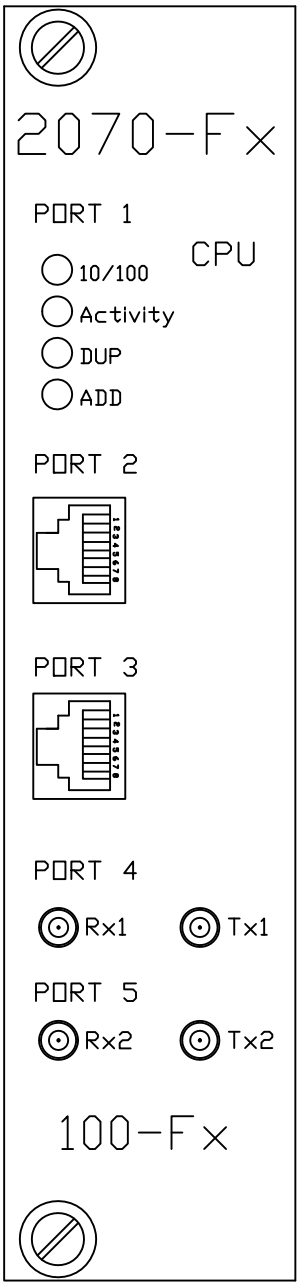
TITLE: MODEL 2070-7A, 7B ASYNC/SYNC SERIAL COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-2



AUX. PORT PIN OUT ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	N/C	5	RXD
2	DCD/KOD	6	TXD
3	N/C	7	CTS
4	GND	8	RTS

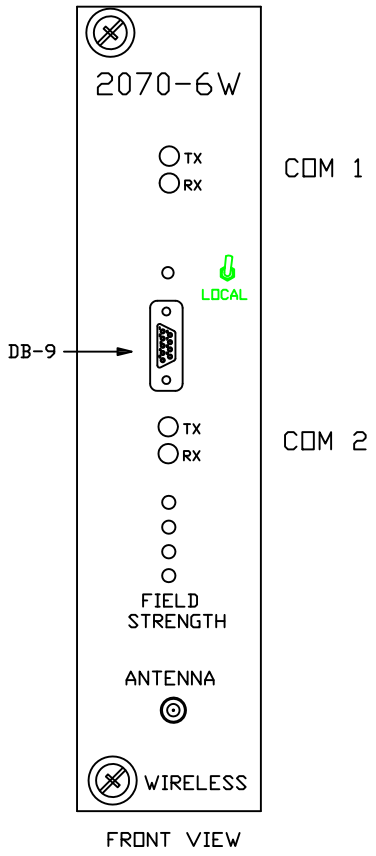
SERIAL PORT PIN OUT ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	+5 VDC	5	RXD
2	DCD	6	TXD
3	N/C	7	CTS
4	GND	8	RTS

TITLE: MODEL 2070 6D FIBER OPTICS MODEM COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-3



PORT 2 & 3 RJ45 PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

TITLE: MODEL 2070-Fx FIBER OPTICS NETWORK COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-4

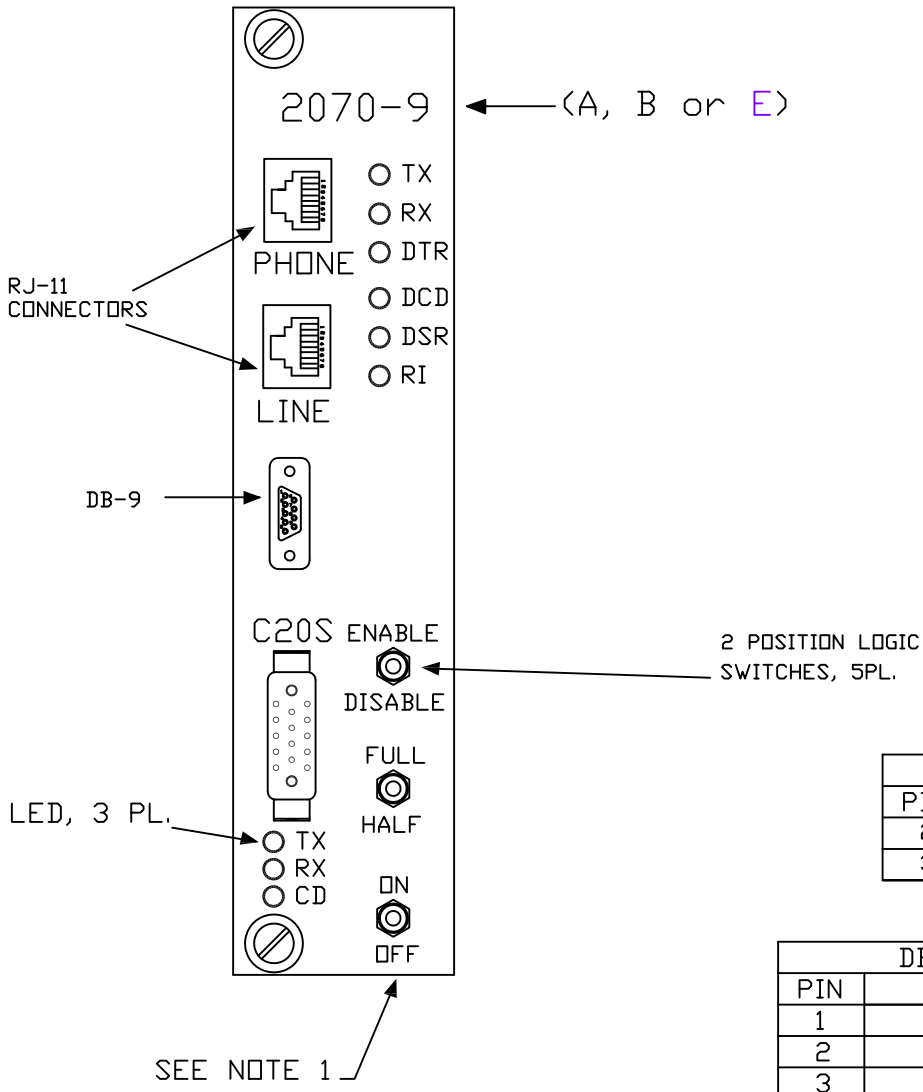


2070-6W (DB-9)	
C21S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.

TITLE: MODEL 2070-6W WIRELESS MODEM COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-5



RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

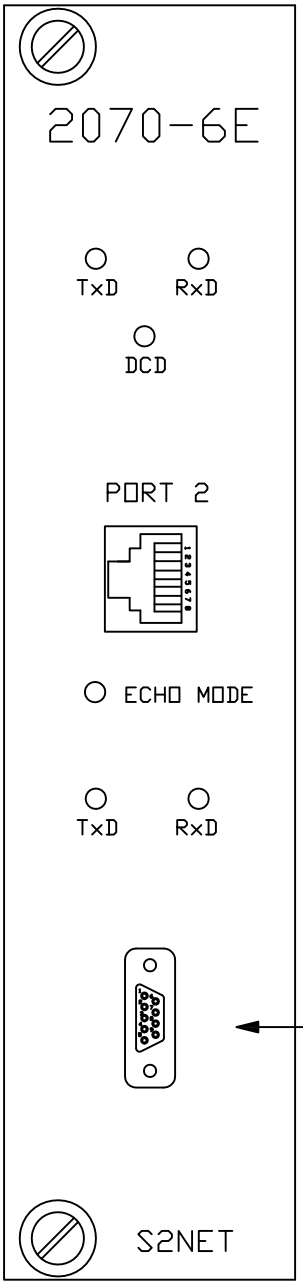
DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6). Front panel shall be Aluminum stock or Stainless Steel.
2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.
3. IFC (Interface) Power and Ground is isolated from the internal ground system and is the voltage reference for the EIA-232 signals also.

C20S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	RXD
C	AUDIO OUT	L	TXD
D	IFC +5 VDC	M	CTS
E	AUDIO OUT	N	IFC GND
F	NA	P	NA
H	DCD	R	NA

TITLE: MODEL 2070-9A, 9B, 9E FSK/DIAL UP MODEM COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-6



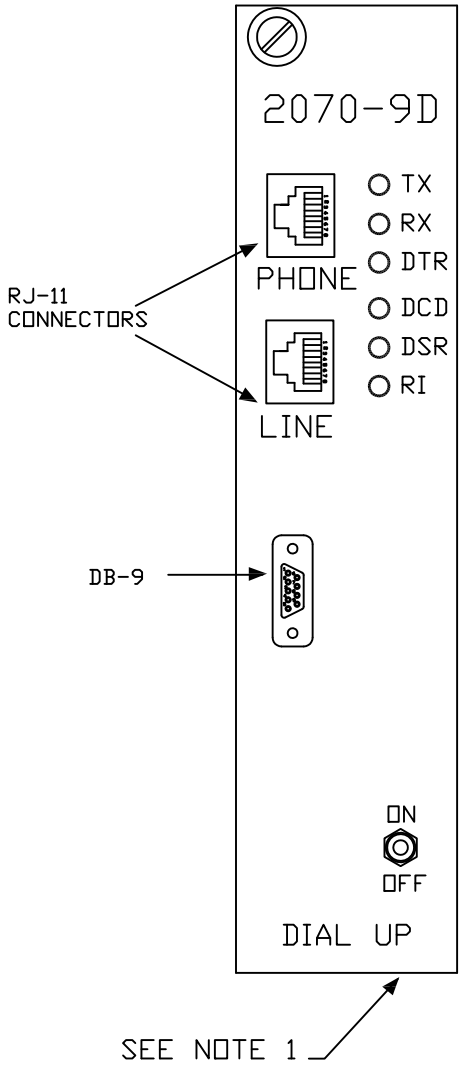
RJ45 ETHERNET PIN ASSIGNMENT	
PIN	FUNCTION
1	TX +
2	TX -
3	RX +
4	RX -
5	NA
6	NA
7	NA
8	NA

DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6). Front panel shall be Aluminum stock or Stainless Steel.
2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.

TITLE: MODEL 2070-6E SERIAL 2 NETWORK COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-7



RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

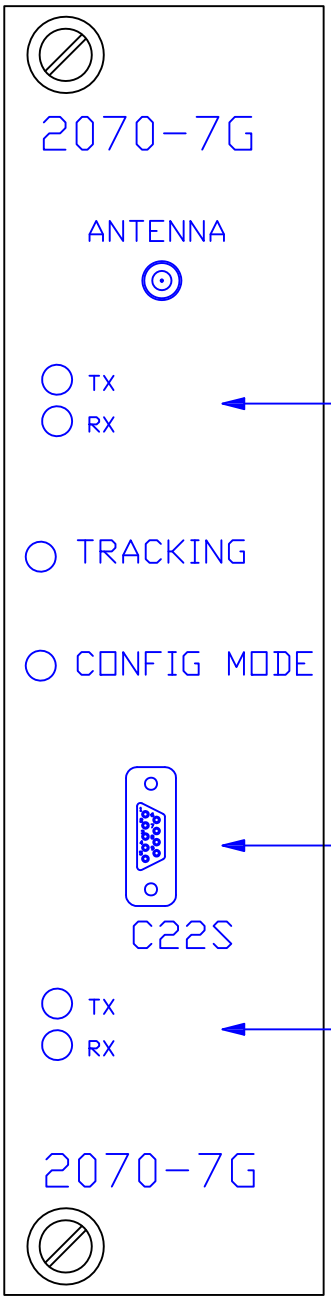
DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6). Front panel shall be Aluminum stock or Stainless Steel.

2. IFC (Interface) Power and Ground is isolated from the internal ground system & is the voltage reference for the EIA-232 signals also.

TITLE: MODEL 2070-9D DIAL UP MODEM COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-8

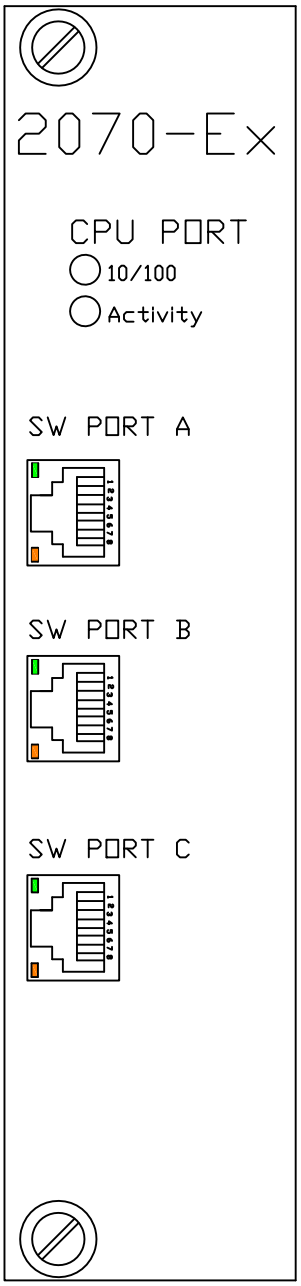


DB9 - PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	GND
6	NA
7	RTS
8	CTS
9	NA

NOTES: (FOR THIS DETAIL)

1. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 2070-7G UNIVERSAL TIME BASE MODULE	
	NO SCALE
TEES 2020	A10-9



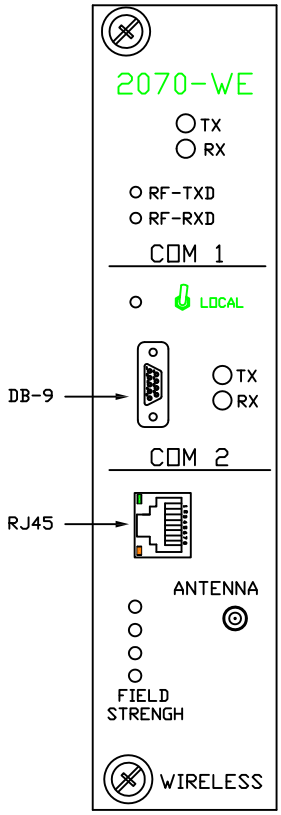
PORT 2, 3, 4 RJ45 PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

1. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 2070-Ex NETWORK SWITCH MODULE	
	NO SCALE
TEES 2020	A10-10

WIRELESS ETHERNET COMM MODULE



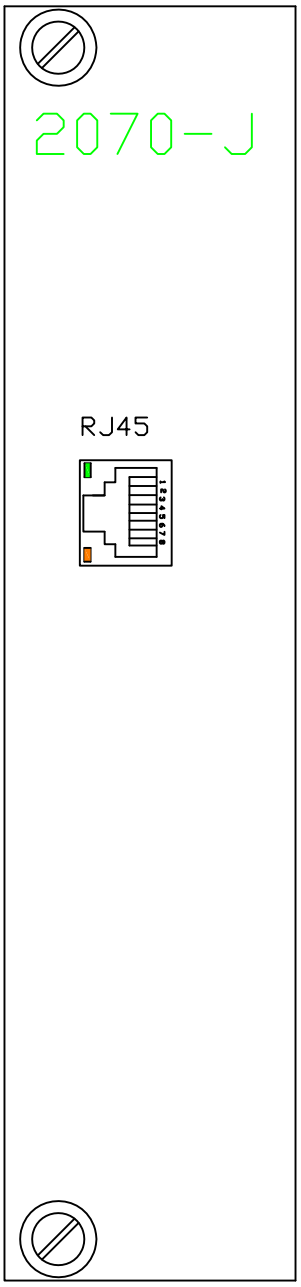
FRONT VIEW

2070-WE (DB-9)	
C21S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.
3. WE = Wireless Ethernet

TITLE: MODEL 2070-WE WIRELESS ETHERNET COMMUNICATION MODULE	
	NO SCALE
TEES 2020	A10-11

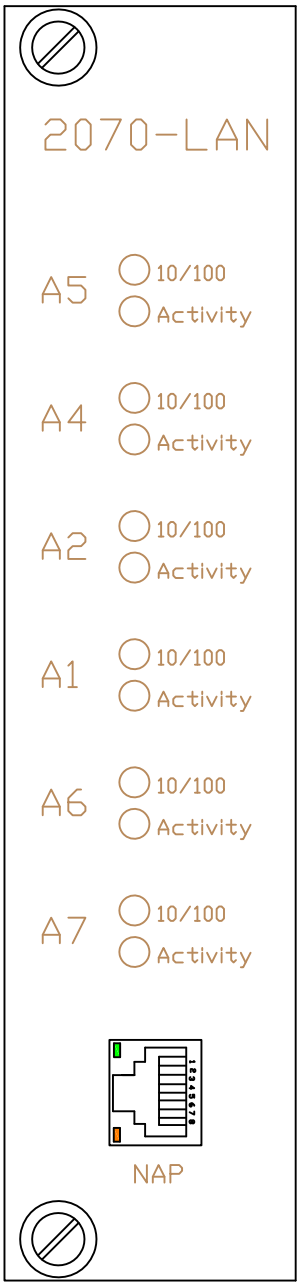


RJ45 PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

1. Front panel shall be Aluminum stock or Stainless Steel.

TITLE: MODEL 2070-J NETWORK JACK MODULE	
	NO SCALE
TEES 2020	A10-12

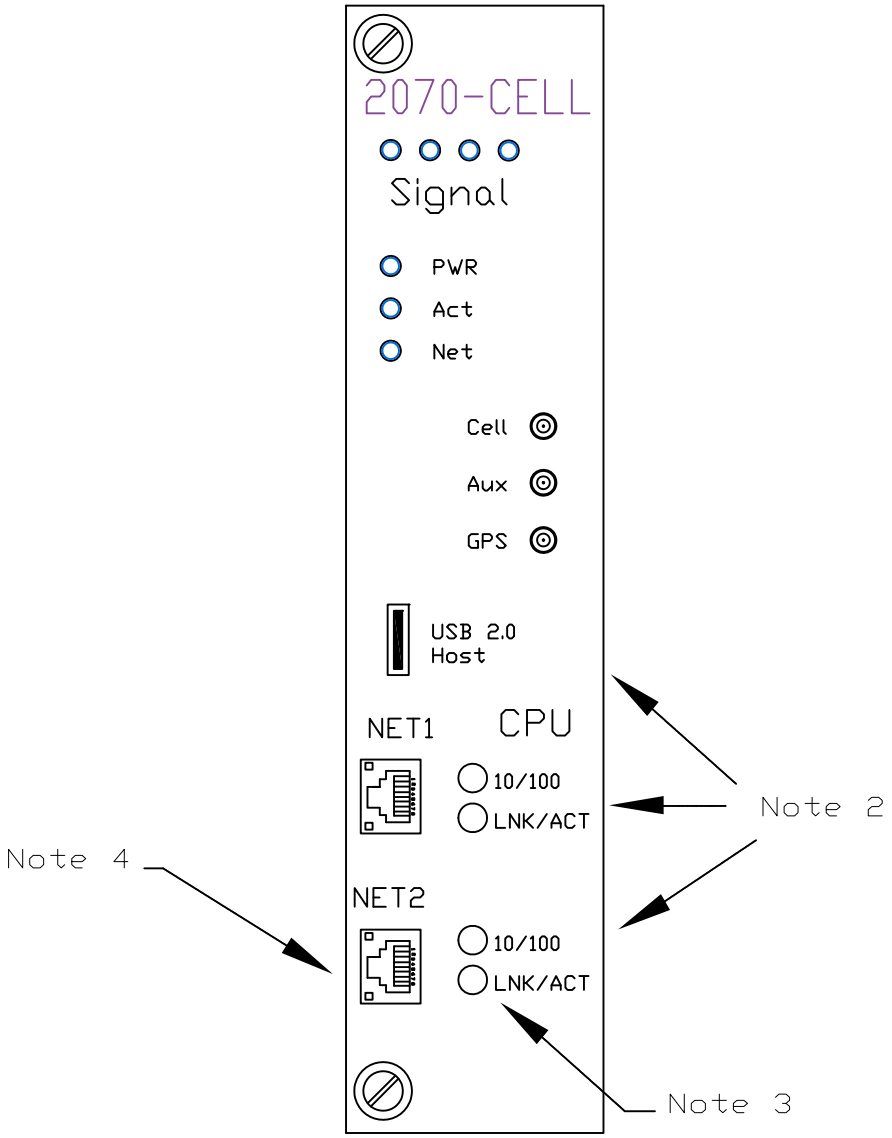


NAP		RJ45 PIN ASSIGNMENTS	
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

1. Network Access Port (NAP).

TITLE: MODEL 2070-LAN 2070 Local Area Network Module	
	NO SCALE
TEES 2020	A10-13



USB 2.0 PIN ASSIGNMENT	
PIN	FUNCTION
1	VCC
2	DATA-
3	DATA+
4	GND

NET1 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NET2 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

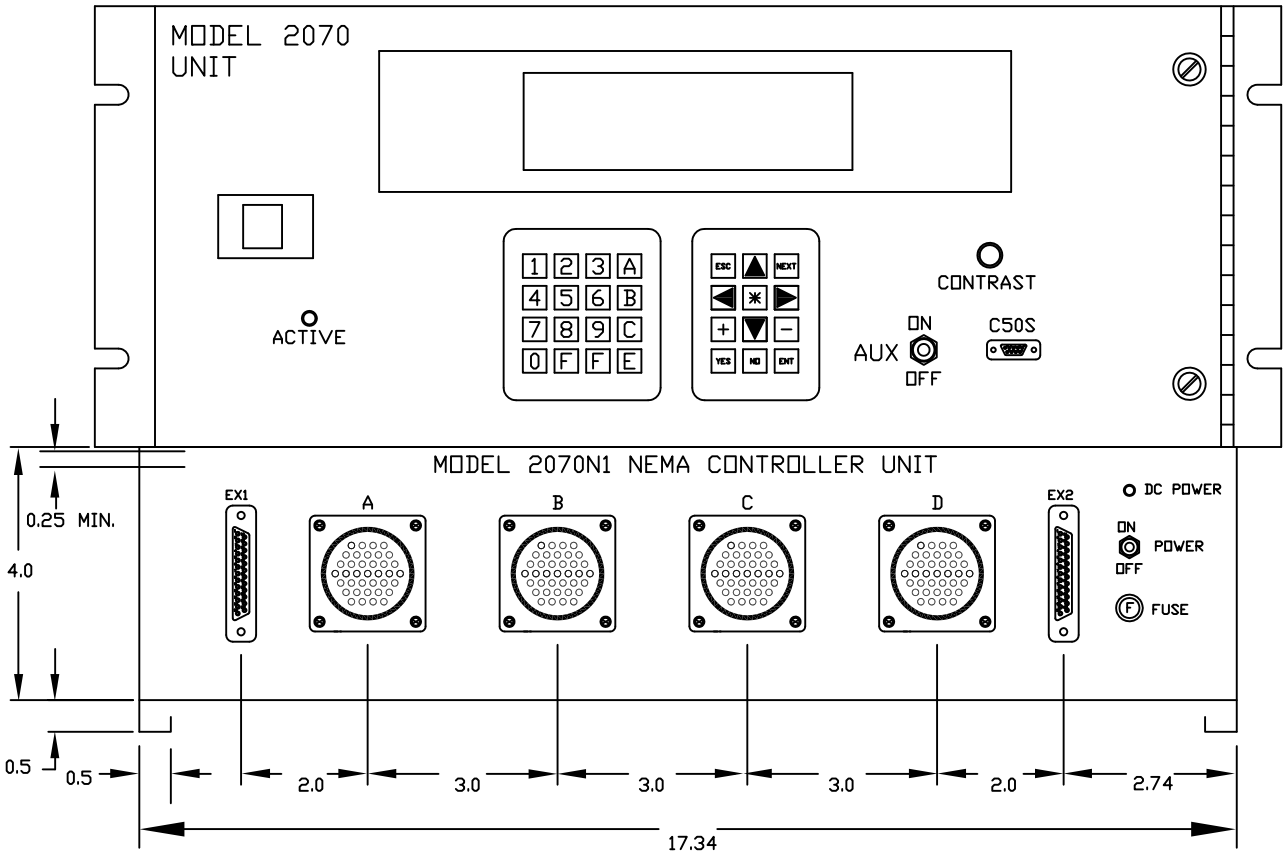
1. BIAS +5VDC refers to voltage required for a Line Terminator device.
2. NET1, NET2, & USB should be placed within the area as shown.
3. LED indicators between switch & CPU.
4. All RJ-45 connectors shall contain LED indicators 10/100 & LNK/ACT.
5. Front panel shall be Aluminum stock or Stainless Steel.

TITLE:

MODEL 2070-CELL
Cellular Comm Module

	NO SCALE
TEES 2020	A10-14

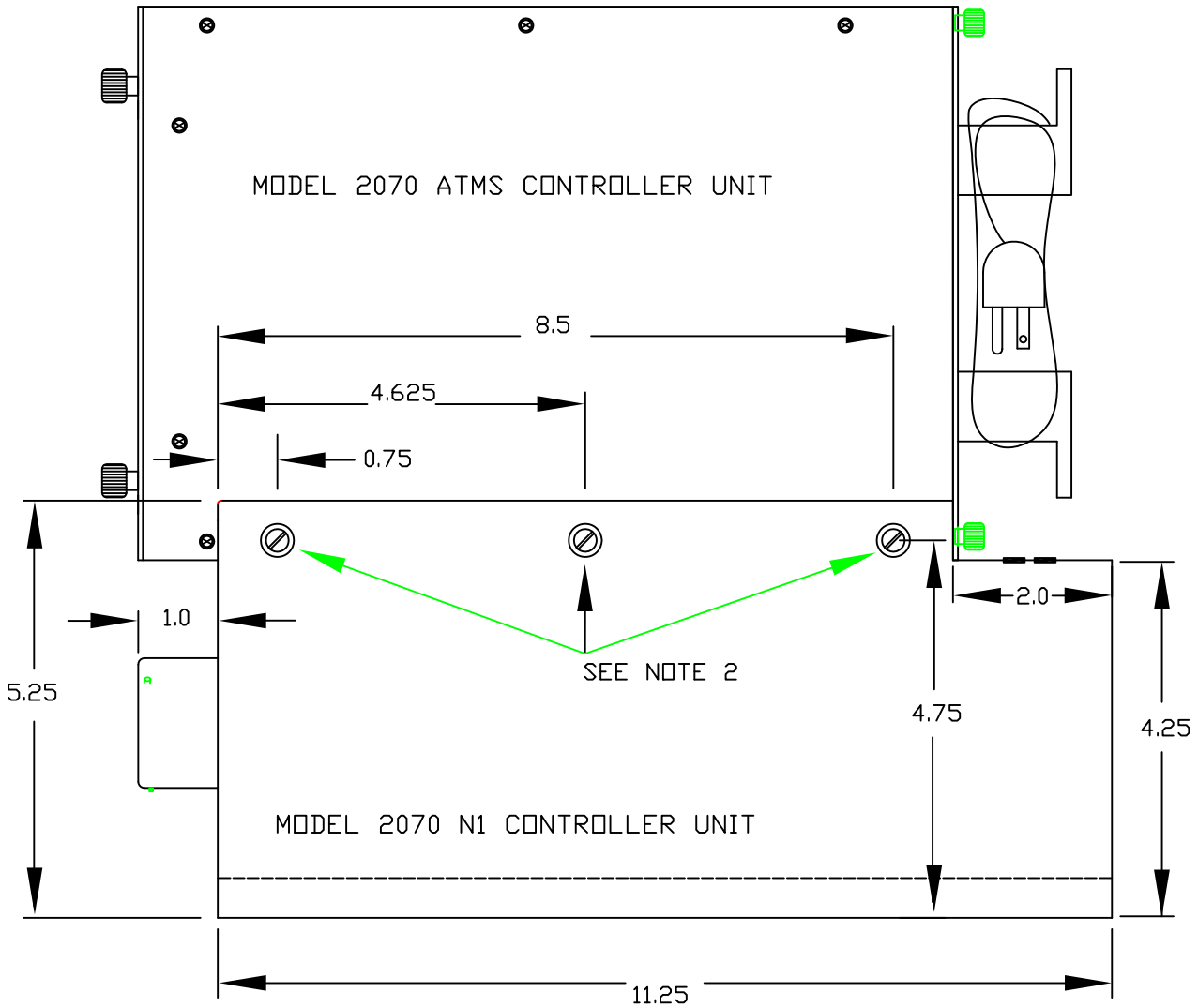
APPENDIX A11
CHAPTER 11 DETAILS



NOTES: (FOR THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for refernce.
2. The bottom supports shall be double flanged.
3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-55S Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25S Type)
   EX2 = Connector EX2 (DB-25S Type)
4. All dimensions shown are in inches.

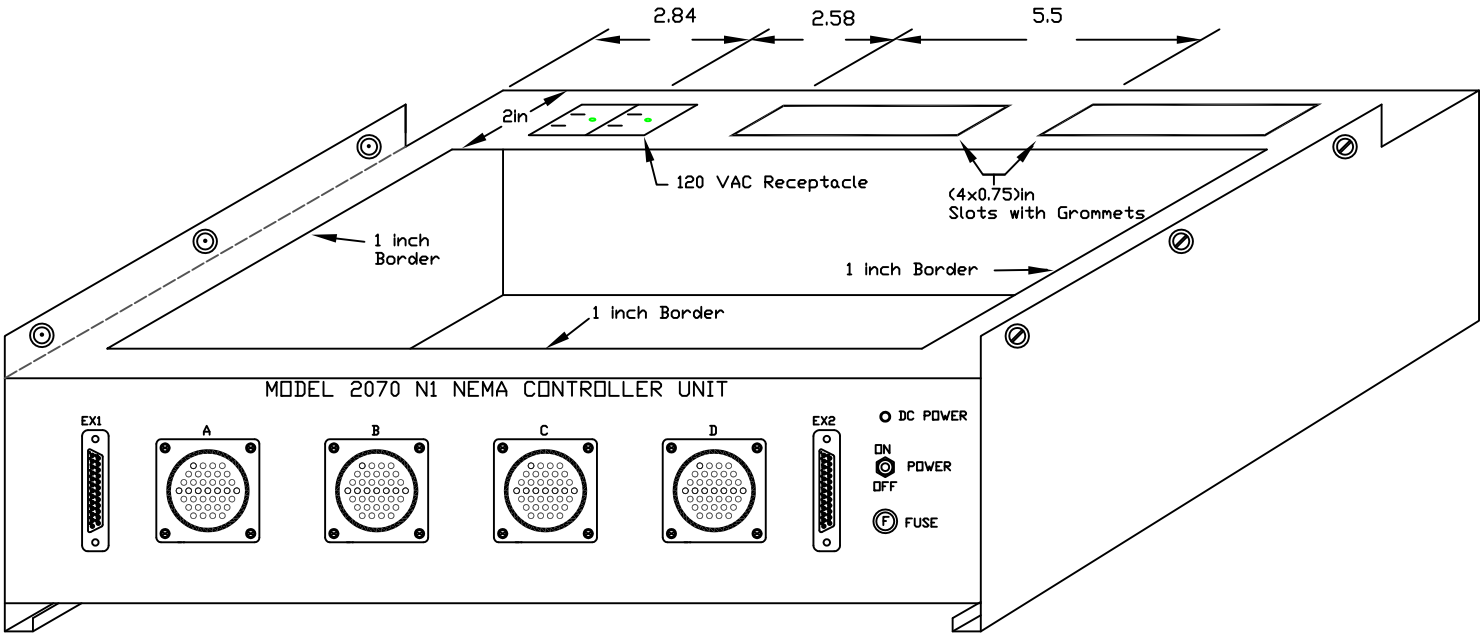
TITLE: 2070 (E or LX) N1 CONTROLLER UNIT FRONT VIEW	
	NO SCALE
TEES 2020	A11-1



NOTES: (FOR THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.
2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module.
3. All dimensions shown are in inches.

TITLE: 2070 (E or LX) N1 CONTROLLER UNIT SIDE VIEW	
	NO SCALE
TEES 2020	A11-2



NOTES: (FOR THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.

2. All dimensions shown are in inches.

TITLE: 2070 (E or LX) N1 CONTROLLER UNIT ISO VIEW	
	NO SCALE
TEES 2020	A11-3

CONNECTOR A			CONNECTOR B	
PIN	FUNCTION		FUNCTION	
	NAME	PORT	NAME	PORT
A	Fault Monitor	---	Phase 1 Next	8-1
B	+24 VDC External	---	Reserved	I9-5
C	Voltage Monitor	---	Phase 2 Next	8-2
D	Phase 1 Red	1-1	Phase 3 Green	3-3
E	Phase 1 Don't Walk	4-1	Phase 3 Yellow	2-3
F	Phase 2 Red	1-2	Phase 3 Red	1-3
G	Phase 2 Don't Walk	4-2	Phase 4 Red	1-4
H	Phase 2 Ped Clear	5-2	Phase 4 Ped Clear	5-4
J	Phase 2 Walk	6-2	Phase 4 Don't Walk	4-4
K	Phase 2 Vehicle Detector	I1-2	Phase 4 Check	7-4
L	Phase 2 Pedestrian Detector	I2-2	Phase 4 Vehicle Detector	I1-4
M	Phase 2 Hold	I3-2	Phase 4 Pedestrian Detector	I2-4
N	Stop Timing (Ring 1)	I6-2	Phase 3 Vehicle Detector	I1-3
P	Inh Max Term (Ring 1)	I6-3	Phase 3 Pedestrian Detector	I2-3
R	External Start	I8-1	Phase 3 mit	I5-3
S	Interval Advance	I8-2	Phase 2 mit	I5-2
T	Indicator Lamp Control	I8-3	Phase 5 Ped mit	I4-5
U	AC Neutral	---	Phase 1 mit	I5-1
V	Chassis Ground	---	Ped Recycle (Ring 2)	I7-5
W	2070N DC Ground	---	Reserved	I9-6
X	Flashing Logic ut	11-7	Reserved	I9-7
Y	Coded Status Bit C (Ring 1)	12-3	Phase 3 Walk	6-3
Z	Phase 1 Yellow	2-1	Phase 3 Ped Clear	5-3
a	Phase 1 Ped Clear	5-1	Phase 3 Don't Walk	4-3
b	Phase 2 Yellow	2-2	Phase 4 Green	3-4
c	Phase 2 Green	3-2	Phase 4 Yellow	2-4
d	Phase 2 Check	7-2	Phase 4 Walk	6-4
e	Phase 2 n	9-2	Phase 4 n	9-4
f	Phase 1 Vehicle Detector	I1-1	Phase 4 Next	8-4
g	Phase 1 Pedestrian Detector	I2-1	Phase 4 mit	I5-4
h	Phase 1 Hold	I3-1	Phase 4 Hold	I3-4
i	Force ff (Ring 1)	I6-1	Phase 3 Hold	I3-3
j	Min Recall All Phases	I8-4	Phase 3 Ped mit	I4-3
k	Manual Control Enable	I8-5	Phase 6 Ped mit	I4-6
m	Call To Non-Actuated I	I6-8	Phase 7 Ped mit	I4-7
n	Test Input A	I9-1	Phase 8 Ped mit	I4-8
p	AC Power	---	verlap A Yellow	10-2
q	I/ Mode Bit A	I8-6	verlap A Red	10-3
r	Coded Status Bit B (Ring 1)	12-2	Phase 3 Check	7-3
s	Phase 1 Green	3-1	Phase 3 n	9-3
t	Phase 1 Walk	6-1	Phase 3 Next	8-3
u	Phase 1 Check	7-1	verlap D Red	11-6
v	Phase 2 Ped mit	I4-2	Reserved	I9-8
w	mit All-Red Clear (Phase 1)	I6-7	verlap D Green	11-4
x	Red Rest Mode (Ring 1)	I6-4	Phase 4 Ped mit	I4-4
y	I/ Mode Bit B	I8-7	Not Assigned	---
z	Call To Non-Actuated II	I7-8	Max II Selection (Ring 2)	I7-6
AA	Test Input B	I9-2	verlap A Green	10-1
BB	Walk Rest Modifier	I9-4	verlap B Yellow	10-5
CC	Coded Status Bit A (Ring 1)	12-1	verlap B Red	10-6
DD	Phase 1 n	9-1	verlap C Red	11-3
EE	Phase 1 Ped mit	I4-1	verlap D Yellow	11-5
FF	Pedestrian Recycle (Ring 1)	I6-5	verlap C Green	11-1
GG	Max II Selection (Ring 1)	I6-6	verlap B Green	10-4
HH	I/ Mode Bit C	I8-8	verlap C Yellow	11-2

TITLE:

2070-8 FILELD I/ MODULE CONECTOR A & B

	NO SCALE
TEES 2020	A11-4

CONNECTOR C			CONNECTOR D	
PIN	FUNCTION		FUNCTION	
	NAME	PORT	NAME	PORT
A	Coded Status Bit A (Ring 2)	O12-4	Detector 9	I10-1
B	Coded Status Bit B (Ring 2)	O12-5	Detector 10	I10-2
C	Phase 8 Don't Walk	O4-8	Detector 11	I10-3
D	Phase 8 Red	O1-8	Detector 12	I10-4
E	Phase 7 Yellow	O2-7	Detector 13	I10-5
F	Phase 7 Red	O1-7	Detector 14	I10-6
G	Phase 6 Red	O1-6	Detector 15	I10-7
H	Phase 5 Red	O1-5	Detector 16	I10-8
J	Phase 5 Yellow	O2-5	Detector 17	I11-1
K	Phase 5 Ped Clear	O5-5	Detector 18	I11-2
L	Phase 5 Don't Walk	O4-5	Detector 19	I11-3
M	Phase 5 Next	O8-5	Detector 20	I11-4
N	Phase 5 On	O9-5	Detector 21	I11-5
P	Phase 5 Vehicle Detector	I1-5	Detector 22	I11-6
R	Phase 5 Pedestrian Detector	I2-5	Detector 23	I11-7
S	Phase 6 Vehicle Detector	I1-6	Detector 24	I11-8
T	Phase 6 Pedestrian Detector	I2-6	Clock Update	I12-1
U	Phase 7 Pedestrian Detector	I2-7	Hardware Control	I12-2
V	Phase 7 Vehicle Detector	I1-7	Cycle Advance	I12-3
W	Phase 8 Pedestrian Detector	I2-8	Max 3 Selection	I12-4
X	Phase 8 Hold	I3-8	Max 4 Selection	I12-5
Y	Force Off (Ring 2)	I7-1	Free	I12-6
Z	Stop Timing (Ring 2)	I7-2	Not Assigned	I12-7
a	Inhibit Max Timing (Ring 2)	I7-3	Not Assigned	I12-8
b	Test Input C	I9-3	Alarm 1	I13-1
c	Coded Status Bit C (Ring 2)	O12-6	Alarm 2	I13-2
d	Phase 8 Walk	O6-8	Alarm 3	I13-3
e	Phase 8 Yellow	O2-8	Alarm 4	I13-4
f	Phase 7 Green	O3-7	Alarm 5	I13-5
g	Phase 6 Green	O3-6	Flash In	I13-6
h	Phase 6 Yellow	O2-6	Conflict Monitor Status	I13-7
i	Phase 5 Green	O3-5	Door Ajar	I13-8
j	Phase 5 Walk	O6-5	Special Function 1	I14-1
k	Phase 5 Check	O7-5	Special Function 2	I14-2
m	Phase 5 Hold	I3-5	Special Function 3	I14-3
n	Phase 5 Omit	I5-5	Special Function 4	I14-4
p	Phase 6 Hold	I3-6	Special Function 5	I14-5
q	Phase 6 Omit	I5-6	Special Function 6	I14-6
r	Phase 7 Omit	I5-7	Special Function 7	I14-7
s	Phase 8 Omit	I5-8	Special Function 8	I14-8
t	Phase 8 Vehicle Detector	I1-8	Preempt 1 In	I15-1
u	Red Rest Mode (Ring 2)	I7-4	Preempt 2 In	I15-2
v	Omit All Red (Ring 2)	I7-7	Preempt 3 In	I15-3
w	Phase 8 Ped Clear	O5-8	Preempt 4 In	I15-4
x	Phase 8 Green	O3-8	Preempt 5 In	I15-5
y	Phase 7 Don't Walk	O4-7	Preempt 6 In	I15-6
z	Phase 6 Don't Walk	O4-6	Alarm 1 Out	O12-7
AA	Phase 6 Ped Clear	O5-6	Alarm 2 Out	O12-8
BB	Phase 6 Check	O7-6	Special Function 1 Out	O13-1
CC	Phase 6 On	O9-6	Special Function 2 Out	O13-2
DD	Phase 6 Next	O8-6	Special Function 3 Out	O13-3
EE	Phase 7 Hold	I3-7	Special Function 4 Out	O13-4
FF	Phase 8 Check	O7-8	Special Function 5 Out	O13-5
GG	Phase 8 On	O9-8	Special Function 6 Out	O13-6
HH	Phase 8 Next	O8-8	Special Function 7 Out	O13-7
JJ	Phase 7 Walk	O6-7	Special Function 8 Out	O13-8
KK	Phase 7 Ped Clear	O5-7	Not Assigned	---
LL	Phase 6 Walk	O6-6	Detector Reset	O11-8
MM	Phase 7 Check	O7-7	Not Assigned	---
NN	Phase 7 On	O9-7	+24 VDC	---
PP	Phase 7 Next	O8-7	2070N DC Gnd	---

TITLE: 2070-8 FILELD I/O MODULE CONECTOR C & D

NO SCALE

TEES 2020

A11-5

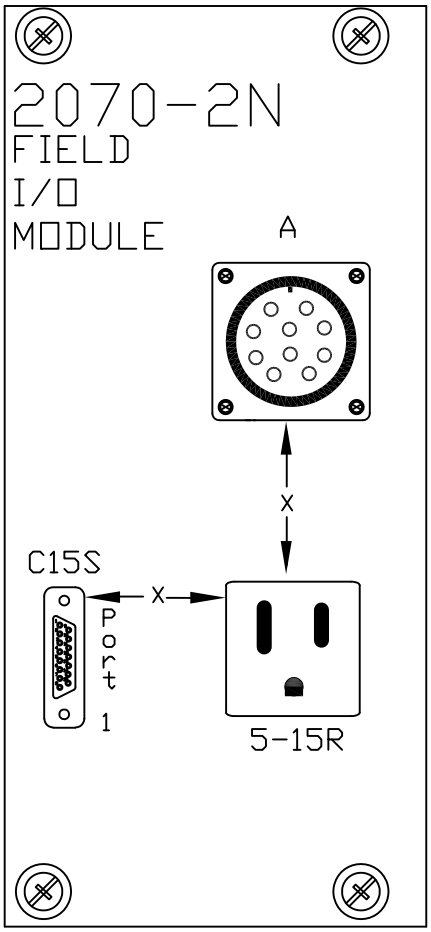
EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD (FCU)
3	RXD (FCU)
4	RTS (FCU)
5	CTS (FCU)
6	NA
7	2070-8 DC GND
8	DCD (FCU)
9	2070-8 DC GND
10	SP3TXD+
11	SP3TXD-
12	SP3TXC+
13	SP3TXC-
14	2070-8 DC GND
15	SP3RXD+
16	SP3RXD-
17	2070-8 DC GND
18	SP3RXC+
19	SP3RXC-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EG (Equipment Ground)
2	TXD (Channel 1)
3	RXD (Channel 1)
4	RTS (Channel 1)
5	CTS (Channel 1)
6	NA
7	IFC GND
8	DCD (Channel 1)
9	AUDIO IN (Channel 1)
10	AUDIO IN (Channel 1)
11	AUDIO OUT (Channel 1)
12	AUDIO OUT (Channel 1)
13	NA
14	EG (Equipment Ground)
15	TXD (Channel 2)
16	RXD (Channel 2)
17	RTS (Channel 2)
18	CTS (Channel 2)
19	NA
20	IFC GND
21	DCD (Channel 2)
22	AUDIO IN (Channel 2)
23	AUDIO IN (Channel 2)
24	AUDIO OUT (Channel 2)
25	AUDIO OUT (Channel 2)

TITLE:

2070-8 FIELD I/O MODULE
EX1 & EX2 CONNECTOR

	NO SCALE
TEES 2020	A11-6



FRONT VIEW

2070-2N FIELD I/O FACE PANEL

A PIN ASSIGNMENT	
PIN	FUNCTION
A	AC Neutral
B	NA
C	AC Line
D	NA
E	NA
F	Fault Monitor
G	DCG #2
H	EG
I	NA
J	NA

C15S PIN ASSIGNMENT	
PIN	FUNCTION
1	SP3TXD+
2	DCG #2
3	SP3TXC+
4	DCG #2
5	SP3RXD+
6	DCG #2
7	SP3RXC+
8	DCG #2
9	SP3TXD-
10	Port 1 Disable
11	SP3TXC-
12	EG
13	SP3RXD-
14	Reserved
15	SP3RXC-

NOTES: (FOR THIS DETAIL)

1. 2070N Faceplate shall be 4X wide.
2. RS-485 Termination Resistors (120 Ohms) provided external to module.
3. Dimension "X" shall be minimum of 1.00 in.
4. A - Intermate with MS3106()-18-1S. C15S - 15-Pin DB Socket Type.
5. EG (Equipment Ground) pin is electrically connected to the faceplate.
6. Port 1 Disable: 0VDC = Disable.
7. Front panel shall be Aluminum stock or Stainless Steel.
8. All dimensions shown are in inches.

TITLE: MODEL 2070-2N FILELD I/O MODULE	
	NO SCALE
TEES 2020	A11-7

TEES 2020
Release Notes Ver. 2.0
11/6/2020
Herasmo Iniguez

Errata No. 1 additions in Blue
Errata No. 2 Changes in Red
Errata No. 3 Changes in Green
Errata No. 4 Changes in Brown
TEES 2020 Changes in Purple

Item	Description of Item	Section
1	Adds Specifications for Model 2020-CELL Module	Chapter 10 Section 14
2	Creats a new Model 2070-1M CPU Module	Chapter 9 Section 1
3	Makes further enhancements to the Model 2070LX+ Controller	Chapter 9 text and Drawings
4	Incorporates all comments	TEES 2020
5	Adds additional specifications to the 700 signs requiring compliance to Nema 4X vs 3R for water resistance.	Chapter 13-Section 11
	TEES 2020 Integrates the following Erratas:	
	Errata No.1	
6	Creates Model 2070E	9.1.1
7	Completes ver Module for 2070E controller	9.2.7.6.1, 9.2.7.6.4
8	Creates Model 2070-7G GPS Module for 2070	10.9.1
9	Creates C11 Harness for the Cabinets	A3-7
10	Adds Health Circuit to the cabinet.	
	Errata No.2	
11	Creates 242L DC Isolator	5.4.1 - 5.4.7
12	Creates Model 342LX, 344LX, and 346LX Cabinets	6.1.1.3 - 6.1.1.5
13	Creates r4 and r8 Drives for the controller	9.2.7.2.2
14	Standardizes Network Communications and disables Telnet and FTP for Cybersecurity.	9.2.7.1
15	Creates Model 2070-2E+ Field I/O Module	9.1.1, 9.3.8.7
16	Fixes Model 2070-7G GPS Module for 2070	10.9.2

17	Integrates C11 Harness into the Model 332L and 342LX Cabinets for bicycle detection.	6.1.1.5
18	Creates independent equipment circuit in the cabinets.	
19	Creates C1 Harness	6.4.8.1
	Errata No.3	
20	Includes specifications for Intelligent Detector Model 222i and 224i	5.7.1
21	Makes Model 332L, 334L and 336L Cabinet touch safe and renames cabinets as 332LS, 334LS and 336LS.	6.1.1
22	Adds encryption requirements to Model 2070E controller for Cybersecurity.	Detail A9-1, A9-10, 9.1.1, 9.5.1, 9.2.3, 9.2.5, 9.2.8, Detail A9-15
23	Updates Model 2070LX to address Cybersecurity	9.2.5.9
24	Creates Wireless Serial and Ethernet Modules for Model 2070 Controller.	10.11.1
25	Integrates Standarized Railroad Preemption Interface to Model 332LS and 342LX Cabinets.	Chapter 6, Page 59, Details A6-5, A6-21, A6-24, A6-25, A6-38, A6-38, A6-46, A6-47, A6-48, A6-50, A6-51, A6-52
26	Includes specifications for Model 2070-J Module	Chapter 19
27	Includes specifications for Model 700/700C CMS	Chapter 13, refer to model 700 CMS Specifications
28	Includes specifications for Model GT-BBS Green Technology BBS	A4-2
	Errata No.4	
29	Includes specifications for Model 2070LX+ Controller	Chapter 9, 9.6
30	Includes redesign of internal network of Model 700/700C CMS	13.3, 13.11
31	Includes redesign of SPA for 332LS and 342LX Cabinets	Chapter 6, Details A6-1, A6-2, A6-3, A6-4, A6-5